

The Module Controller Chip (MCC) of the ATLAS Pixel Detector

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Abstract

The ATLAS pixel detector is organized in 3 barrels and 5 forward and backward disks. The basic building block for each of those detector components is the detector module. There are a total of 2,228 of them, each one having 16 analog Front-End (FE) chips, bump-bonded to individual diodes of a silicon detector, and a Module Controller Chip (MCC). There are 61,440 channels in a module for an active area $16 \times 64 \text{ mm}^2$ which are controlled and read out by a MCC. Therefore in total there are 1.4×10^8 channels to be read out the whole detector. Main LHC constraints are 40 MHz bunch crossing, 75 kHz Level 1 trigger rate, $2.5 \mu\text{s}$ Level 1 trigger latency and a dose of 300 kGy ($1 \times 10^{15} \text{ cm}^{-2}$ 1 Mev neutron equivalent fluence), for the innermost barrel. The MCC described in this paper is a non rad-hard version which is used for the ATLAS pixel demonstrator program. The aim of this program is to demonstrate the feasibility and the robustness of the detector module. The MCC is a large digital circuit that implements complex functions like complete Event Building and Trigger, Timing and Control logics. This paper describes the MCC architecture, the adopted design methodology and some of the measurements made on the silicon samples.

I. INTRODUCTION

The LHC accelerator will challenge the ATLAS Pixel Detector both for rad-hard resistance and data flow rate.

The whole pixel detector [2] will have 1.4×10^8 channels with few thousand hits per beam crossing, occurring every 25 ns .

The detector module [3], shown in Figure 1 has an active area of $16 \times 64 \text{ mm}^2$ with 61,440 channels. Each sensor element of $300 \times 50 \mu\text{m}^2$ is connected to an electronic front end channel of the same size. The module is made up of 16 analog Front-End (FE) chips which are bump-bonded to the pixel detector, and of a digital Module Controller Chip (MCC).

Data are transmitted from FE's to MCC by 16 serial links read out in parallel by the MCC. The communication between the MCC and the Read Out Drivers (ROD) sitting in the counting room use optical fibres. Optical transmitters use Vertical Cavity Surface Emitting Lasers (VCSEL), while a pin diode is used as optical receiver. This scheme provides a bandwidth of 40 Mbit/s per line. Two outgoing data lines are provided, while incoming data are encoded together with the system clock using a Biphasic Mark Encoding scheme. The clock signal is locally restored on the MCC. All data links between the MCC and the 16 FE's use Low Voltage Differential Signalling (LVDS) drivers in order to reduce EMI and to balance current flow. Standard CMOS drivers are used for signals which are not active during data acquisition.

Data links have a star topology with the MCC acting as

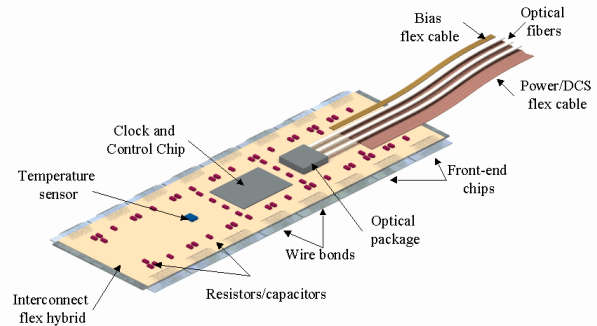


Figure 1: ATLAS Pixel Detector module.

data concentrator. This topology was chosen to improve fault tolerance. Event readout from a FE is done as soon as an event is selected by a LV1 trigger. This “data push” algorithm minimizes the time an event waits in a FE and therefore the size of local FE memories.

A simplified block diagram of a whole module can be seen in Figure 2.

Each FE has 3,840 channels which are organized in a matrix of 24 columns by 160 rows. Every channel, in addition to a charge sensitive amplifier, includes a comparator with programmable threshold, and a local hit-storage and read-out logic. As parts of the readout logic in the pixel can be shared between pixels, two columns with pixels arranged back to back form a column pair. The logic at the bottom of the column pair receives the hit information, stores it into buffers and selects hits associated with LV1 triggers. A coarse measurement of the released charge in the detector by a particle is obtained by measuring the time-over-threshold (ToT), with a 7 bit resolution, in the discriminator.

Only data associated to a level one (LV1) trigger are sent out from the FE chips to the MCC.

The MCC, whose architecture will be described in the next section, receives data from 16 FE chips in parallel, performs an event building (and eventually some error recovery function) and sends out the reconstructed events.

The MCC, in addition, distributes the clock to all the FE chips of one module, it initializes all FE's at startup, and it has Trigger and Timing logic able to handle correctly the control signals needed by the FE's to do event readout.

The ATLAS Pixel Collaboration is building a “detector module demonstrator” which will implement all the final requirements of the system with the following exceptions:

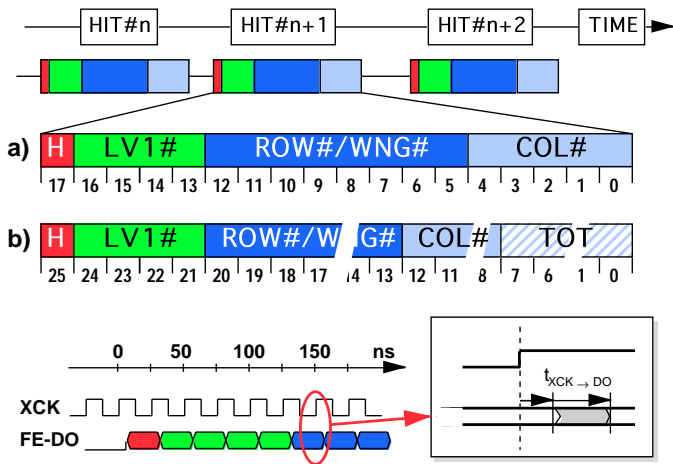


Figure 4: FE—MCC data protocol

Fast commands can be issued during data acquisition (for example the LV1—trigger command). Slow commands automatically set the MCC out of data acquisition mode and are meant for configuration and test purpose only.

TTC (Trigger and Timing Control): This block mainly deals with the LV1 commands. It has the ability to block the LV1 sent to the FE chips in case to many events are still to be reconstructed; this is necessary in FE/MCC data push architecture to avoid synchronization lost.

Module Port: This block performs the interface between the MCC and the ROD's. In this version of the chip the interface uses LVDS drivers, in the final ATLAS chip it will do optical encoding/decoding and it will directly interface with the opto—electronic components.

Clock Tree: Clock distribution for the detector module is done by the MCC. In order to minimize clock skew on the module the clock signal received by the MCC is buffered inside the chip and re—distributed to the FE chips and to the via the XCK pin. This buffered clock signal is also fed-back to the MCC itself from the XCKIN pin and used both to synchronize data from the FE chips and to clock the chip core.

All the data transmission lines between FE—MCC and MCC—ROD use a serial transmission format with a header and a trailer which allows automatic recover in case of transmission errors. Event data are transmitted using “single hit frames” from the FE chips and using “full event frames” from the MCC.

III. DATA FORMAT PROTOCOL

Serial protocols have been chosen in order to minimize the number of interconnection lines between FE chips and MCC and between MCC's and ROD's.

Figure 4 shows event data format from FE chips: each hit is encoded using a fixed length frame of 18 bits (26 if the optional ToT information is selected). There are: 1 header bit to wake up the receiver, 4 bits to identify the LV1 trigger

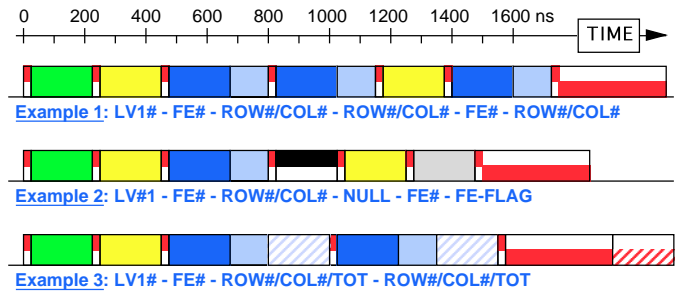


Figure 5: MCC—Rod data protocol

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number, 8 row number and 5 column number bits. All possible errors, warnings and EoE messages from the FE's are coded in the unused 8-bit row number (row numbers from 224 to 255). A row number above 224 is always interpreted as an EoE. Individual hits, belonging to the same event, can be separated by any number of zeroes. Once an event is finished an End-of-Event (EoE) word is sent to the MCC. This EoE word has to be sent to the MCC even if there are no hits associated with the event. One EoE word for each FE is in fact needed by the MCC in order to start the event building. Detailed simulations show that data rate on these links is relatively low, which allows automatic data recovery if a gap of more than 18 (26) zeroes appear in the data stream.

The data stream generated by the MCC is little more complicated as all information is organized on an event format. All information sent out by the MCC is organized in data—blocklets preceded by a header (“1”) and followed by a trailer (“100_0000_0000_0000”). This trailer is a unique pattern if the data stream is interleaved by synchronization bits (“1”). Each event is defined by an 8 bit LV1 number, which labels the event, an 8 bit FE number followed by all hits belonging to this FE organized in an 8 bit row number, 5 bit column number and possibly by an optional 8 bit ToT. After the first non empty FE data has been transmitted a second 8 bit FE number followed by row, column, ToT is serialized. Possible error or warning flags produced by the MCC are coded in the data stream. Figure 5 shows an example of MCC data format.

Event by event coding opposed to hit by hit coding allows a significant data compression. Even then simulations show that for the innermost barrel a bandwidth of 40 MHz/s is not sufficient and therefore two data lines connecting the MCC to the ROD's are needed. Use of two optical links allows redundancy in the links (in case of failure of one connection) at least for the two outermost barrels and reduced data loss in case of a broken link in the innermost barrel.

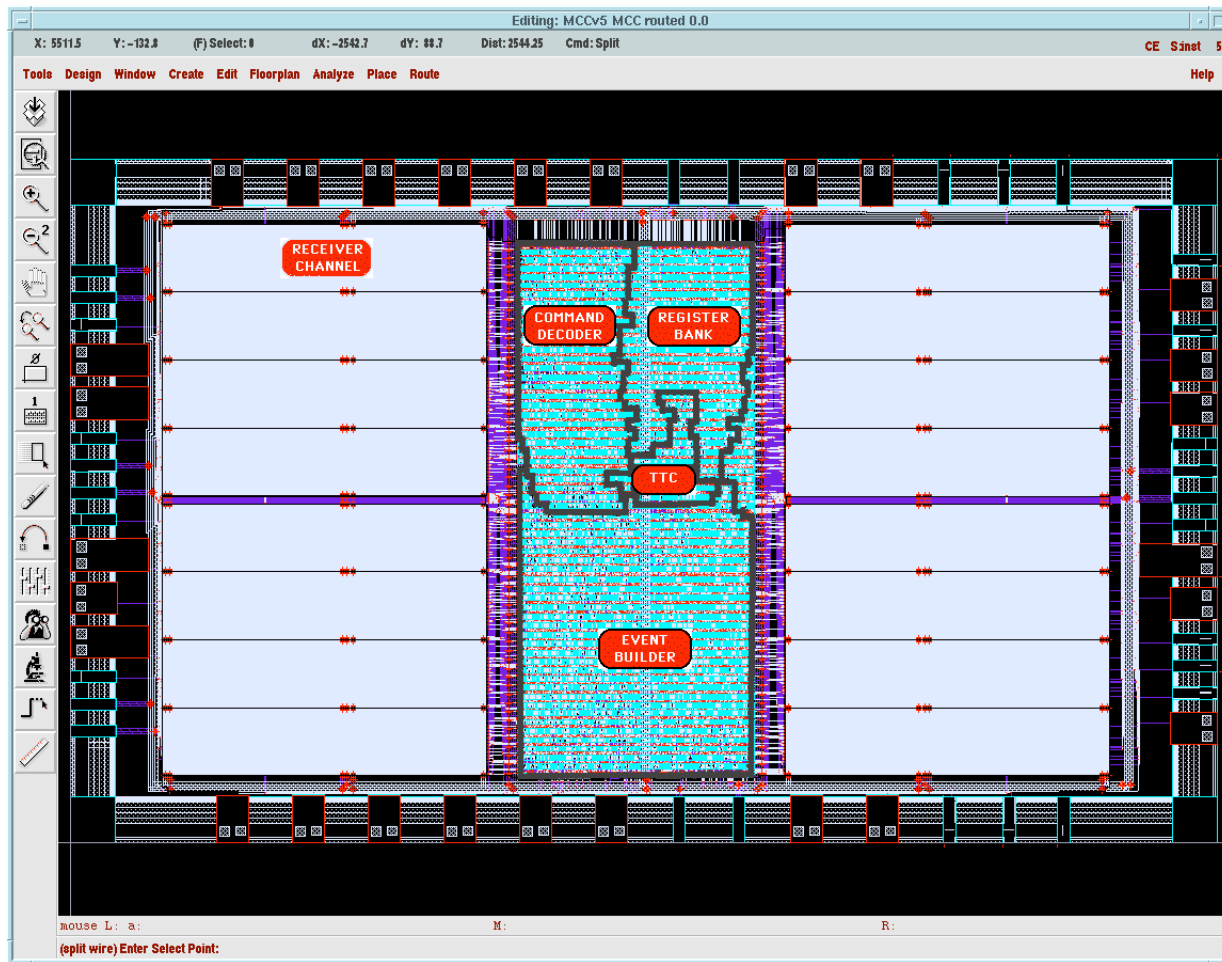


Figure 6: MCC Layout. All main building blocks are highlighted.

IV. DESIGN METHODOLOGY AND CHIP LAYOUT

Figure 6 is a plot of the routed chip. All the main building blocks (described in section II) are highlighted. The chip has 83 Input-Output pads, 57 of them are full-custom LVDS drivers or receivers. The main area of the chip is occupied by 16 identical blocks: the *Receiver's* which contain the full custom FIFO. The FIFO occupies approximatively half of the size of a single *Receiver*. The central part includes the *Event Builder*, the *TTC* and the *Register Bank*.

Given the high structural complexity of the MCC the design methodology chosen is completely based on behavioural description, logic synthesis and automatic placement and routing. The CAE tools used for the design of the MCC are from CadenceTM, while the libraries and technology files are from AMSTM (Austria Mikro Systeme). The main design steps are:

Functional description: VERILOG

The chip has been described at behavioural level using the VerilogTM simulation language. This approach allows a high level description and simulation of the whole architecture, which in turn allows to develop all the main building blocks using a top-down approach.

Correct functionality has been validated by a large number of test vectors (more than one million clock cycles).

Logic synthesis: SYNERGY

The Verilog description has been synthesized using the SynergyTM package and mapped to the 3.3 V, 0.8 μm CMOS library from AMS. This approach eases the realization of very complex state machines present, for example, in the *Command Decoder* (more than 100 states!).

The synthesized design is realized with 18,000 standard cell instances.

Floor planning and Routing: CELL ENSEMBLE

LVDS I/O pads and all 16 FIFO's are full custom blocks which were manually placed. A clock tree has been realized in order to keep signal skews at a minimum. We used the following approach: in each region of standard cells we inserted a column of buffers (one in each standard cell row) connected in parallel in order to realize a big "distributed buffer" which minimizes routing length of clock signals to all Flip-Flops. In order to drive this big buffer, realized with approximatively

200 standard cell buffers, a clock tree was built. Standard cells placement and routing were done automatically using the Cell Ensemble TM software package. Also the routing of signal lines going from the 16 *Receivers* to the *Event Builder* were hand routed.

Final steps

The final steps required design rule check (DRC) and layout/schematic comparison at transistor level (LVS). All the capacitance load of the wires has been extracted, producing a back-annotated netlist. A Verilog back annotated simulation validated all the timing relations. A detailed simulation of the clock skew has been performed. Particular care was taken in ensuring that all data was correctly validated by the latches present in the design in order to deal correctly with the clock distributed to the whole module by the MCC itself.

V. MCC AND MODULE TESTS

The whole design was submitted at mid of April to AMS. Together with the MCC also a fully CMOS version of the FE chip was submitted on the same reticle. At the beginning of July, 15 4" wafers, containing 34 MCC's and 34 FE chips each, were received.

All the MCC's were tested by the foundry with a set of Test-Vectors running at a frequency of 10 MHz.

Power consumption measurements were done up to 20 MHz. These measurements show a power consumption of 120 mW at 20 MHz with LVDS outputs terminated at 100 Ω . Extrapolating power consumption up to 40 MHz a total power consumption of 210 mW results. Detailed measurements on power consumption at 40 MHz are still to be done.

The total yield of this batch was 64%.

15 chips were packaged using an 84 pin CLCC ceramic package in order to ease the first tests in the laboratory.

All tested chips worked fine up to 40 MHz which is the target clock speed.

In order to perform the test of the whole system a dedicated test setup was realized. The main issue being the ability to test each component independently in order to decouple eventual problems, our setup is composed by a VME crate hosting a board able to communicate either with the MCC or with one single FE. This board is controlled by software through a PC with LabWindows and has to be able to support both MCC and FE data protocol. On line histogramming and direct storage of event data coming from the chips directly on board is possible, in order to be able to cope with 40 Mbit/s data rate.

Three kind of test boards were realized by our community. A Single FE chip board allows to test a single FE bump-bonded to a small silicon pixel detector realized ad hoc. A second single board hosting the MCC was built in order to allow the testing of a stand alone MCC, or an MCC connected to only one FE chip, if these two boards are connected together. The third board is a module support board where a detector with 16 FE chips can be connected to a packaged MCC or the complete module (including the kapton Flex-Hybrid glued on top of the detector with the MCC wire-bonded to it) can be tested.

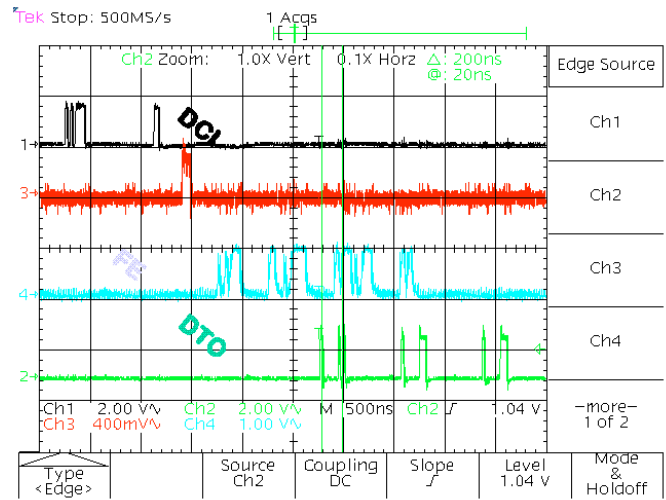


Figure 7: Event Readout through the MCC

This provides a very convenient way to proceed because it allows all institutions collaborating to the project to test first their single parts and then provide a way to test the final module at each step of its realization using always the same experimental setup. As an example for that, this setup allowed to test many different detector layouts in order to understand the best design building single chip detectors with different geometries, both in the lab and in a Test-Beam at CERN. All these detectors were also irradiated to the maximum expected dose for 10 years of LHC operation.

At the moment we were able to test completely an MCC connected to a single FE chip ensuring that all the communication protocols between the MCC and the FE and between the MCC and the Read Out Driver work up to 40 MHz. Measurements for both non irradiated and irradiated detectors and FE chips were successfully performed.

The test of the whole module is under way and some very preliminary results can be seen in Figure 7. This figure represents an event read out by the MCC. One can see the command sent to the MCC (DCI), the output of the FE and the output of the MCC (DTO).

VI. CONCLUSIONS

In this article we presented the architecture of the Module Controller Chip and the way it has been designed. A full event builder plus trigger and control logic has been coded in silicon using more than 400,000 transistors for a final die size of $10.6 \times 6.3 \text{ mm}^2$. The chip design was done using AMS 0.8 μm technology. A complete 25×32 bit full-custom FIFO has been designed, while the rest of the chip was done using Standard Cells.

At the moment of writing the Front-End (FE) chips and the silicon detector have been successfully tested in a Test Beam at CERN. The MCC has been tested in the lab and tests on a whole module are being performed. This will provide the complete functionality of the ATLAS Pixel Demonstrator program.

Future plans are to develop a rad-hard module which meets all ATLAS specifications. This module will include a fully

rad-hard version of the MCC with some minor changes in his architecture in order to be able to cope with the radiation requirements of LHC. Particular attention will be putted into tolerance of data with respect to Single Event Upset phenomena. As the final version of the chip will have to be interfaced with optical fibres (one incoming and two outgoing fibres), optical drivers and receivers are being developed by the ATLAS Pixel Collaboration.

The goal is to integrate these devices in the final version of the MCC in order to provide a Module Controller Chip capable to deal with all the interfacing between the 1×10^8 electronic channels provided by the detector, and read out by 16 Front-End chips, and the Read Out Drivers.

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VII. REFERENCES

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