



# MCC-FDR: Layout & Timing Verification

Giovanni Darbo / INFN - Genova

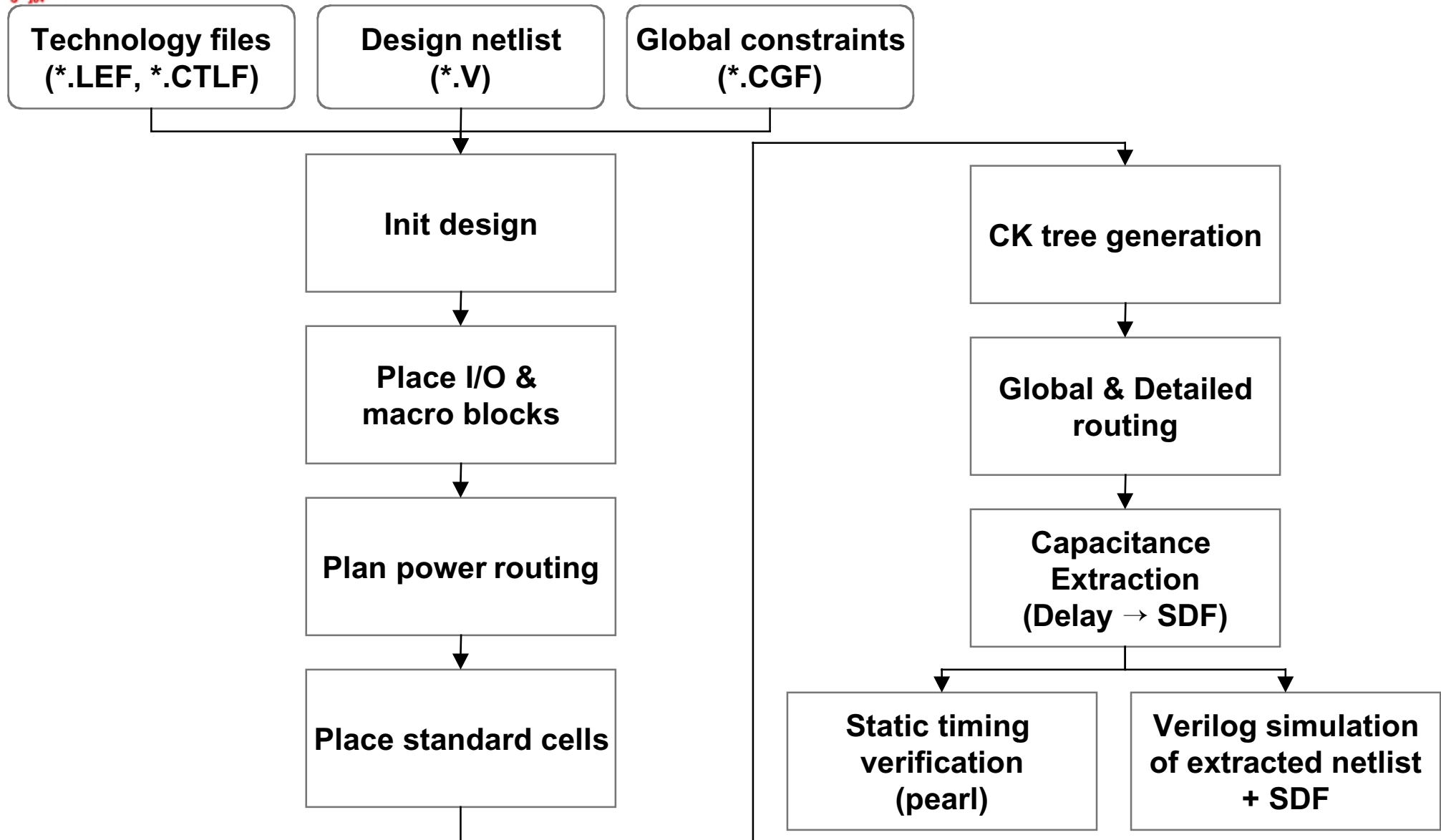
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## Talk highlights:

- Design Flow;
- Technology files;
- Pinout & Size;
- Floorplanning;
- Clock tree synthesis;
- Time driven Place & Route.



# Silicon Ensemble Design Flow





# Silicon Ensemble Tech File (LEF)

- The technology LEF file define the geometrical rules necessary for SE to do place & route
- We have modified the CERN/RAL technology file used by Silicon Ensemble (**cmos6sf25TechLib.lef** → **cmos6sf25TechLib\_5LM2V.lef**):
  - ↳ From 3 metals (M1, M2, MZ) to 5 metals (M1, M2, M3, M4, LM);
  - ↳ New values for plate/edge capacitance of wires;
  - ↳ Added via resistance (Max value:  $7\Omega/\text{via}$ );
  - ↳ Defined double cut vias to increase yield and stacked vias to increase routing density;
  - ↳ Added antenna default pin value: Silicon Ensemble can repair antenna violation;

# LEF-Metal Capacitance: Formulas for Plate/Edge Capacitance

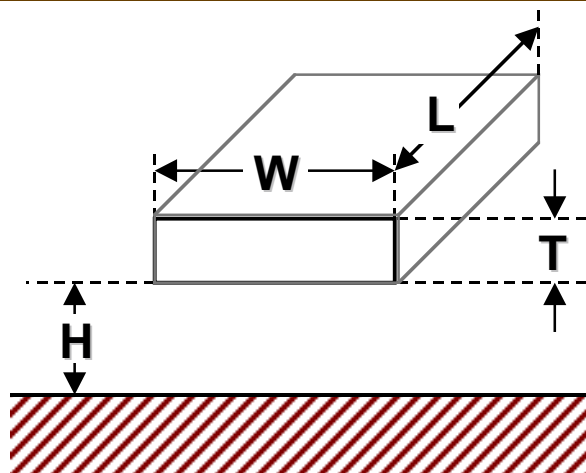


Plate / Edge capacitance calculation				
Metal	H ( $\mu\text{m}$ )	T ( $\mu\text{m}$ )	C (plate) (pF/ $\mu\text{m}^2$ )	C (edge) (pF/ $\mu\text{m}$ )
M1	1.035	0.40	3.507E-05	5.470E-05
M2	2.235	0.54	1.624E-05	4.686E-05
M3	3.575	0.54	1.015E-05	4.053E-05
M4	4.915	0.54	7.386E-06	3.696E-05
MZ	6.255	0.73	5.804E-06	3.760E-05
H = Metal high from substrate				
T = Metal thickness				

- Plate capacitance per square unit:

$$C_{\text{plate}} = \frac{\epsilon WL}{H}$$

- Edge capacitance per unit length:

$$C_{\text{edge}} = \epsilon \left( \frac{\pi}{\ln \left( 1 + 2 \frac{H}{T(1 + \sqrt{1 + \frac{T}{H}})} \right)} - \frac{1}{4} \frac{T}{H} \right)$$

- H is the height of the metal layer to substrate (table 64, pg. 94);
  - T is the metal thickness (table 65, pg. 95);
  - $\epsilon_r = 4.1$  (par. 4.9.2, pg. 94).
- (CMOS 6SF & CMS 6SFS Design Manual May 12, 2000)

↳ [Ref: Lance A. Glasser & Daniel W. Dobberpuhl, The design and Analysis of VLSI Circuits, Addison Wesley, pg.135-136.](#)



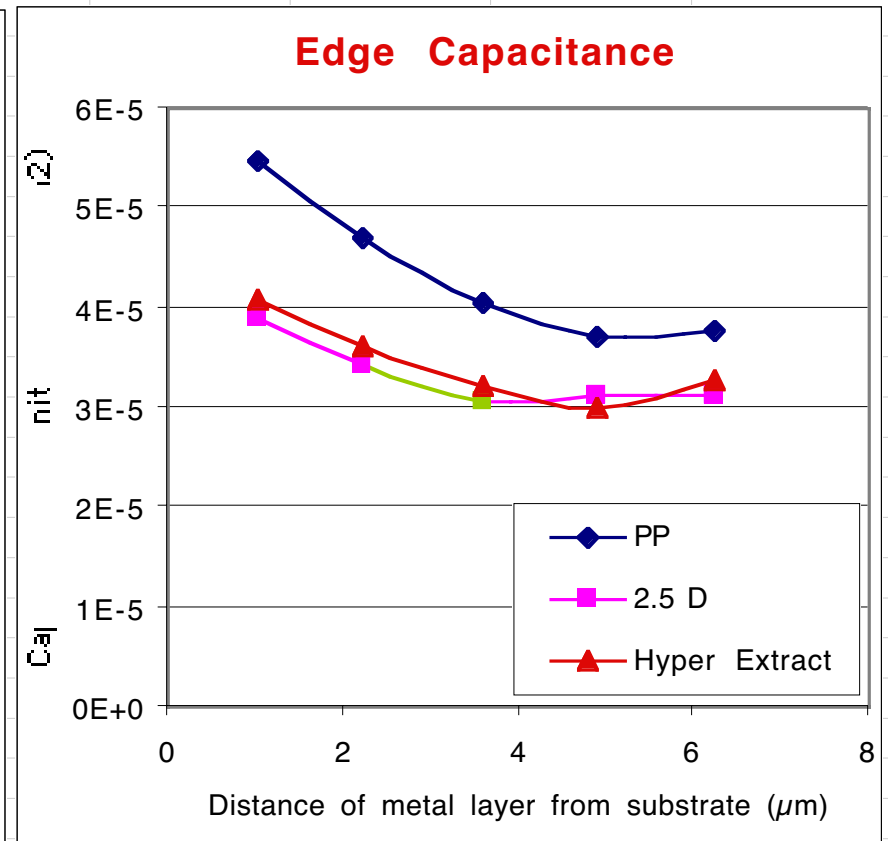
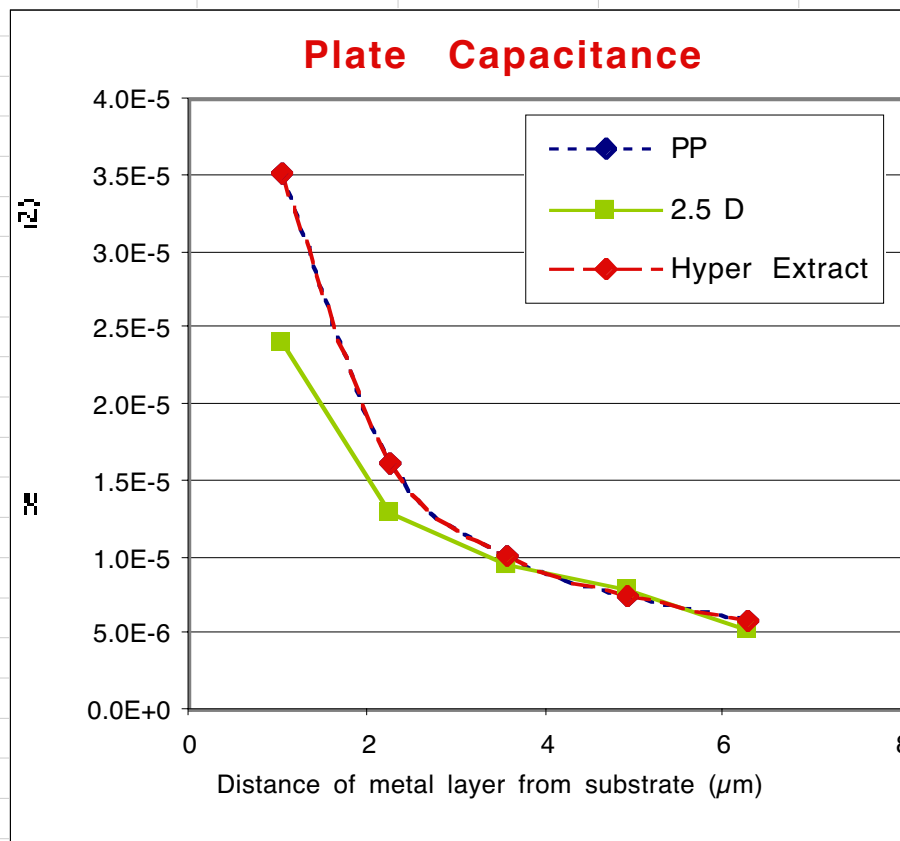
# Capacitance used by SE

- Silicon Ensemble use a “parallel plate” (PP) model for wire capacitance. The values we have used are the capacitance from the metal to substrate for isolated wires. Those values are optimistic.
- Once the design is routed, the interconnect delay/parasitics information (SDF/RSPF), to be used for static timing verification (Pearl) and Verilog simulation, is extracted using a 3D model (HyperExtract) that considers also inter metal and inter wire (at minimum pitch) capacitance. Those values are pessimistic since routing is not everywhere at minimum pitch.
- There is also a 2.5 D model for extraction of wiring
- Next slide compares the plate and the edge capacitance for minimum size metal to substrate (SUB)



# Capacitance Extraction Models: Comparison

Plate / Edge capacitance calculation								
Metal	H ( $\mu\text{m}$ )	T ( $\mu\text{m}$ )	PP		2.5 D		HyperExtract	
			C (plate) ( $\text{pF}/\mu\text{m}^2$ )	C (edge) ( $\text{pF}/\mu\text{m}$ )	C (plate) ( $\text{pF}/\mu\text{m}^2$ )	C (edge) ( $\text{pF}/\mu\text{m}$ )	C (plate) ( $\text{pF}/\mu\text{m}^2$ )	C (edge) ( $\text{pF}/\mu\text{m}$ )
M1	1.035	0.40	3.507E-05	5.470E-05	2.40E-05	3.89E-05	3.51E-05	4.09E-05
M2	2.235	0.54	1.624E-05	4.686E-05	1.29E-05	3.43E-05	1.62E-05	3.61E-05
M3	3.584	0.54	1.013E-05	4.050E-05	9.50E-06	3.05E-05	1.02E-05	3.22E-05
M4	4.915	0.54	7.386E-06	3.696E-05	7.87E-06	3.11E-05	7.39E-06	2.99E-05
LM	6.255	0.73	5.804E-06	3.760E-05	5.20E-06	3.11E-05	5.80E-06	3.28E-05





# LEF: Double Cut and Stacked Vias

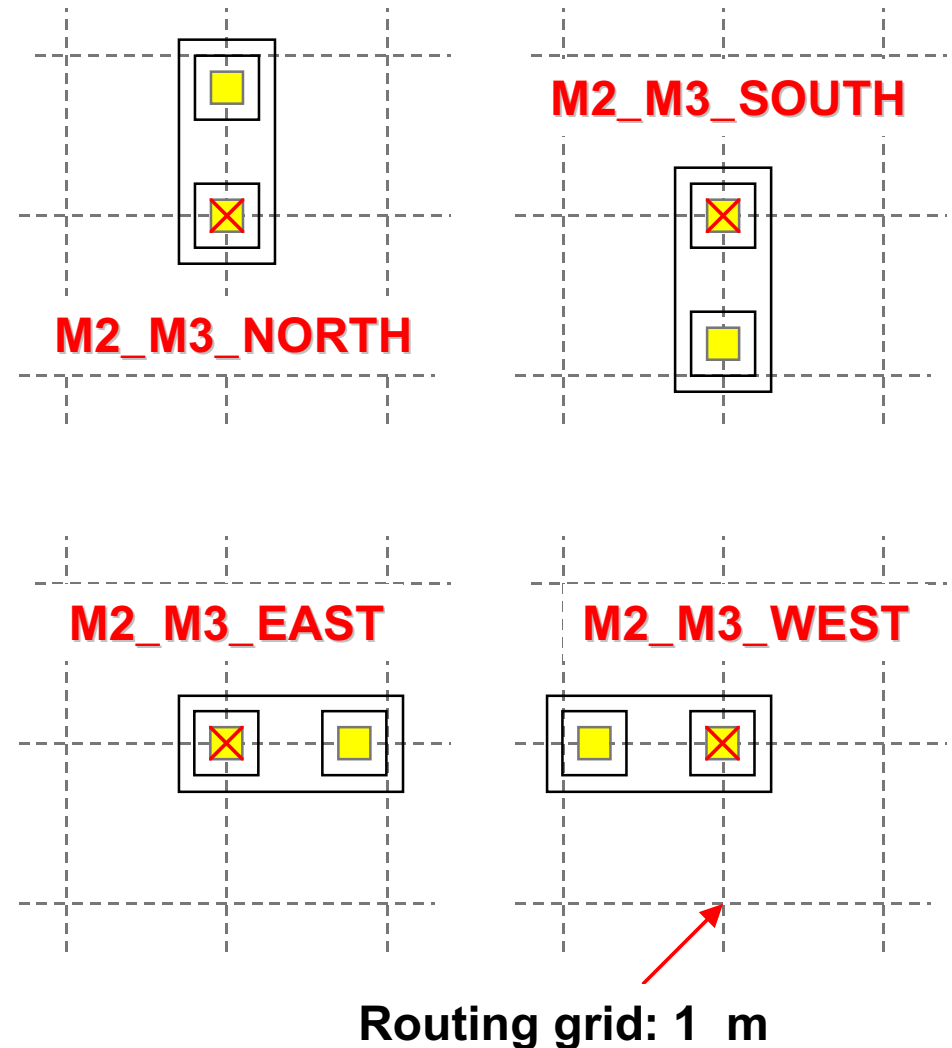
Via definition extracted from technology LEF file:  
**cmos6sf25TechLib\_5LM2V.lef**

```
# Four double cut vias between M2/M3
VIA M2_M3_NORTH DEFAULT
  RESISTANCE 3.5 ;
  LAYER M2 ;
    RECT -0.26 -0.26 0.26 1.06 ;
  LAYER V2 ;
    RECT -0.18 -0.18 0.18 0.18 ;
    RECT -0.18 0.62 0.18 0.98 ;
  LAYER M3 ;
    RECT -0.26 -0.26 0.26 1.06 ;
END M2_M3_NORTH

VIA M2_M3_SOUTH DEFAULT
  ...
END M2_M3_SOUTH

VIA M2_M3_EAST DEFAULT
  ...
END M2_M3_EAST

VIA M2_M3_WEST DEFAULT
  ...
END M2_M3_WEST
```

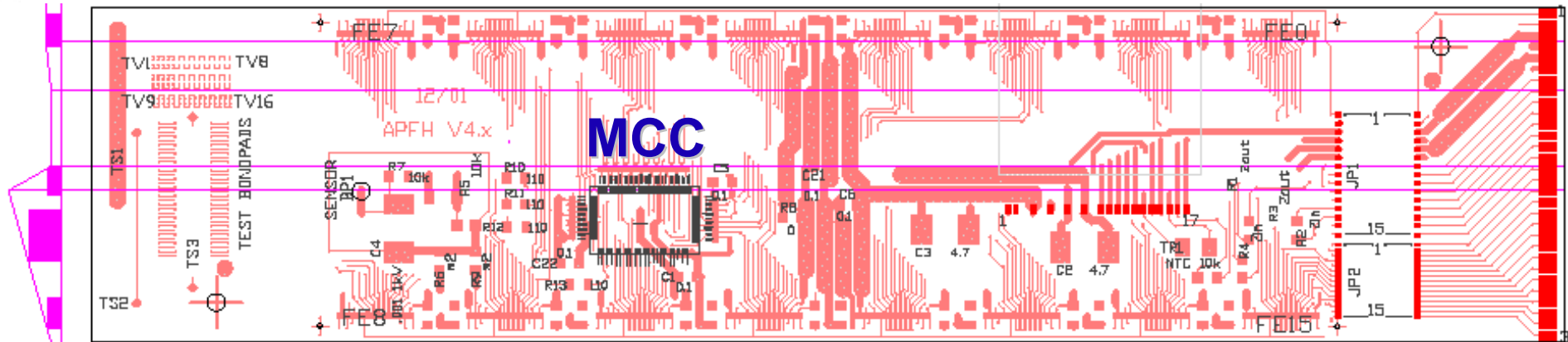




# LEF - Antenna Rules

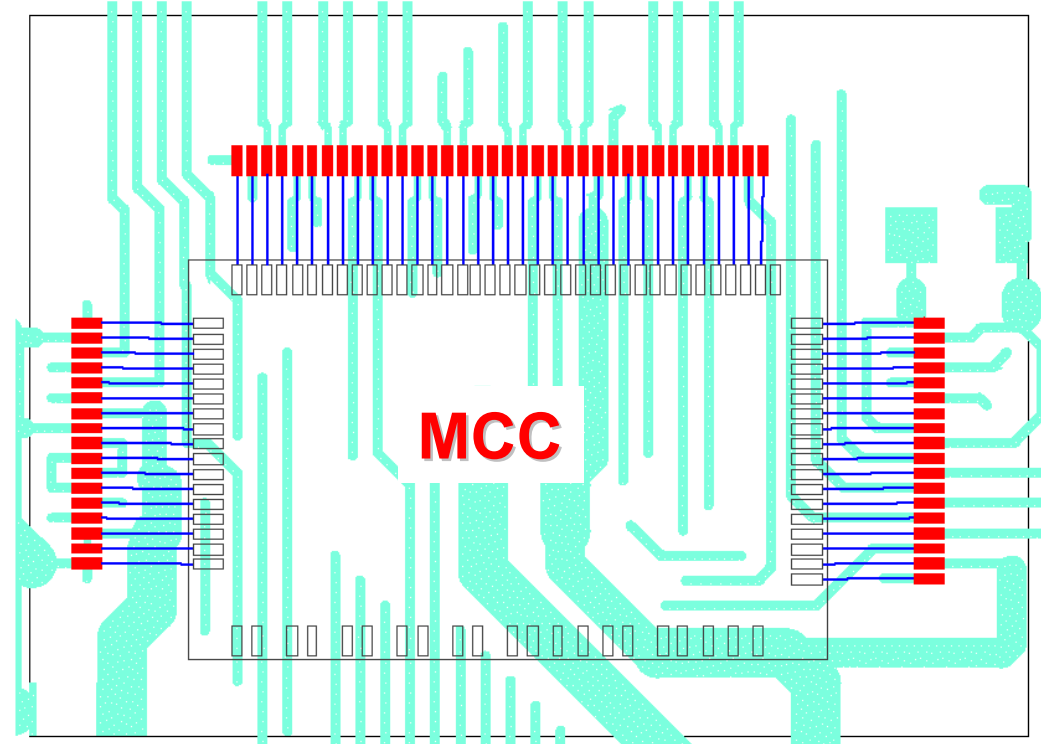
- Default pin antenna parameters: **cmos6sf25TechLib\_5LM2V.lef**
  - ↳ `INPUTPINANTENNASIZE 2.0 ; # antenna area of 2  $\mu\text{m}^2$`
  - ↳ `OUTPUTPINANTENNASIZE -1000000 ; # infinite output sink`
  - ↳ `INOUTPINANTENNASIZE -1000000 ; # infinite inout sink`
  - ↳ `ANTENNAAREAFACOR 0.005 ; # rule 130 - Ratio 200 of antenna`
- Silicon Ensemble environment variables to compute PAE (Process Antenna Effects):
  - ↳ `SET VAR VERIFY.ANTENNA.METHOD "LAYERONLY" ;`
  - ↳ `SET VAR VERIFY.ANTENNA.SUMGATEAREA TRUE ;`
- The value of `INPUTPINANTENNASIZE` we have put is much smaller than the values in the standard cells (All SC's have a gate area of  $3.7 \mu\text{m}^2$  or larger, only the pin D of cell `E_TSPC` has a value of 2.4, but we are not using it). If Silicon Ensemble does not generate antenna violation, also Hercules should not give DRC errors.
- We have seen that with those values WrapRouter is able to repair all violations (antenna and geometry). This important because to correct for antenna violation by hand on the final design can be very heavy.

# Module Envelope -> MCC I/O pads



The module envelope requires that the MCC sits in the lower part of the module (top).

Again, to fit in the envelope only 3 chip sides can be used for wire bonds (right).

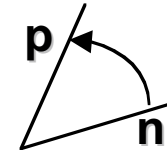




# I/O Pad

- MCC-DSM and MCC-AMS
- MCC-DSM only
- MCC-AMS only
- Test

LVDS Polarity:

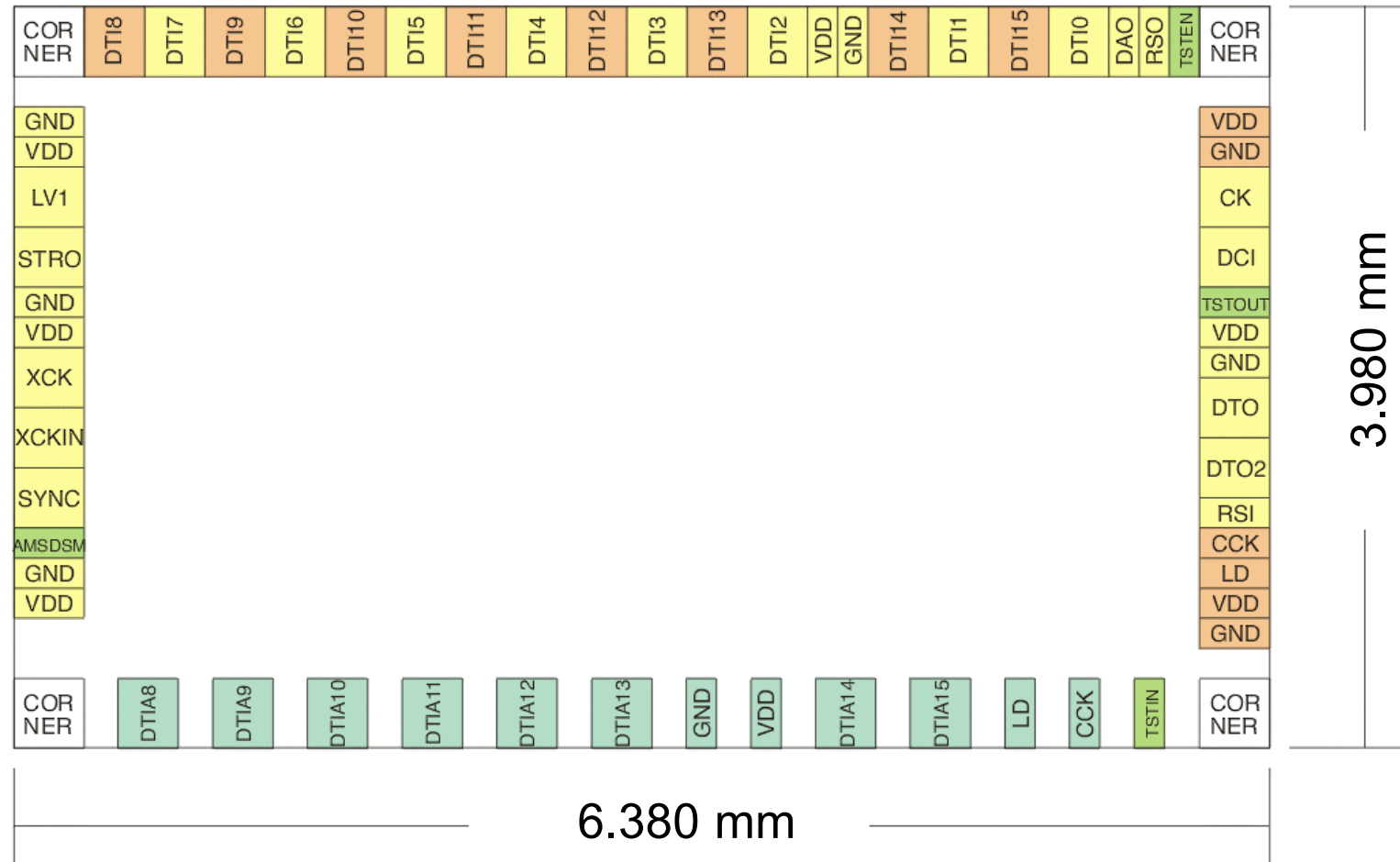


I/O Pad compatibility with older AMS MCC design

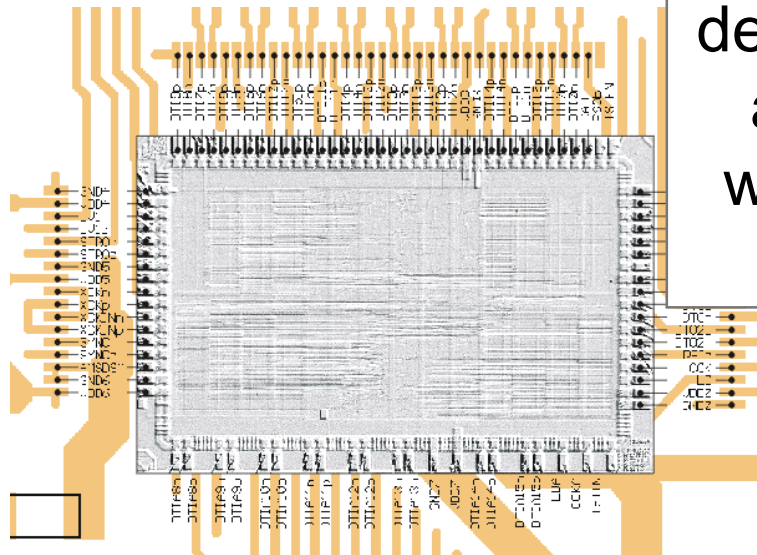
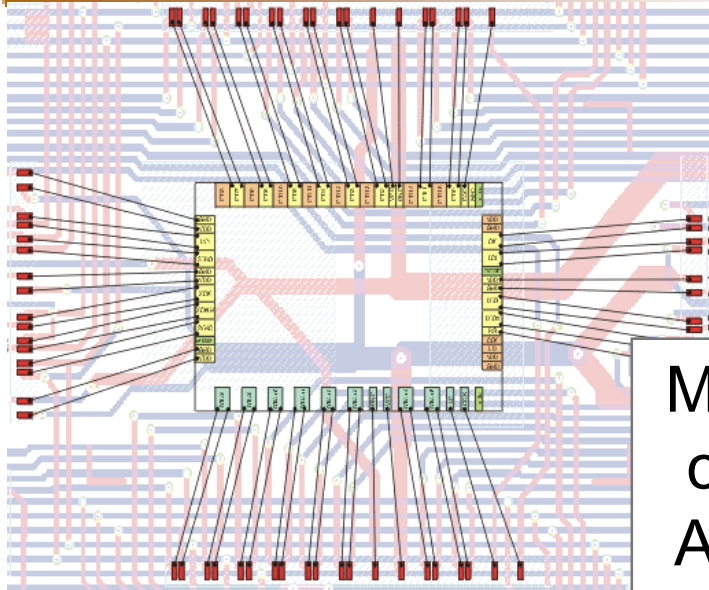
reuse test tools in the standard 84 LDCC package

Only 3 chip sides used for WB to FH

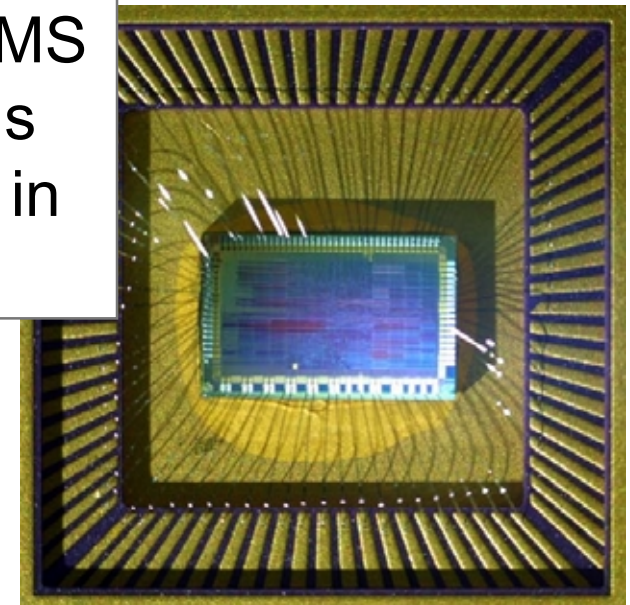
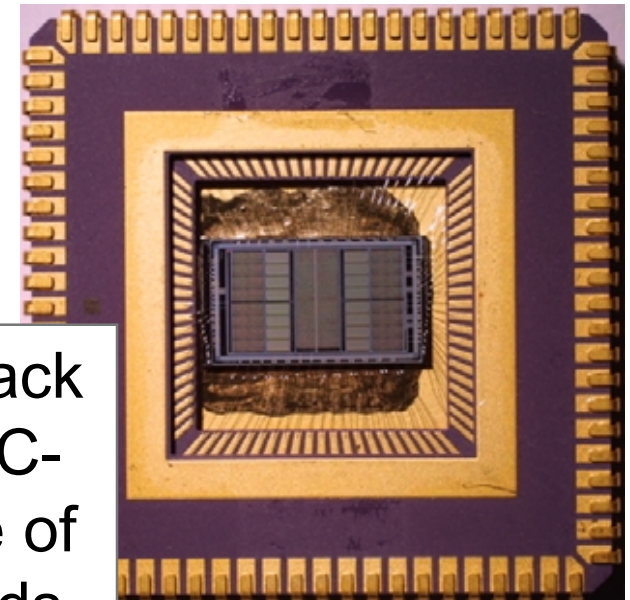
8 VDD/GND pairs:  
7 used in the module



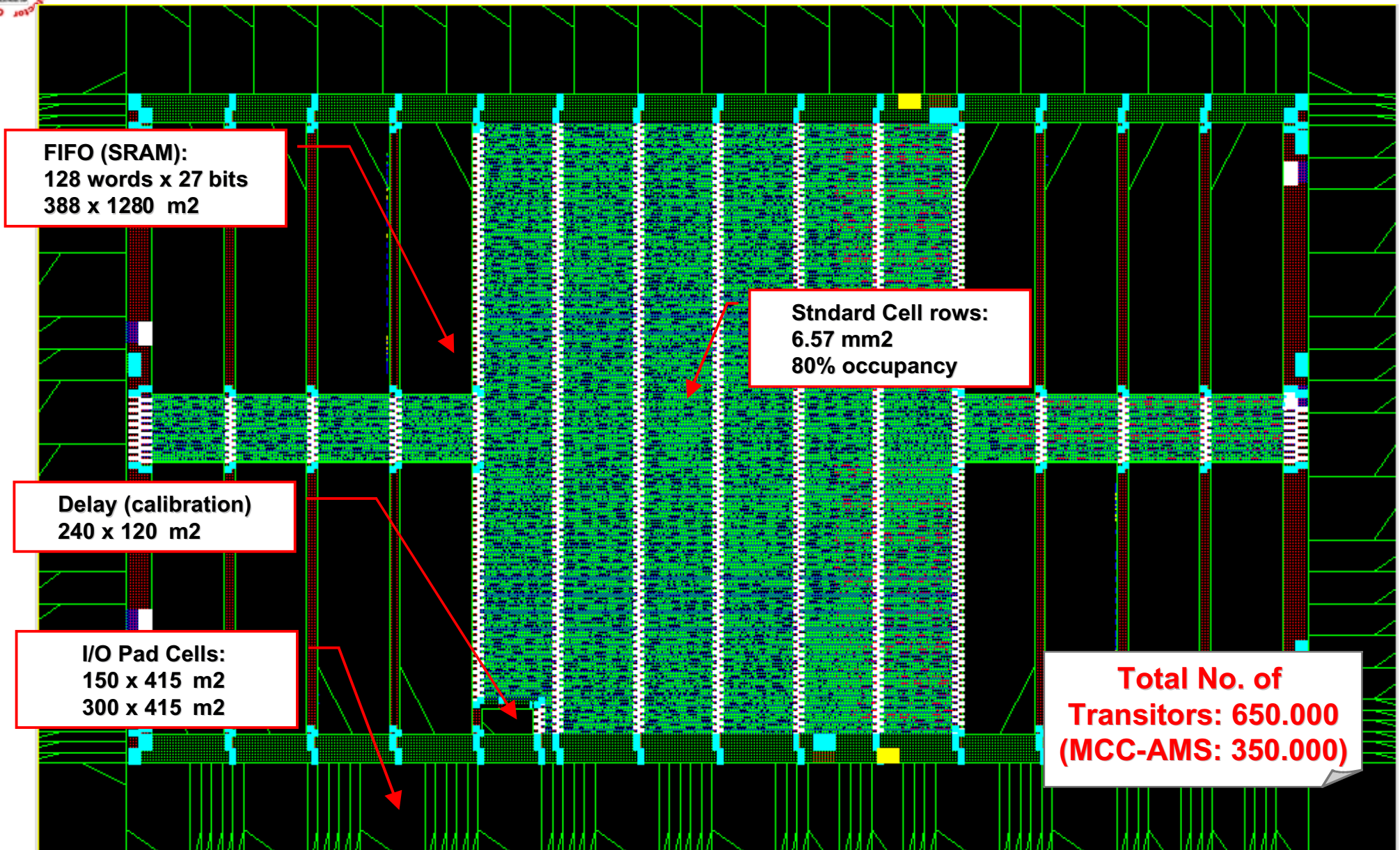
# Pinout: MCC-AMS Compatibility



Making the MCC-I back compatible with MCC-AMS, allows the use of both older flex hybrids designed for MCC-AMS and all the test tools which use the MCC in the package

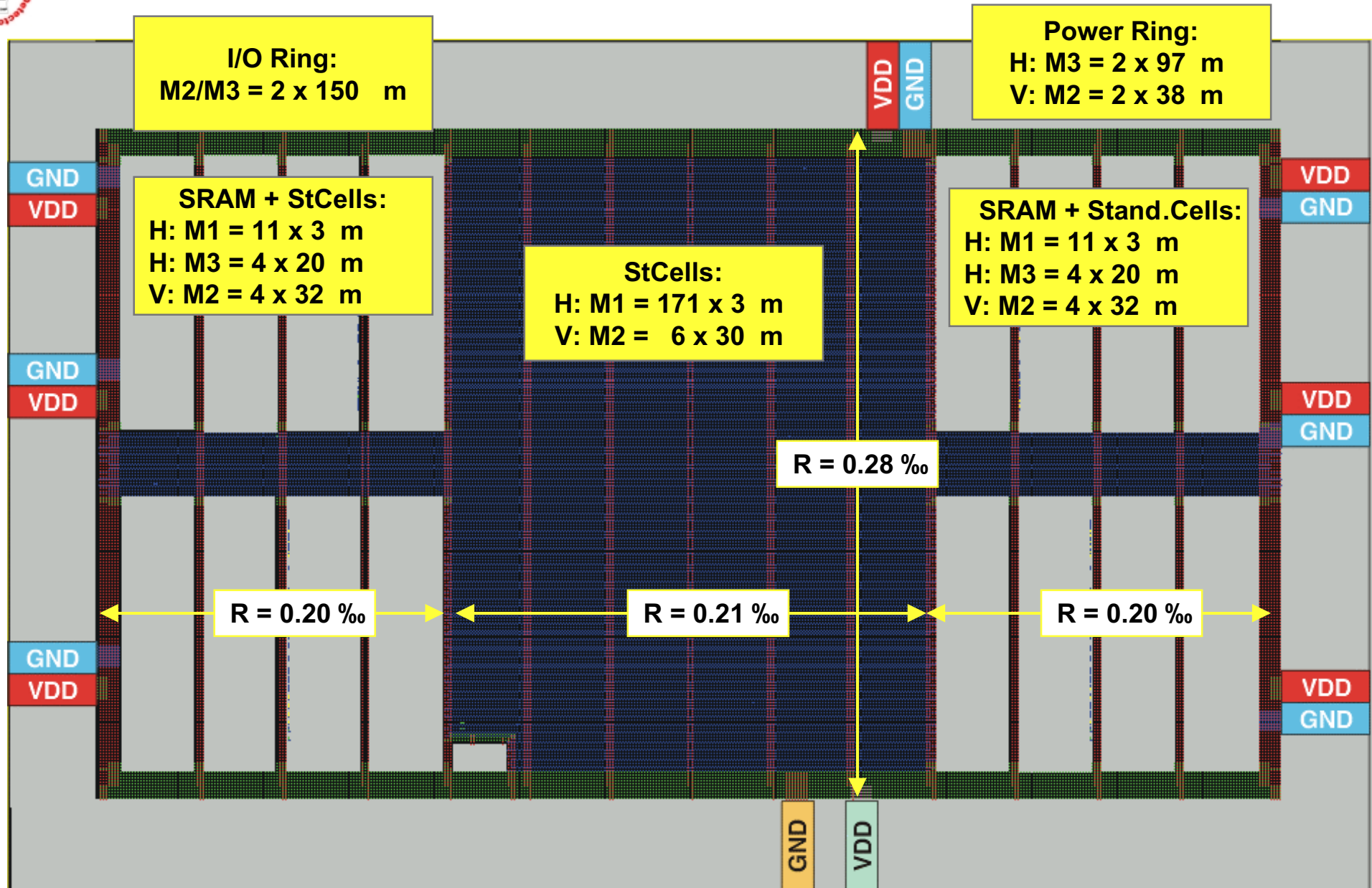


# Layout





# Power Distribution: VDD (GND)

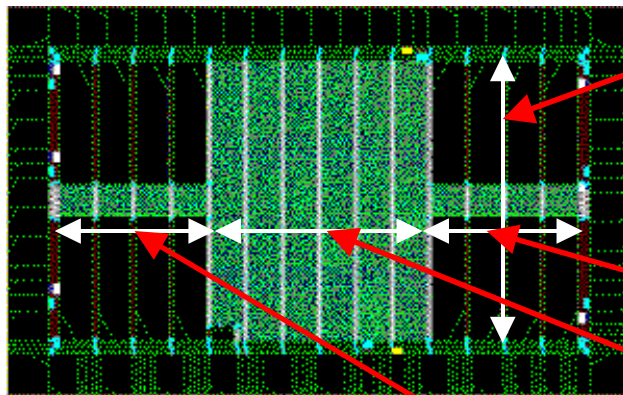


# Power Distribution



Rough estimation using sheet resistance:

- ↳ No Power Mill tool used (lack of time)
- ↳ Total IDD = 100 mA @ 40 MHz → 20 mV drop for 20 mΩ resistance. If better estimation and the 7 VDD/GND pads are considered there are (probably) less than 10 mV disuniformity for the whole chip.



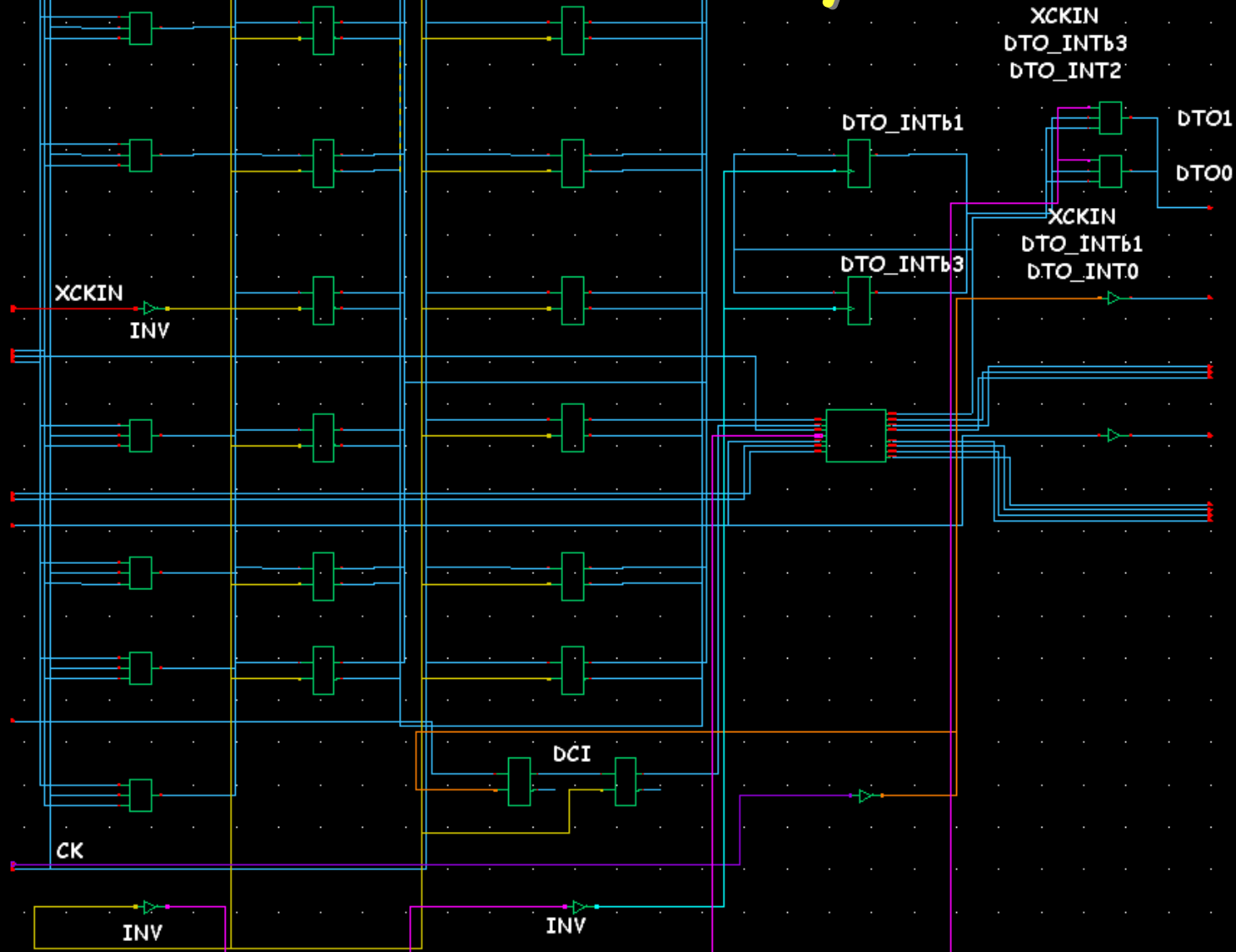
Metal	Width/Trk	Sheet res. (Ω/sq.)	Length 2.90 mm		Note
	(μm)		No. Trk	Resistance	
M2	32	0.078	8	0.88	Block Rings
M2	30	0.078	6	1.26	Stripes
M2	38	0.078	2	2.98	Power rings
M2/M3	150	0.078	2	0.75	IO rings
<b>Total</b>				<b>0.28</b>	

Metal	Width/Trk (μm)	Sheet res. (Ω/sq.)	Left (1.55 mm)		Center (2.20 mm)		Right (1.55 mm)		Note
			No. Trk	Resistance	No. Trk	Resistance	No. Trk	Resistance	
M1	3	0.127	11	5.97	171	0.54	11	5.97	StCell rails
M3	20	0.078	4	1.51	0		4	1.51	FIFO rails
M3	97	0.078	2	0.62	2	0.88	2	0.62	Power rings
M2/M3	150	0.078	2	0.40	2	0.57	2	0.40	IO rings
<b>Total</b>				<b>0.20</b>		<b>0.21</b>		<b>0.20</b>	

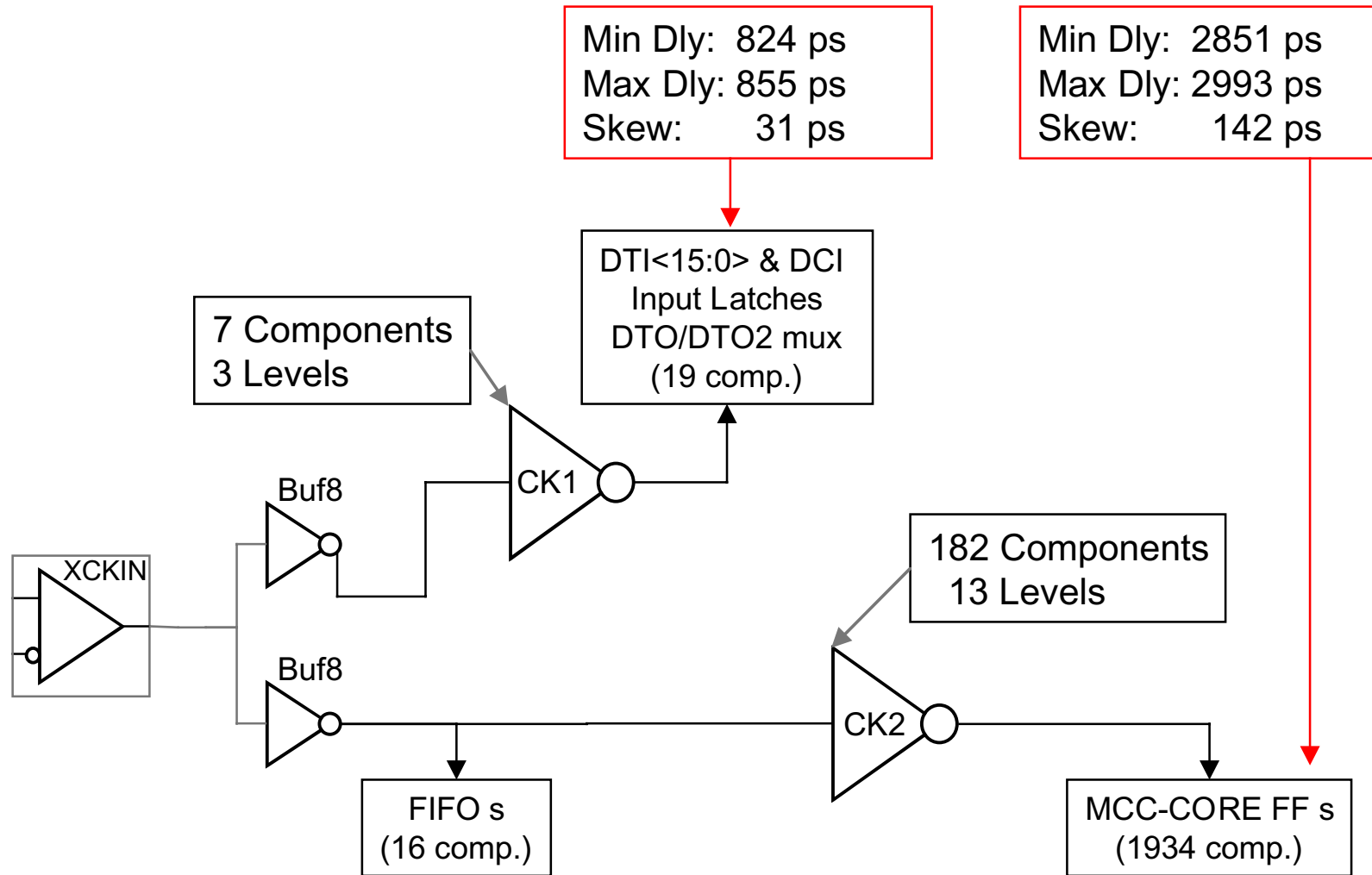
# Clocks

- There are two clocks signals in the MCC: CK and XCKIN. CK is the master clock coming from the off detector electronics. CK is buffered inside the MCC and fanned out as XCK (+ 5 ns delay). XCK is fed back into XCKIN.
- The input signal DCI (coming from off detector) is latched with CK, while all the input signals internal to the module (DTI<15:0>, DTIa<15:8> together with the output of the latched DCI are latched by an early tap of the XCKIN clock (see next slide).
- All the 1934 FF in the MCC are clocked by a clock tree (CK1) with the root being XCKIN.

# Clock & I/O synchronisation



# Clock Tree Synthesis



**Note:** Delays are calculated for worst case by ctgen command (placedCTGenRun).  
Actual routing is only estimated at this level



# Clock Tree: skew - delays

- Clock tree report (max) generated by ctgen, using estimated layout and PP model for interconnect capacitance

Report: **placedCTGenRun**/rpt/final.timing

Design: MCC\_DSM

Clock tree root: Top/XCKINbuf2 Y

Timing start pin: Top/XCKINbuf2 Y

Max. transition time at leaf pins:	0.346 ns
Min. insertion delay to leaf pins:	2.851 ns
Max. insertion delay to leaf pins:	2.993 ns
Max. skew between leaf pins:	0.142 ns

Clock tree root: Top/XCKINbuf1 Y

Timing start pin: Top/XCKINbuf1 Y

Max. transition time at leaf pins:	0.185 ns
Min. insertion delay to leaf pins:	0.824 ns
Max. insertion delay to leaf pins:	0.855 ns
Max. skew between leaf pins:	0.031 ns

- Clock tree report (max) generated by SE tool after routing and using hyper-extract for interconnect capacitance

Report: **routedClockSkewRun**/rpt/routed.timing

Design: MCC\_DSM

Clock tree root: Top/XCKINbuf2 Y

Timing start pin: Top/XCKINbuf2 Y

Max. transition time at leaf pins:	0.341 ns
Min. insertion delay to leaf pins:	2.511 ns
Max. insertion delay to leaf pins:	2.984 ns
Max. skew between leaf pins:	0.473 ns

Clock tree root: Top/XCKINbuf1 Y

Timing start pin: Top/XCKINbuf1 Y

Max. transition time at leaf pins:	0.179 ns
Min. insertion delay to leaf pins:	0.742 ns
Max. insertion delay to leaf pins:	0.778 ns
Max. skew between leaf pins:	0.036 ns

# Clock analysis



- We have compared on a pre-final version of the MCC layout the clock insertion delay, the skew and the transition time at the leaf pins of the clock tree.
- The tool used is the clock analysis of Silicon Ensemble
- The wire interconnect parasitics were extracted in RSPF format using the PP, 2.5 D and the HyperExtract models.
- The two next slides compare the results: the 2.5 D and the HyperExtract model give results that match quite well to each other.

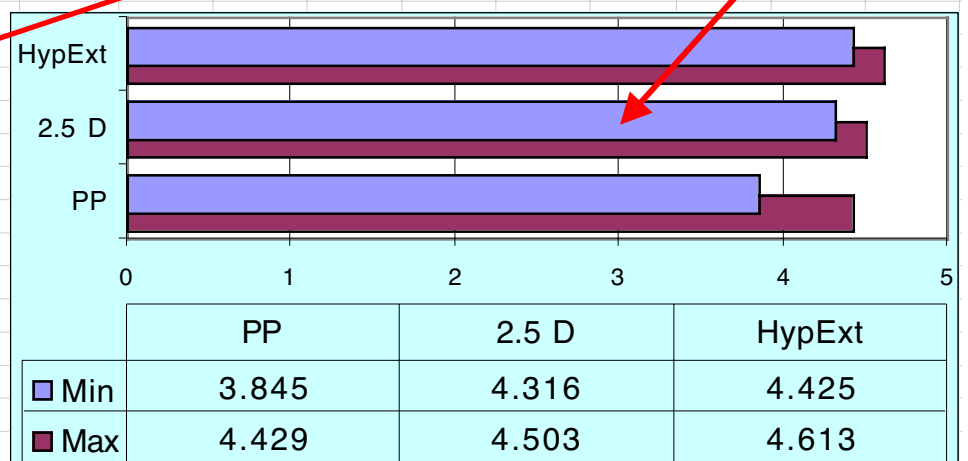
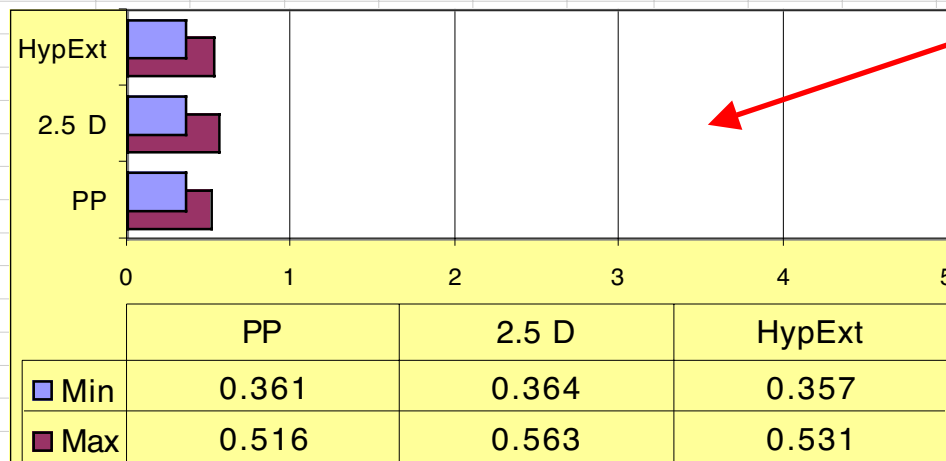
# Clock Tree Analysis: Insertion Delay / Skew

## CK Tree - 1 I/O latches

## CK Tree - 2 All Core FF

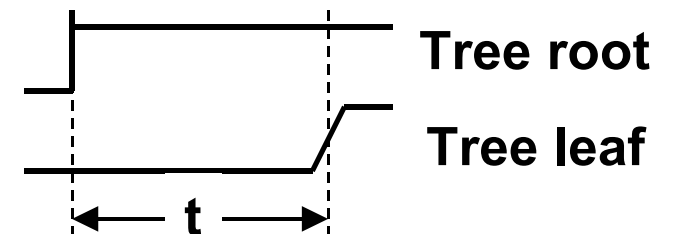
Min./Max. insertion delay to leaf pins									
Model	Best case			Typical			Worst		
	Min	Max	$\Delta$	Min	Max	$\Delta$	Min	Max	$\Delta$
PP	0.046	0.084	0.038	0.152	0.245	0.09	0.400	0.655	0.255
2.5 D	0.048	0.089	0.041	0.154	0.253	0.1	0.403	0.672	0.269
HypExt	0.047	0.084	0.037			0	0.404	0.679	0.275

Min./Max. insertion delay to leaf pins									
Model	Best case (nS)			Typical			Worst		
	Min	Max	$\Delta$	Min	Max	$\Delta$	Min	Max	$\Delta$
PP	0.361	0.516	0.155	1.156	1.446	0.290	3.845	4.429	0.584
2.5 D	0.364	0.563	0.199	1.303	1.493	0.190	4.316	4.503	0.187
HypExt	0.357	0.531	0.174			0	4.425	4.613	0.188



### Note:

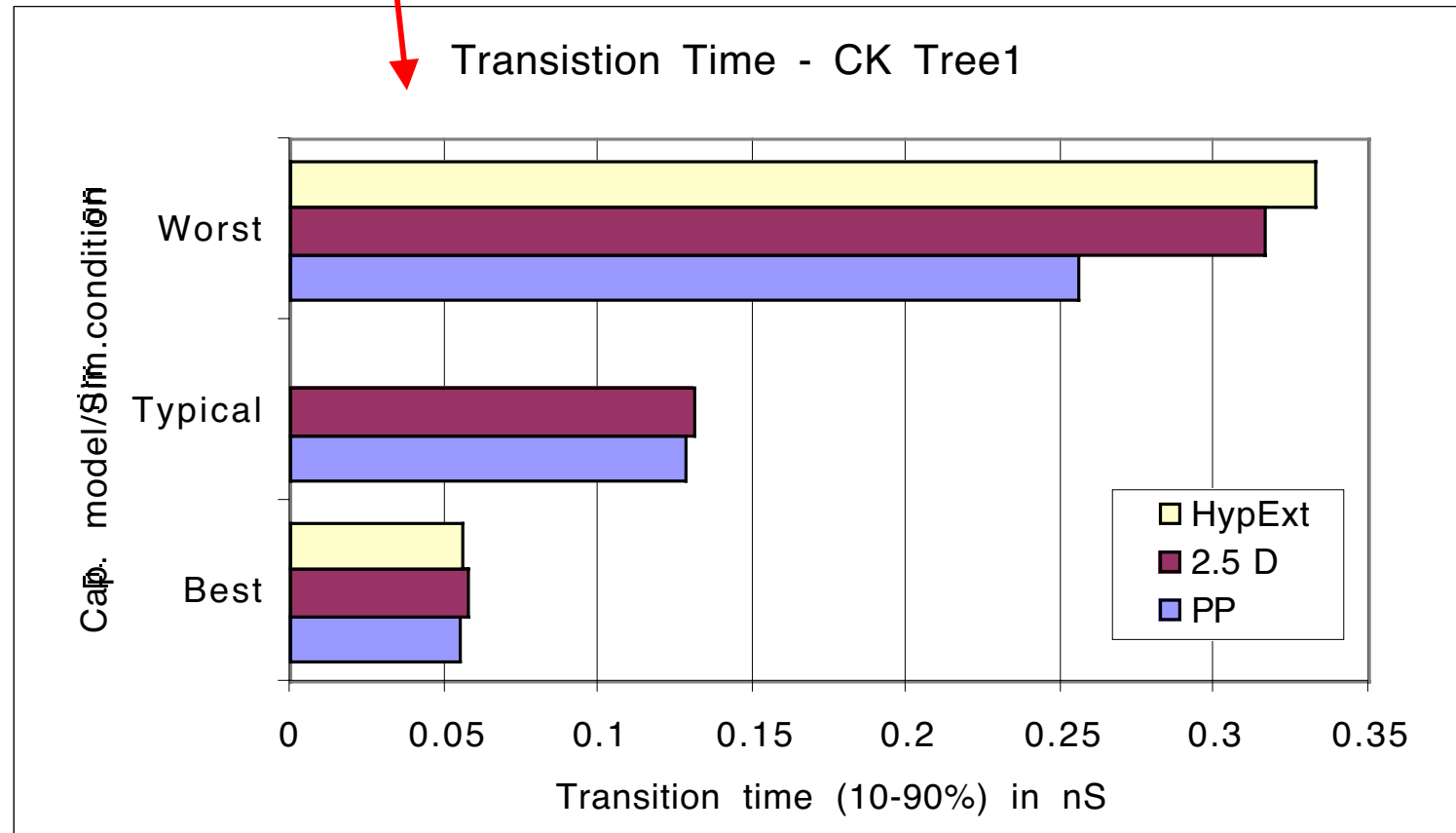
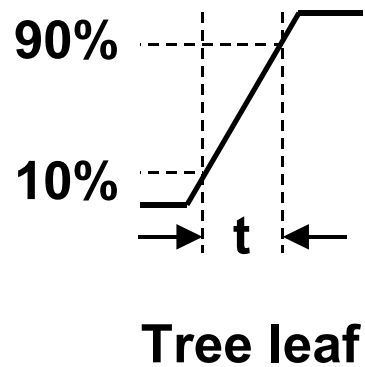
- In the 2.5D the metal distances have been calculated from PC and not from SUB layer.





# Clock Tree Analysis: Transition Time

CK Tree 1				CK Tree 2			
Transition time at leaf pins				Transition time at leaf pins			
Model	Best	Typical	Worst	Model	Best	Typical	Worst
PP	0.055	0.128	0.256	PP	0.063	0.149	0.583
2.5 D	0.058	0.131	0.316	2.5 D	0.066	0.154	0.613
HypExt	0.056	0.128	0.333	HypExt	0.058	0.149	0.638





# Static Timing Analysis

The timing behaviour of the MCC has been checked using static timing analysis by the Pearl tool. The Pearl program uses a netlist extracted from the final routed view of Silicon Ensemble (which includes the complete clock tree). In addition the interconnect parasitics in the RSPF format are extracted using Hyper Extract from the same routed view.

With the static timing analysis we check the maximum slack in setup time (we have used a 15 ns clock period instead of nominal 25 ns). The slack time in max conditions tells the margin of operation at 66 MHz (= 1/15 ns). The result is that the chip can be operated at 80 MHz at 2.5 V in worst case. The margin for 40 MHz nominal clock seems to be enough (test of the chips have demonstrated that they work in excess of 70 MHz after 60 Mrad and at 2.0 V)

The minimum slack time in hold time with min conditions tells that there is a 110 ps margin. In this value is included the clock tree skew. This slack time was obtained from a synthesised design where the hold protection was defined to be 400 ps (with ideal clock)



# Static Timing Analysis: Timing Paths

- Pearl Static Analysis:
- Example of path schematics window.

**Pearl Path Details #8345: Setup Slack 12.62ns**

File Edit View Windows Help

Delay	Delta	Node	Edge	Device	
0.00ns		XCKINp	✓		
2.00ns	2.00ns	DTIn_13_	✓	arrival	
2.00ns	0.00ns	DTIn_13_	✓		
3.00ns	1.00ns	DTI_13_	✓	DTI_pad_13_	in ^ -> out v
3.06ns	0.06ns	DTI_13_	✓		
3.60ns	0.54ns	top/DTI_mux_13_	✓	top/DTImux_13_	A v -> Y v
3.60ns	0.00ns	top/DTI_mux_13_	✓		

Path Schematic | Path Waveforms

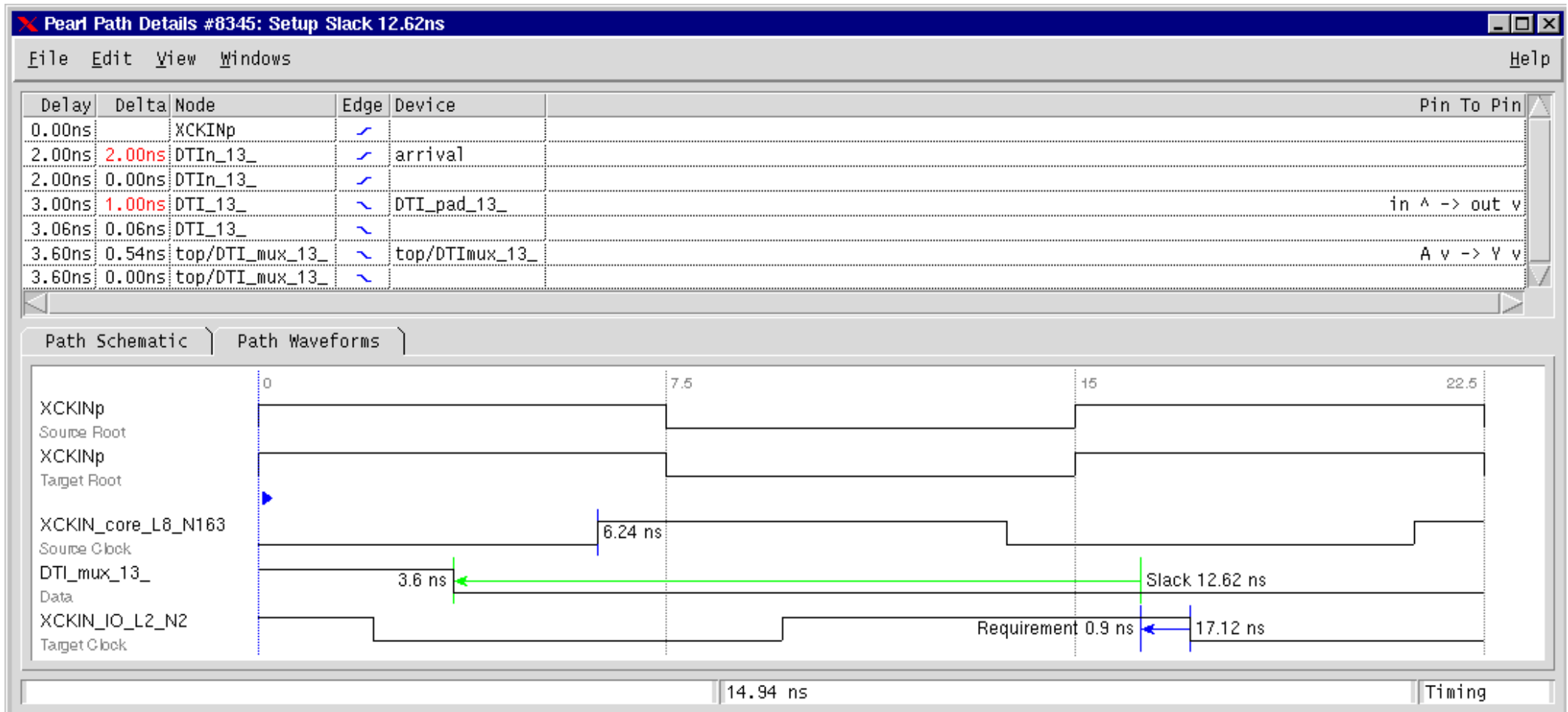
The schematic diagram illustrates the timing path for constraint #8345. It starts at the XCKINp input, passes through an arrival block, then through DTIn\_13\_ (input of MCCpadLVDSr500), DTI\_13\_ (output of MCCpadLVDSr500), DTI\_mux\_13\_ (input of E\_Mux2), and finally DTI\_LD\_13\_ (output of E\_Mux2). The path is labeled with nodes: arrival, DTIn\_13\_, DTI\_pad\_13\_, DTI\_mux\_13\_, and DTI\_LD\_13\_. The path is also labeled with devices: MCCpadLVDSr500 and E\_Mux2. The path is also labeled with signals: XCKINp, DTIn\_13\_, DTI\_13\_, DTI\_mux\_13\_, and XCKIN\_IO\_L2\_N2. The path is also labeled with ports: in, out, A, Y, and D. The path is also labeled with components: LD and DTI\_mux\_13\_.

Constraint At top/DTI\_LD\_13\_ | Timing



# Static Timing Analysis: Timing Paths

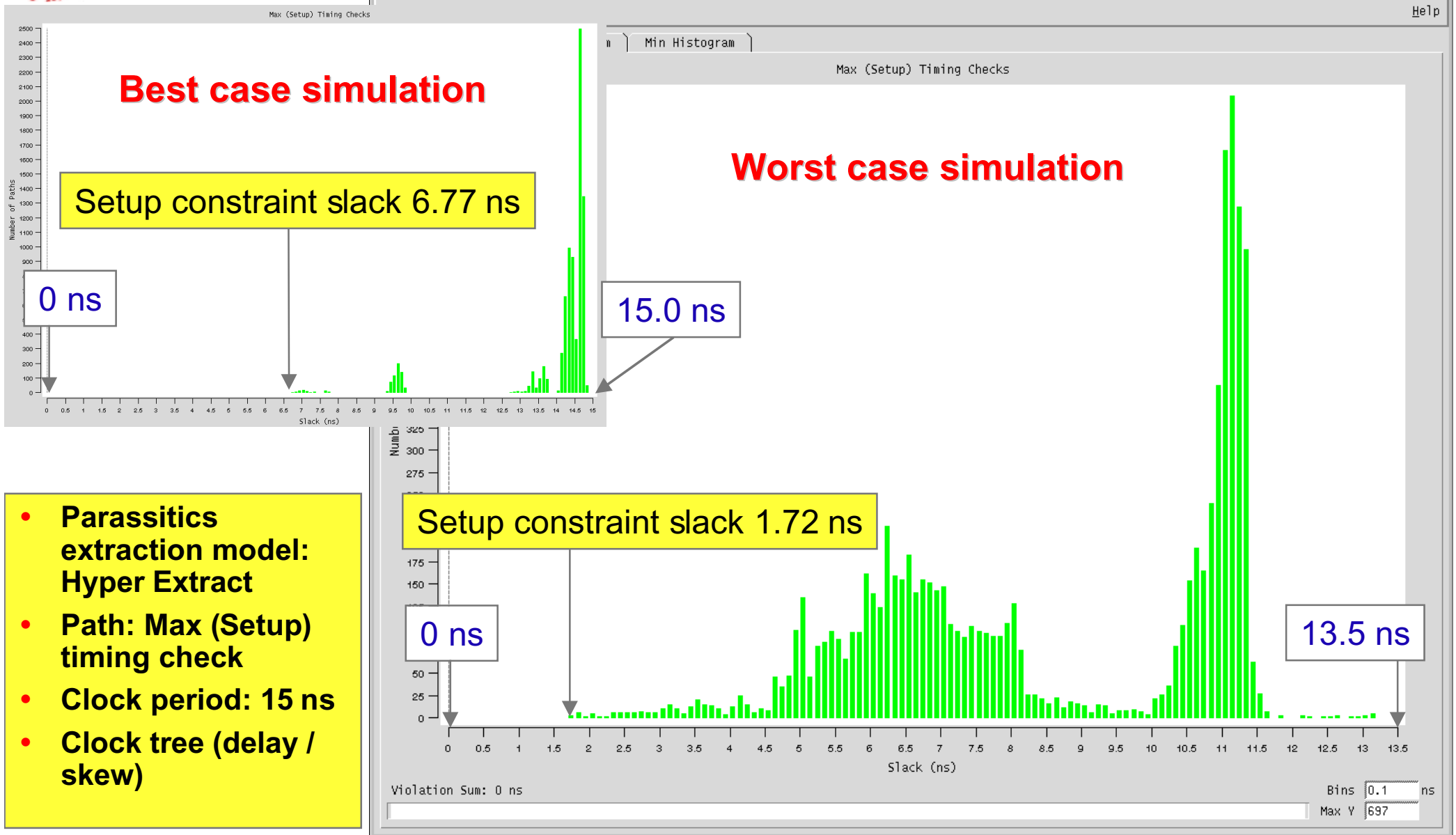
- Pearl Static Analysis:
- Example of path waveform window.





# Pearl: Setup Slack (Min/Max)

Pearl Summary: TimingVerify (16708)



- Parassitics extraction model: Hyper Extract
- Path: Max (Setup) timing check
- Clock period: 15 ns
- Clock tree (delay / skew)



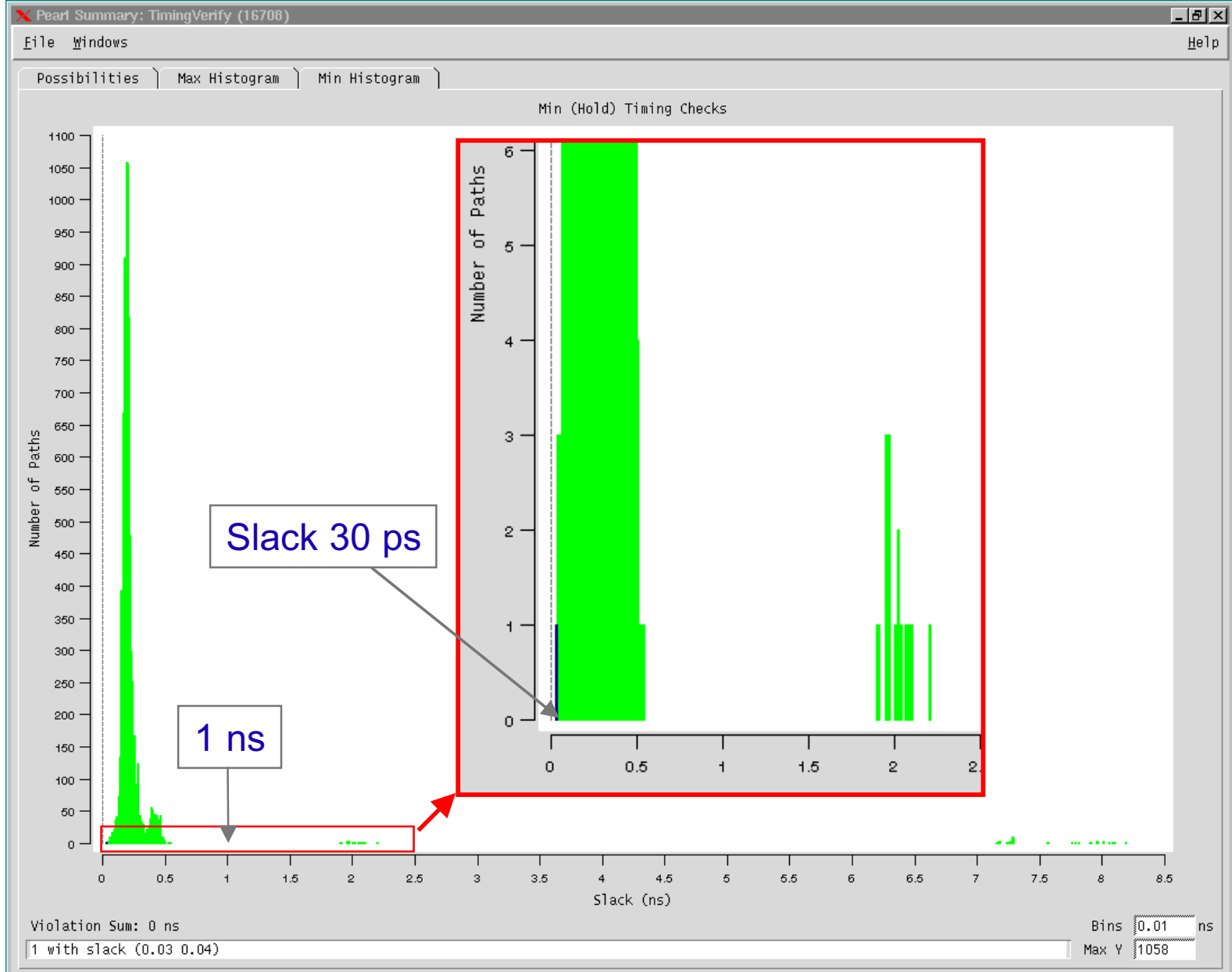
# Pearl: Hold Slack (Min/Max)

Design synthesised with 300 ps hold time protection;

Hold time due to layout and clock skew is critical!

In the final synthesis we used 400 ps hold protection -> slack time on hold = 110 ps.

- Parassitics extraction model: Hyper Extract
- Path: Min (Hold) timing check
- Clock period: 15 ns
- Real clock (skew)





# Static Time Analysis: Results

- Backannotated MCC layout tested by pearl:
  - ↪ Parasitic extraction using PP, 2.5D and HyperExtract give comparable results (last two are more refined models and give more similar results);
  - ↪ Maximum working frequency is about 80 MHz in max conditions;
  - ↪ Clock skew is about 500 ps in max condition and final routing. This is critical for the shortest paths (hold time);
  - ↪ The minimum slack time for the shortest paths in min conditions is 110 ps. A posteriori we have seen that this is not a problem for chip operated between 1.5 to 2.5 V.

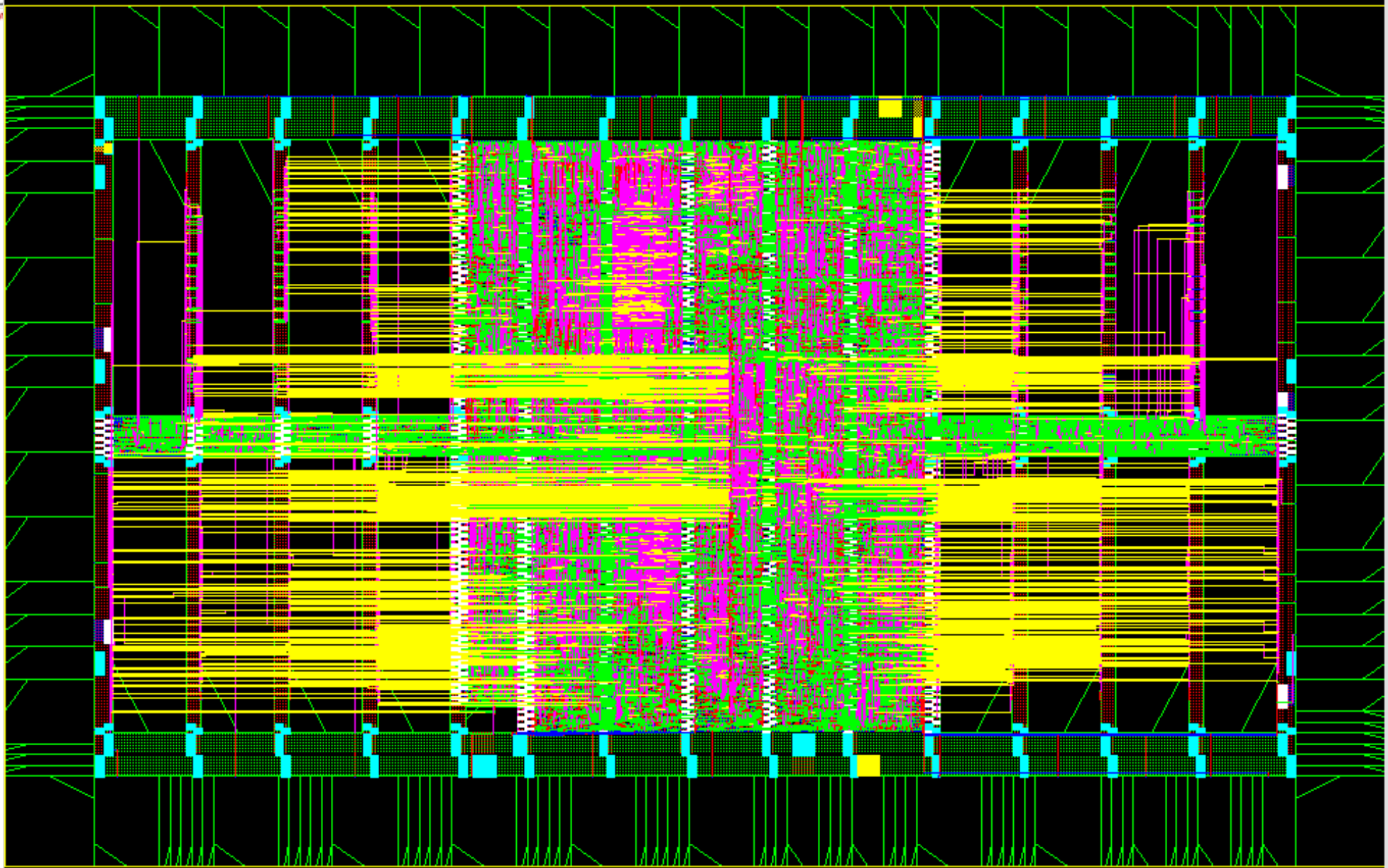


# Comparison on MCC Sizes

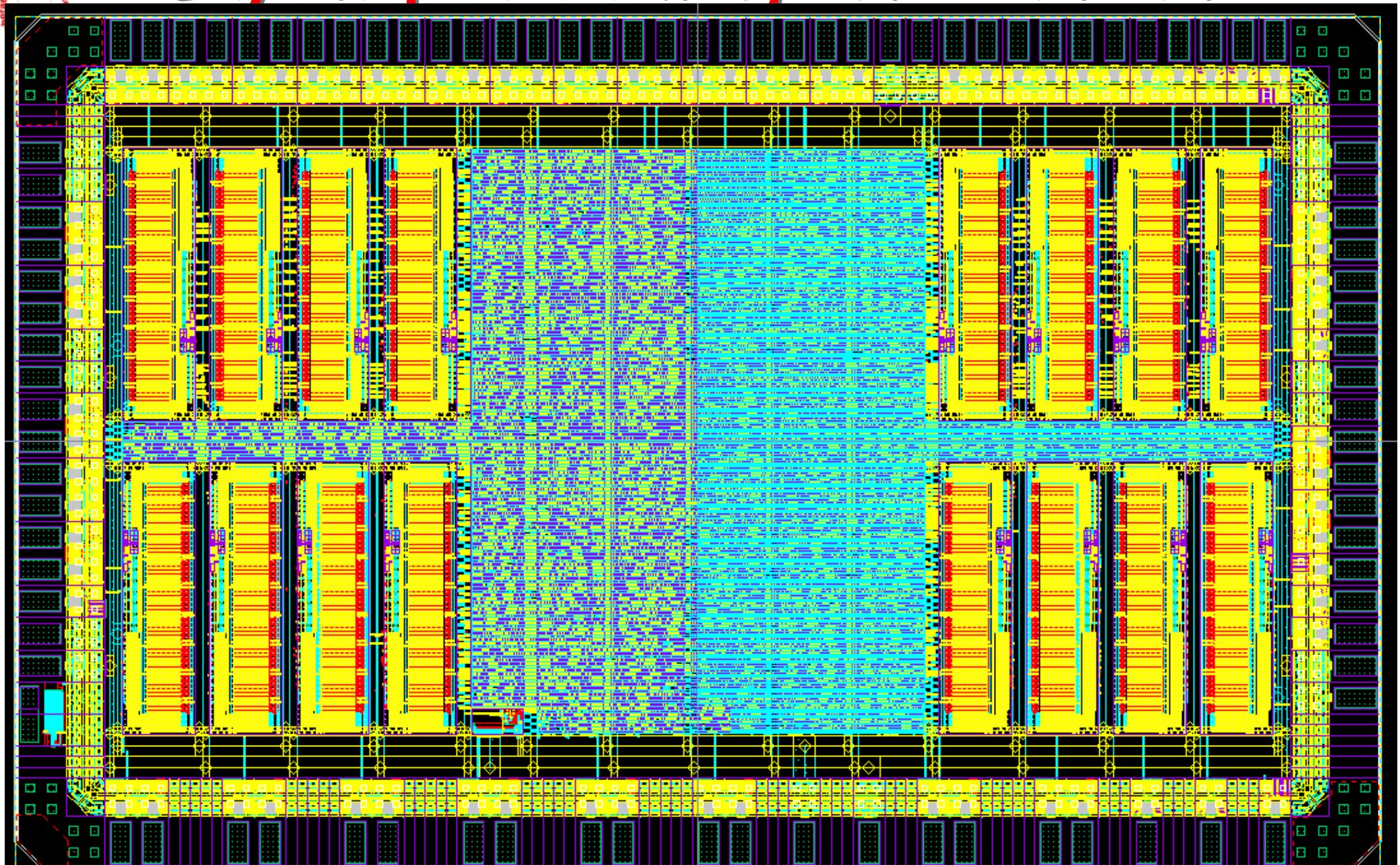
	<b>MCC-DSM</b>	<b>MCC-D2</b>	<b>MCC-AMS</b>
	No. Cell	No. Cell	No. Cell
<b>EVB</b>		5 026	3 145
<b>Receiver</b>		446	701
<b>CMD</b>		572	1 405
<b>REG</b>		574	1 045
<b>Total</b>	<b>33 210</b>	<b>13 446</b>	<b>17 922</b>

- The number of standard cells for the MCC-DSM corresponds to the whole MCC excluded the buffer inserted by the clock-tree synthesis.

# Routing as seen on Silicon Ensemble

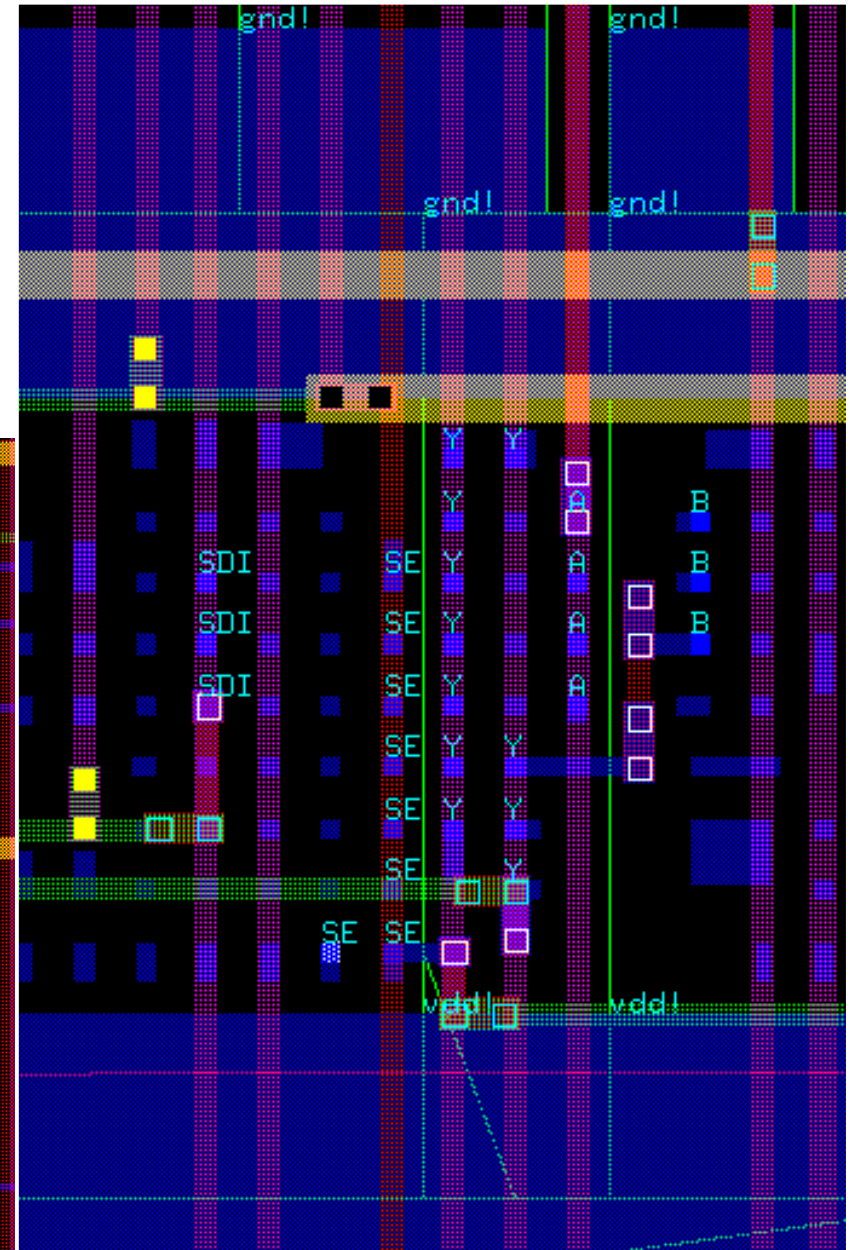
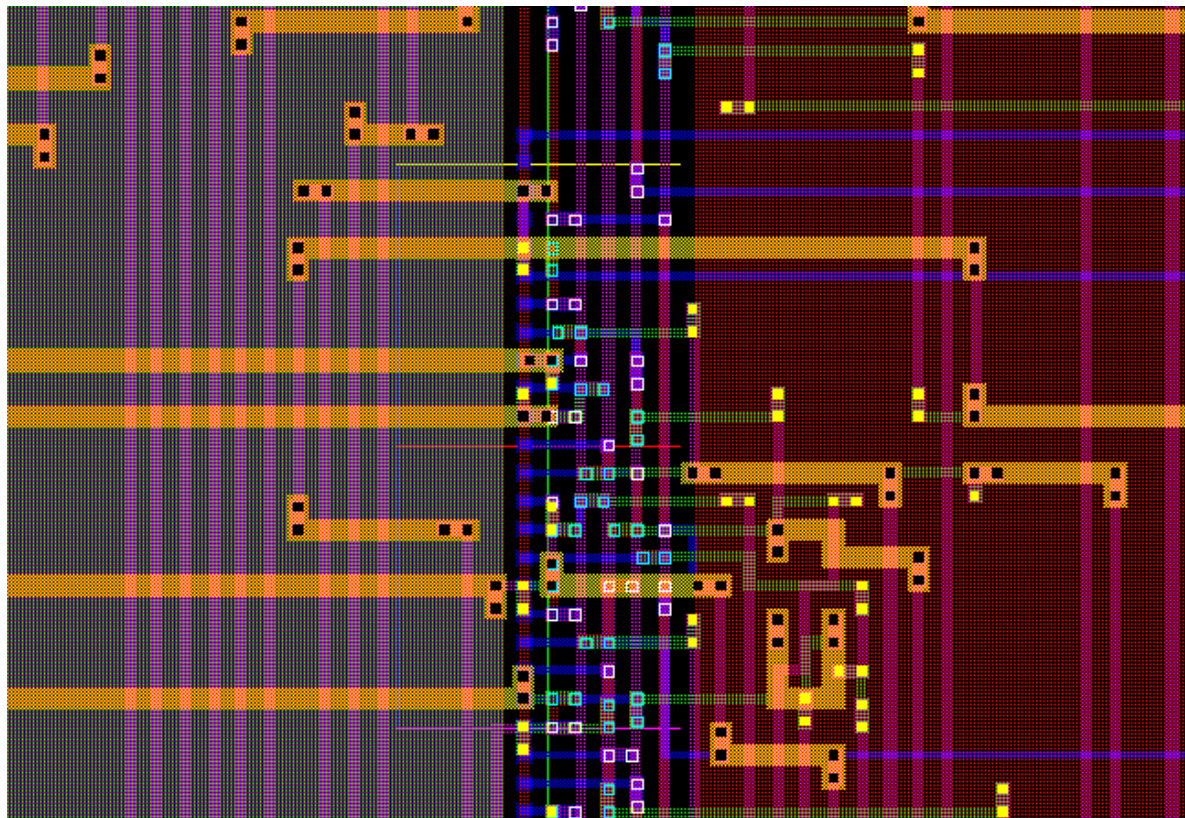


# Layout plot showing RX PC M2 M3



# Time Driven Routing

Examples of routing using the double cut vias defined in the technology LEF file



# Signal Routing



Layer	H-Length ( m)	V-Length ( m)	Down-Via	Violation	Antenna
1st routing	130 342	2 487	0	0	( 0)
2nd routing	6 767	1 126 163	95 804	0	( 0)
3rd routing	1 789 203	207	67 922	0	( 0)
4th routing	145	912 222	28 257	0	( 0)
5th routing	923 650	46	5138	0	( 0)
	<b>2 850 108</b>	<b>2 041 127</b>	<b>197 121</b>	<b>0</b>	<b>( 0)</b>

- Typical execution times of time driven Place & Route tools:

- ↳ QPlace cells: 11 min (CPU)
- ↳ CTGen: 7 min (CPU)
- ↳ WRoute signals: 19 min (CPU)



# LVS

The net-lists match.

LVS executed on flat design.  
The two view: *extracted* and  
*schematics*, match.

See *si.out* report file 

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	660286	627972
total	660286	627972
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	248379	248379
total	248379	248379
	terminals	
un-matched	0	0
matched but		
different type	0	0
total	79	79

End comparison: Oct 29 14:20:28 2001



# DRC (Hercules): errors & waivers

DRC executed on the final MCC design (by Genova running Hercules on a CERN machine) first and on the whole reticle by LBNL. 3 groups of errors: metal filling, SRAM & I/O pads.

- Metal filling: disappear after metal filling at reticle level
  - ↳ `DENSITY allrx {COMMENT = "PDRX: RX + RXFILL Density < 25% or >75%"}`
  - ↳ `DENSITY allm4 {COMMENT = "PDM4: M4 + M4FILL Density < 30% or 70%"}`
- SRAM: already accepted waiver for previous designs.
  - ↳ `INTERNAL ngate {COMMENT = "GR3: Nfet device length on a 45 < 0.280, or GR120a: Gate with 90 bend "}`
  - ↳ `BOOLEAN poss112a AND poss112b {COMMENT = "GR112: PC overlap of RX near RX corner(<0.100) < 0.420"}`
  - ↳ `BOOLEAN PC AND gate_corner_115 {COMMENT = "GR115: PC corner to RX, when gate and RX are on same FET < 0.14 or GR120a: Gate cannot have a 90 bend"}`
  - ↳ `INTERNAL TV {COMMENT = "GR650a: TV width < 14.000 }`
- Bump bonding pad: waiver
  - ↳ `AREA TV {COMMENT = "GR651a: TV area < 550.00`
  - ↳ `INTERNAL opgate_733 {COMMENT = "GR738: OP intersect RX or PC must be rectangular "}`
- Hercules bug:
  - ↳ `BOOLEAN twirebond AND enclosed_m1 {COMMENT = "GR956b: NO M1 enclosed area are allowed under a wirebond"}`