



Overview of MCC design specification updates since FDR

Roberto Beccherle / INFN - Genova

E-mail: Roberto.Beccherle@ge.infn.it

Copy of This Talk:

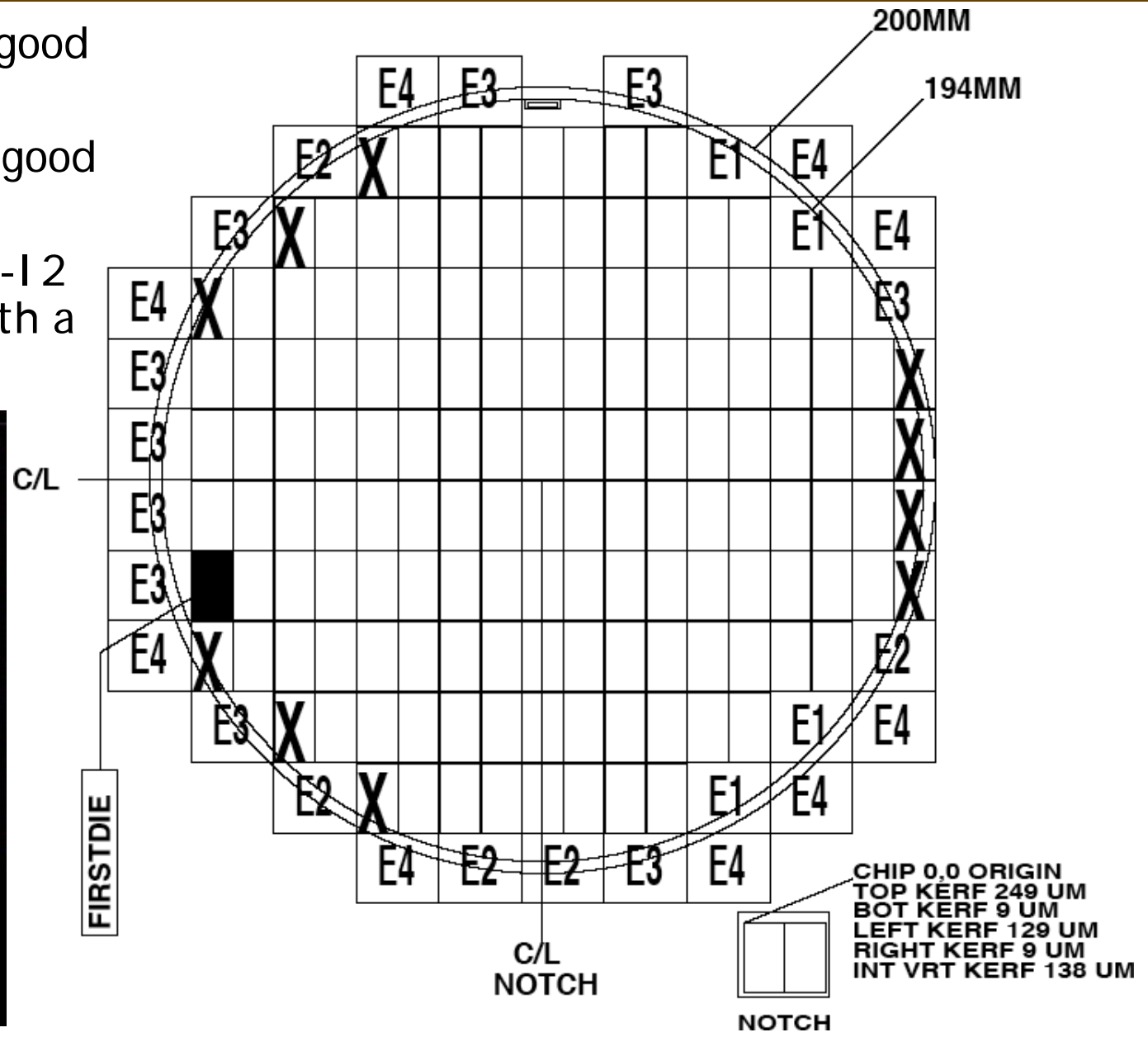
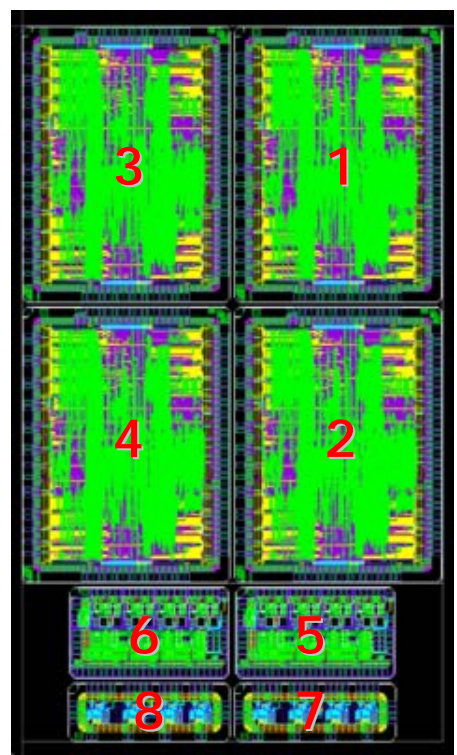
<http://www.ge.infn.it/ATLAS/Electronics/home.html>

MCC-I 2.1: The final ATLAS-Pixel chip

- After last FDR a new and final version of the MCC was submitted to IBM!
- This chip is essentially the same as the MCC-I 1 version with only slight modifications that though have a non negligible impact on the chip size and performance.
- The main reason for making this newer version was to try to address SEU issues that could affect the usability of the MCC in the ATLAS-Pixel detector, and especially in the B-Layer, and improve chip testability.
- Full backward compatibility had to be assured in order to avoid duplication of all test setups in our labs and therefore:
 - ✓ No changes in the architecture were performed.
 - ✓ Some new test features were included, and the existing ones were improved.
 - ✓ Protection against SEU occurrence was implemented where possible.
 - ✓ A new FE-Flag word is generated that allows more information to be sent out.
- Chip testability is greatly improved and mechanism for debugging the EventBuilding process are provided.
- As will be seen by the following talks today the MCC-I 2.1 fully satisfies the ATLAS-Pixel detector requirements and will therefore be used in the experiment.

The SMPW1 Wafer

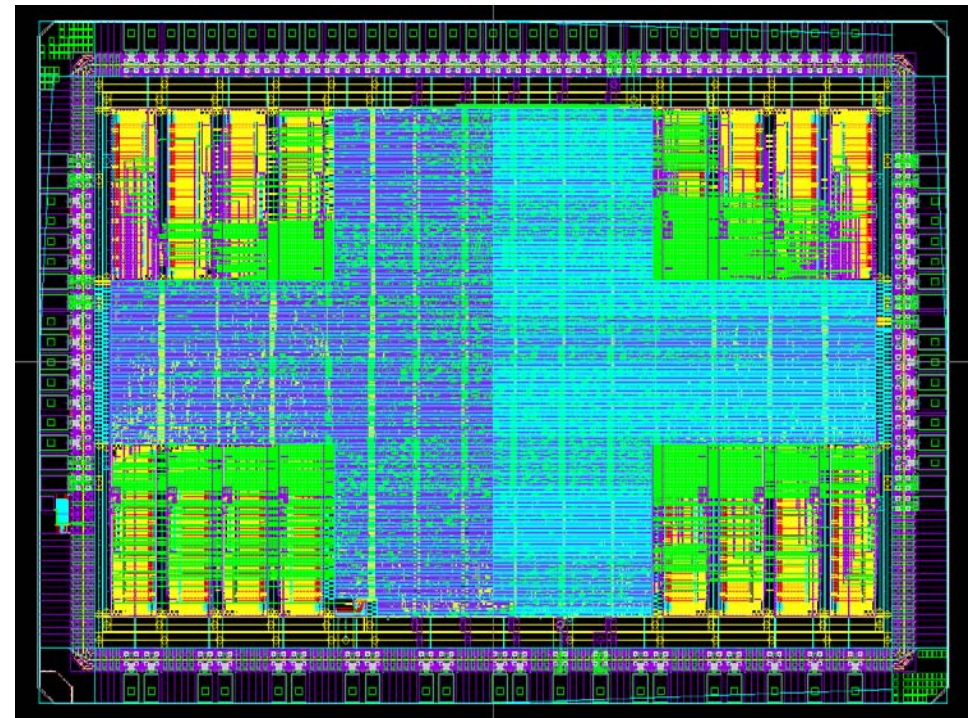
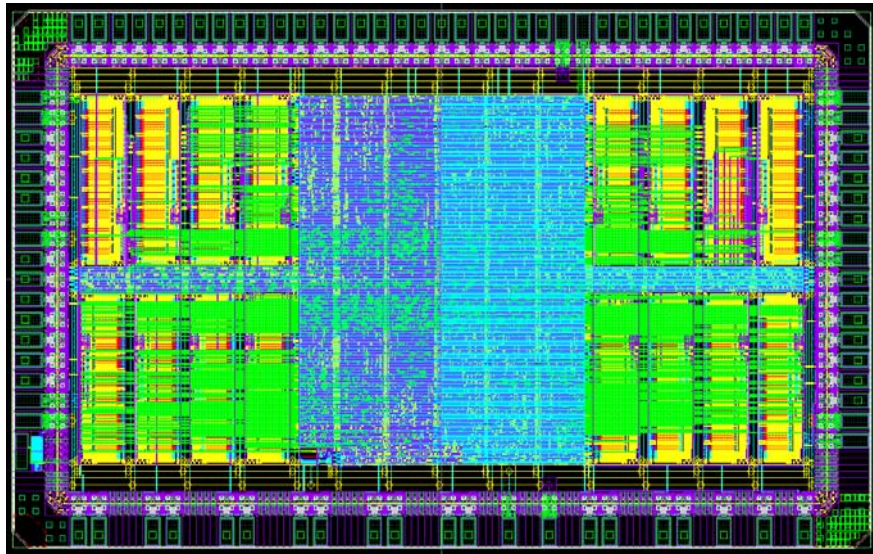
- 134 potentially good reticles/wafer
- 562 potentially good MCC-I 2/wafer
- 2666 good MCC-I 2 for 6 wafers with a yield of 79.1%.



MCC-I 1 vs MCC-I 2

- No. of Std Cells: 33332
- No. of nets: 34368
- No. of Inv1: 18834
- No. of transistors: 660K
- Dimensions: 6380 x 3980 μm^2

- No. of Std Cells: 67919
- No. of nets: 69501
- No. of Inv1: 35130
- No. of transistors: 880K
- Dimensions: 6840 x 5140 μm^2



MCC-I 2: SEU hardening

- A lot of effort has been put inside the MCC-I 2 in order to avoid as much as possible problems due to SEU effects.
Nevertheless not all circuitry could be protected!
- The whole **Command Decoder** has been triplicated with a majority voting circuit on all outputs.
In case of a SEU error the information stored in a dedicated Register.
- All Control bits of the **Register Bank** have been triplicated with a majority logic on the outputs.
In case of a SEU error the information stored in a dedicated Register.
 - ✓ At each clock cycle the value extracted by the majority voting circuit updates the Registers so that increased error protection has been built built-in.
- The **Event Builder Control FSM** has been triplicated with a majority voting circuit on all outputs. All control signals generated by this state machine are therefore protected against SEU.
In case of a SEU error the information stored in a dedicated Register.
 - ✓ No protection could be built-in in the **Scoreboard** and in the **Output Port**.
- All control signals generated by the **Receiver** block and all counters dealing with writing data in the FIFO have been triplicated.
No information is written out in case a SEU occurs.

MCC-I 2: Changes in the FIFO

- The **FIFO** now uses 27 bits, instead of 21, and we used a SEU proof encoding in data written to it so that it is impossible to mix **EoE words** with **Hit words** in case of an SEU occurring anywhere in the FIFO.
- This is done using "0000" as a Hit marker in the FIFO word.
- An EoE word can have different encodings because an EoE word can be with or without a Warning (either from FE or from the Receiver) or with or without a Parity Error in FE data.
- Possible EoE encodings are therefore:
 - ✓ 0111: True EoE word (no Warning and no Parity Error);
 - ✓ 1011: EoE word with no Warning and a Parity Error;
 - ✓ 1101: EoE word with Warning and no Parity Error;
 - ✓ 1110: EoE word with both a Warning and a Parity Error.
- The Event Builder will then recognize any combination of "0000", "1000", "0100", "0010" and "0001" as Hit words.
- All other combinations are detected as EoE words.
- It is still possible to mix different EoE words due to bit flips but this will generate an empty **MCC-Flag** which can easily be corrected by the **ROD**.

MCC-I 2: Changes in the Register Bank

- The CSR register was changed and some new have been added.
- **SBSR**: ScoreBoard Status Register, 16 bit wide, address 1000:
 - ✓ New Read-Only register. Used to read out the status of the ScoreBoard.
 - ✓ Each bit is "1" if the corresponding Receiver has seen at least one EoE.
 - ✓ For disabled Receivers the value read out is "1" (16h1111 at startup).
- **WBITD**: Warning Bit disable, 13 bit wide <12:0>, address 1001:
 - ✓ Allows to disable single Warnings (8 possible from FE and 5 from the MCC).
 - ✓ Eventually the FE-Flag word in the output data is not generated.
- **WRECD**: Warning Receiver Disable, 16 bit wide, address 1010:
 - ✓ Allows to disable selectively Warnings belonging to certain Receivers.
- **CSR**: Its default value is 16h0000 and not implemented bits are read out as "0".
 - ✗ **CSR<15:11>** are EvbSEU, CmdSEU, RegSEU, Lv1I dChkFail and BCI dChkFail. xxxSEU turn on if a SEU in the corresponding block has been detected, the others are consistency checks.
 - ✓ **CSR<10:8>** are WngFast, WngSlow and WngLV1 have the same meaning as before.
 - ✗ **CSR<7>** is EvbDisable and allows to completely disable the EventBuilder.
 - ✓ **CSR<6:5>** are PLBK and OPAT have the same meaning as before.
 - ✗ **CSR<2>** is RecDisable. It allows to decide the meaning of the WRECD register.
If "1" all flags for the selected Receiver are removed from the MCC data stream.
If "0" only Flags selected by WBITD are removed from all Receivers.
 - ✓ **CSR<1:0>** is OM and has the same meaning as before.

MCC-I 2: Changes in the Data Format

- The **No-ToT** mode has been dropped.
 - ✓ The StartUp procedure must be changed as there's no ToT in the CSR anymore.
- **WrFifo** and **RdFifo** commands have now to be 6 bits longer in order to take into account the modified FIFO size.
 - ✓ Compatibility with old hardware/software is kept as long as one leaves a gap of at least 6 bits between old MCC commands.
- The **NULL** word has been removed from the Output Data Format.
- It has been replaced with a new **FE-Flag** word generated by the MCC-I 2.
- The new Flag is: **1_1111_MMMM_MMMM_FFFF_FFFF** where:
 - ✓ **FFFF_FFFF** are the 8 flags produced by the FE-I 2
 - ✓ **MMMM_MMMM** are 8 flags reserved for the MCC, even if only 5 are used by MCC-I 2.
- The old Flag (**1_1110_FFFF_MMMM**) is kept in the format specification but is not used by MCC-I 2.
 - ✓ Compatibility between different generations of MCC is kept but both in hardware and software one must implement the changes in the protocol.
 - ✓ The modified Hardware/Software will still be able to read out modules equipped with MCC-I 1's.
 - ✓ It is possible to build modules using MCC-I 2 with FE-I 2 or FE-I 1.

MCC-12: New Test Features

- Particular emphasis has been put into chip testability, especially at the module level.
- We added the ability to read-out the contents of the ScoreBoard via a RdRegister command.
- There is the ability to completely disable the EventBuilding state machine setting the EVBD bit in the CSR.
- One can put the MCC in PlayBack mode (as before) setting the PLBK bit in the CSR.
- One can simulate data coming from the FE chips using the WrReceiver command (as before).
- One can read out the contents of all ReceiverFifo's (RdFifo command) and of the PendingEventFifo (RdRegister command).
- Combining this features:
 - ✓ Complete debugging of the Eventbuilding process;
 - ✓ No interaction with the FE chips as the Trigger commands are blocked during TestMode and therefore the FE chips do not reply;
 - ✓ One can interrupt EventBuilding, read all relevant information, and resume it without affecting the output data.

Conclusions & Outlook

- All modifications present in the new version of the MCC were presented.
- Special circuitry against SEU occurrences has been embedded in the chip.
- The chip is still not completely SEU proof but its performance under irradiation has been greatly improved and fulfills all requirements.
- The chip is fully compatible with both versions of the IBM FE chips.
- Chip testability, at the module level, has been improved and all new features have been presented.
- The chip area has increased by 38%.
- This is the final version of the MCC for the ATLAS-Pixel project!