



Report of the Production Readiness Review of the pixel front-end chips (FEI & MCC)

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PRODUCTION READINESS REVIEW REPORT

Pixel Front-End Chips (FEI & MCC)

Abstract

The PRR of the Pixel front end chips was held at CERN on December 12th 2003. This document gives the report of the review.

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Distribution: EB Members, Pixel Members, all participants mentioned in the report.

PURPOSE OF THIS REVIEW

The purpose of the review was to give the green light for the production of the ASICs.

MEMBERS OF THE REVIEW COMMITTEE

Review Committee

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For Information

AGENDA & DOCUMENTATION

The agenda and documentation are available at

<http://agenda.cern.ch/age?a035914>

OUTCOMES

General comments:

The review committee was impressed by the quality of the work done. The problems encountered in the previous versions of the chips have been elegantly and efficiently solved. In particular the problem of the threshold dispersion has now disappeared thanks to the thorough analysis of the problem and to a very clever design done at LBL.

The lay-out of the FEI chip has also been proven to be very efficient in maintaining the noise at a very low level even during read-out.

The problem of the clock distribution discovered on FEI version-2 has been fully cured.

FEI

The chip is now at a mature level and no critical point has to be mentioned. The following items should, however, be carefully followed during the testing phase and/or the system installation:

- Temperature dependence is affecting the analogue parameters. The main effect is on the threshold tuning. A procedure should exist to either control the temperature and/or apply analogue parameters tuning during the experiment lifetime (it is likely that the temperature will be stable enough that this is not an issue).
- SEU rate numbers have been measured during the summer test beam, but were not presented at the time of the review. It would be nice to have these numbers presented in a document.
- There is no plan to perform tests of I/O timings according to some specification. It was understood that the only interface is to the MCC chip, and the MCC/FEI system can be seen

as one synchronous machine. There is some flexibility embedded into the design to adapt the timing; anyhow if a timing compatibility problem exists, it will not be discovered before the module testing. A careful examination of the test systems timing versus the chip typical timing should be done to check that there is no possible adverse effect of the test system timing on chips characterization.

- There are some discrepancies between the internal and external charge injection mechanisms. This may be due to some non-linearity in part of the circuitry. Although it is not a show stopper the problem will be studied further.
- The testing of the wafers is done at two sites (LBL and Bonn) with different systems. It is important to make sure that the cuts will be done in the same way. The testing time is about 13 hours per wafer and this should easily allow one to meet the production schedule.

It has been decided to produce 250 wafers. This is assuming a yield of 50%. This number is conservative enough to make sure that enough chips will be available. In addition, the production will be done in 5 batches of 48 wafers delivered every 2 months. The quantity can be adapted depending on the test results.

Given the requirement of extremely high radiation dose, it is proposed to irradiate at least one complete module equipped with FEI chips from the same batch for every production batch.

MCC

It was noted that the chip production and testing is already done (6 wafers). Chips perform on modules as expected. Testing of chips is carefully done. However, the minimum VDD at which the chip fully works has a large spread and some of the chips eventually fail at the VDD target value (2V). The minimum voltage at which the chips operate correctly also increases with irradiation. A binning of chips according to their VDD-low limit should be done. An irradiation campaign to characterize the drift of minimum VDD vs. TID should be done.

The setting of VDD at 2.5 V instead of 2V for modules after some irradiation dose can be accommodated by the pixel system design, in particular in the power supplies system and the cooling system. While this is not expected to provide a problem, the ramifications of operating the pixels at the higher value of VDD should be further explored and documented.

RECOMMENDATIONS

The production of the FEI can go ahead. Some additional irradiation tests of the MCC must be done in order to make sure that there are enough working chips available after the change in VDD with irradiation.