

Minute of the MCC-DSM Design Meeting held on 20th November 2002

(Periodic meeting on MCC project progress)

Present: *Roberto Beccherle, Giovanni Darbo, Guido Gagliardi, Paolo Morettini, Carlo Schiavi.*

1. General information.

This is the first MCC meeting after the submission of MCC-I1. The meeting was devoted to the preparation of the next MCC-I2 submission. Giacomo has been contacted and he agrees to come to Genova for 2-3 weeks before the end of February: He will work on the DRC and on the LVS of the chip. To profit from his work, we must have the final netlist and layout ready before his coming. Kevin asked if we need help from Gerrit, because he wants to know it in advance. We consider that Gerrit will take care of the reticle assembly and metal filling. In addition we expect from LBL the new LVDS current reference.

2. Specification changes and behavioural Verilog.

We have defined and circulated the changes in the design that we want to implement in the MCC-I2. Those changes are:

- The WrFifo (RdFifo) command will expect 27-bit data field (will generate 27 bit output). The same commands were 21-bit long in the MCC-I1. The 6 additional bits will be added in the LSB.
- The scoreboard will be read accessible through a new MCC register. Each bit of this register will be 0 if the corresponding scoreboard is empty or 1 otherwise.
- The NULL field defined in the specifications for the output data stream will be dropped (it was never implemented in the previous MCCs, but it was defined in the specs in case the event builder would not be fast enough in producing data).
- Dropping the FE-flag allows the implementation of a new FE-flag that has 8 bits dedicated to the FE and 8 bits for the MCC itself (instead of 4+4). The old FE-flag will be not implemented in the MCC-I2. In this way MCC-I1 and MCC-I2 output data streams can be univocally decoded independently from their version.

In addition to the former changes, in the specs there are several bugs present in the MCC-I1 version that will be fixed. The additional changes will concern the SEU tolerance improvement and will be transparent to the user. Those changes are:

- Triplication of FEEN and CSR register with majority logic at the output.
- Triplication of the command decoder with majority decision on its output.
- Adding of redundancy bits in the ReceiverFIFOs to reduce the risk of confusion between EoE and Hits.

We are aware that the improvement of SEU tolerance it might not be enough for the operation in the experiment and we possibly ask for a higher rate of ECR issuing.

Roberto is looking at the way of implement the changes.

3. Simulation tools (SimPix / Verilog).

Roberto is trying to run SimPix + VCS (Synopsys Verilog environment) on PC instead of SimPix on PC and VCS on Sun. This should drastically improve the speed of the simulation. To do that it is necessary to modify some routines written by Alessandro Brunengo. Unfortunately some pieces of source code have been lost and must be rewritten (the work needed seems of the order of one or few days). The changes must be done with the help of Alessandro.

Also SimPix needs some small changes:

- The WrFifo / RdFifo commands must be updated in the SimPix script and in the output decoding algorithm.
- The new FE-flag must be recognised by SimPix.
- We also want to implement in SimPix the possibility of overlapping event amongst different FE's.

There were also a discussion on the proposal of dropping the possibility of not having ToT data at the output of the MCC. There might be the risk that in case of saturation of bandwidth in the disk we do not have this handle to reduce the occupancy in the link. For the disk it is planned to have only 1 link at 40 Mb/s per module and, at maximum trigger rate and luminosity, is used at 60% of the bandwidth. Paolo and Kevin should discuss further more.

4. Layout.

Giovanni tried to run the old scripts to generate the layout in Silicon Ensemble from the MCC-I1 netlist. The used version of Silicon Ensemble is now 5.3 (for MCC-I1 was 5.2). The result is that, after the placement of the Fifo and Delay blocks, the pads on the left end side of the MCC are not anymore selectable and if routing is executed a wrong result is obtained. We have reinstalled the old 5.2 version and the result is still wrong. There is a workaround solution (dump the DEF of the design and re-import it again) that seem to work.

5. MCC-I1 tests at DELTA.

3 wafer have been sent to DELTA. At DELTA they have almost setup the testing procedure and they sent us the results they obtained from 2 dice. Functional test works correctly at 40 MHz (5 MHz for the scan chain). There are still a few things to set be setup and then they will proceed wit the complete test.

6. Irradiation analysis

Guido will complete the analysis of dynamic tests. We will discuss with Kostas to see if would be possible to simulate with spice the effect of SEU in the standard cell FF and in the SRAM cell such to compare with measurements. We are considering to write a paper with those results in the next months.