

Minute of the MCC-DSM Design Meeting held on 4th December 2002

(Periodic meeting on MCC project progress)

Present: *Roberto Beccherle, Giovanni Darbo, Paolo Morettini, Carlo Schiavi.*

1. MCC-I2 design.

The interface between SimPix (on Windows) and VCS (Verilog of Synopsys on Linux) works in the direction SimPix → VCS works. There are still problem in the opposite direction. Roberto is still looking at the list of known bugs and changes to be implemented. He hopes to have a first version of the updated netlist the 18th of December.

Paolo will look at the necessary changes in the SimPix script language and in the decoding of the output stream from the MCC.

Carlo will implement the changes in the C++ behavioural MCC-I2 model.

Giovanni did some studies on the MCC clock skew using the MCC-I1 old netlist but with the new version of Silicon Ensemble (5.3). The results are in appendix.1. The clock skew of the routed design is much better in the newly routed design than the one submitted for production (<200 ps now > 400 ps last year). The result is not completely understood because at level of ctGen the estimated delays have not large difference between this and last year, while the routed ones have. The results we obtained on the submitted design are in the talk presented at the MCC-I1 FDR:

http://www.ge.infn.it/ATLAS/Electronics/MCC-DSM/MCC-FDR/08.GD_LayoutTimingVer.pdf

2. MCC-I2 test.

Delta sent back the 3 MCC-I1 tested wafers. The results of the test for the 3 wafers are given in the form of STDF and log files are available on the WEB:

<http://www.ge.infn.it/ATLAS/Electronics/MCC-DSM/Delta/datalogs.zip>

The STDF file have been processed by a demo copy of Galaxy STDF Examiner (www.galaxysemi.com) and histograms and statistics are available on the WEB:

http://www.ge.infn.it/ATLAS/Electronics/home_frames/MCC-DSM_frame.html

3. A.o.B.

We decided that Giovanni will report test results on MCC-I1 and Roberto on the MCC-I2 status at the next Pixel Week of December.

Appendix 1.

Clock tree analysis made on the MCC-I1 netlist, but with the new version of Silicon Ensemble (v.5.3, instead of 5.2 used for chip submission). Clock tree analysis is made using worst case conditions. The main CK tree is Top/XCKINbuf2 which drives 1933 FF. The second CK tree (Top/XCKINbuf1) drives the synchronisation I/O latches.

CK-Tree generated by CTGen

Only clock tree generation and placement of clock buffer are considered in this estimation of the delays. No real routing is made yet.

Report: placedCTGenRun/rpt/final.timing
Design: MCC_DSM

Clock tree root: Top/XCKINbuf2 Y
Timing start pin: Top/XCKINbuf2 Y
Max. transition time at leaf pins: 0.335 ns
Min. insertion delay to leaf pins: 2.501 ns
Max. insertion delay to leaf pins: 2.640 ns
Max. skew between leaf pins: 0.139 ns

Clock tree root: Top/XCKINbuf1 Y
Timing start pin: Top/XCKINbuf1 Y
Max. transition time at leaf pins: 0.197 ns
Min. insertion delay to leaf pins: 1.032 ns
Max. insertion delay to leaf pins: 1.121 ns
Max. skew between leaf pins: 0.089 ns

Clock skew analysis using PP RSPF file

CK tree is generated and only the clock nets have been routed by Wroute. The parasitics are extracted using parallel plate model (PP) and are written in RSPF format.

Report: ckTreeClockSkewRun/rpt/routed.timing
Design: MCC_DSM

Clock tree root: Top/XCKINbuf2 Y
Timing start pin: Top/XCKINbuf2 Y
Max. transition time at leaf pins: 0.289 ns
Min. insertion delay to leaf pins: 2.246 ns
Max. insertion delay to leaf pins: 2.423 ns
Max. skew between leaf pins: 0.177 ns

Clock tree root: Top/XCKINbuf1 Y
Timing start pin: Top/XCKINbuf1 Y
Max. transition time at leaf pins: 0.176 ns
Min. insertion delay to leaf pins: 0.934 ns
Max. insertion delay to leaf pins: 1.056 ns
Max. skew between leaf pins: 0.122 ns

Clock skew analysis using HypeExtract RSPF file

CK tree is generated and only the clock nets have been routed by Wroute. The parasitics are extracted by Hyperextract model and are written RSPF format.

Report: ckTreeClockSkewRun/rpt/routed.timing
Design: MCC_DSM

Clock tree root: Top/XCKINbuf2 Y
Timing start pin: Top/XCKINbuf2 Y
Max. transition time at leaf pins: 0.294 ns
Min. insertion delay to leaf pins: 2.267 ns
Max. insertion delay to leaf pins: 2.431 ns
Max. skew between leaf pins: 0.164 ns

Clock tree root: Top/XCKINbuf1 Y
Timing start pin: Top/XCKINbuf1 Y
Max. transition time at leaf pins: 0.180 ns
Min. insertion delay to leaf pins: 0.938 ns
Max. insertion delay to leaf pins: 1.060 ns
Max. skew between leaf pins: 0.122 ns

Clock skew analysis using HypeExtract RSPF file and completely routed design.

CK tree is generated and all the nets have been routed (together) by Wroute. The parasitics are extracted by Hyperextract model and are written RSPF format.

Report: routedClockSkewRun/rpt/routed.timing
Design: MCC_DSM

Clock tree root: Top/XCKINbuf2 Y
Timing start pin: Top/XCKINbuf2 Y
Max. transition time at leaf pins: 0.300 ns
Min. insertion delay to leaf pins: 2.384 ns
Max. insertion delay to leaf pins: 2.487 ns
Max. skew between leaf pins: 0.103 ns

Clock tree root: Top/XCKINbuf1 Y
Timing start pin: Top/XCKINbuf1 Y
Max. transition time at leaf pins: 0.198 ns
Min. insertion delay to leaf pins: 0.958 ns
Max. insertion delay to leaf pins: 1.061 ns
Max. skew between leaf pins: 0.104 ns