

Minute of the MCC-DSM Design Meeting held on 18th December 2002

(Periodic meeting on MCC project progress)

Present: *Roberto Beccherle, Giovanni Darbo, Guido Gagliardi, Paolo Morettini, Carlo Schiavi.*

1. MCC-I2.

Interface between SimPix and VCS still has problem. It works at 40x1 Mb/s but not with the other DTO/DTO2 transmission speeds. Roberto claims that the problem should be easy to fix. No more advancement on the update of the netlist with the changes for the MCC-I2.

Decision on specs:

- We have decided that the no ToT mode will be dropped in the MCC-I2. The no ToT mode was a historical decision taken when only 40 Mb/s mode were available in the MCC-AMS and we were worried that not enough bandwidth were available.
- There was a request of an output mode that could generate an indefinite number of 1's on DTO/DTO2 to allow a faster annealing of VCSELs. Roberto will look at a possible solution.

The other specs agreed with are listed in the appendix.

MCC-I2 SimPix model (Carlo), SimPix script and SimPix program (Paolo) will be updated to simulate the new design according to spec changes of appendix.

Giacomo will be available to come to Genova before the end of February.

There is some concern on the schedule for the chip submission, we still have some margin, but usually each step requires more time than foreseen.

2. Irradiation analysis and new irradiation.

We discussed with Kostas and Federico Faccio about the analysis carried on by Guido on the MCC-I1 irradiated last summer and to compare the results with the APV25 chip of CMS. Guido will write an ATLAS note with our measurements. A limited effort will be tried to match the results we have at 1.8 and 2.2 V of VDD by simulating injected charge in the Spice models of the SRAM and of the FF memory cells. Kostas is interested in doing such simulation in January. We will decide if we will make a paper for Nucl. Instr. and Meth. after the ATLAS note.

Next year we will have two periods of irradiation that will involve the MCC-I2 (one in July with the Module and one in October with the MCC-I2 stand alone). The Module irradiation will use the TPLL/TPCC. It would be possible to do system studies of SEU by digital injection on known pixels and study the results coming out. To do that the TPLL must be operated in raw mode. Paolo will look at the possibilities and we will discuss and take some decision at the February Pixel Week. In October we will use the MCCex with the usual ancillary boards. In this case we will concentrate on effect of SEU on the event building by using simulated events in WrReceiver mode. It is probably less efficient than using the Module, but it will add some more information. Guido will give priority at the Hardware / Software setup for the 2003 irradiation campaign, starting from the end of January.

Appendix: Specification changes from MCC-I1 to MCC-I2

- Output data format

The NULL field will be dropped. This allows a new FE-FLAG word to be added to the data format. This new flag will be identified by the <11111> header. This new flag will be 21-bit long. The proposed format of the flag is:

1_1111_FFFF_FFFF_MMMM_MMMM.

This flag will be the only FE-FLAG implemented in the MCC-I2. It allows 8-bits reserved for the FE chip plus 8 for the MCC itself. The old FE-FLAG (1_1110_FFFF_MMMM) will be kept for compatibility with MCC-I1.

Implications:

Hardware (ROD, TPLL) and Software (TurboDAQ, SimPix, DAQ-1, etc...) will have to implement the modifications of the protocol. Backward compatibility with MCC-I1 equipped modules, even if we decide to use these chips in part of the final experiment, will be ensured by the fact that MCC-I1 will never produce a NULL word.

- Drop of NoToT mode

The MCC-I2 will not have the ability to drop the ToT information from the Data.

The bit of the CSR which sets the ToT mode will be dropped.

Implications:

Hardware (ROD, TPLL) and Software (TurboDAQ, SimPix, DAQ-1, etc...) will still need to be able to decode the No-ToT case of the Output Data Format in order to be able to operate with MCC-I1 equipped modules. One has to add the new flag decoding instead of the NULL word decoding.

Software (TurboDAQ, SimPix, DAQ-1, etc...) will have to change the start-up sequence for MCC-I2's as there is no ToT bit in the CSR register.

- WrFifo / RdFifo

The data field of this command will be 27 bits instead of 21 bits. New bits will be added in the LSB part of the word so that there is backward compatibility. For modules with MCC-I1's one simply has to insure that the 6 LSB of the WrFifo command are set to 0.

Implications:

Hardware (ROD, TPLL) does not require any change.

Software (TurboDAQ, SimPix, DAQ-1, etc...) will have to implement these modifications. The new format is the only one to be implemented as it is automatically compatible with both formats.

- Add Scoreboard register

A new address will be added to the existing ones. This register is a Read Only register!

Implications:

Hardware (ROD, TPLL) does not require any change.

Software (TurboDAQ, SimPix, DAQ-1, etc...) will have to implement these modifications.