

Minute of the MCC-DSM Design Meeting held on 16th of January 2003

(Periodic meeting on MCC project progress)

Present: Roberto Beccherle, Giovanni Darbo, Guido Gagliardi, Paolo Morettini, Carlo Schiavi.

1. MCC-I2.

Analysis of MCC-I1 known bugs: Roberto has completed the analysis and is now in the phase of their correction to release soon rev.1 of his MCC-I1 code (see minutes of 9/1/03). There are two claims of misbehaviour of the MCC-I1:

- Increment of L1 counter by two (in case of BCR?) instead than by one. This claim is from John Richardson. Roberto tried to reproduce it, but he think it might be to the not correct distribution of the reset to all the MCC internal blocks. It was also not very clear what exactly was the problem. Roberto will ask John for clarification.
- EoE overflow. Paolo and Roberto, during the test beam run of last year, saw cases where EoE overflow flag appeared in the data. This should never happen in the case of correct behaviour of FE's and MCC. Is it a problem in the module, TPLL or is it misbehaviour of the MCC? We should try to reproduce it in the lab.

Command sequence in system operation: We found that some sequences of commands used in system operation are weak. The solution will be both in design changes in the chip and in the specification of the correct sequence at level of TPLL/ROD software. The step between configuration and run mode must be treated carefully. In particular:

- *Configuration → run mode:* When MCC goes to run mode the system must make sure that the MCC starts from a clean data path status. This can be done issuing an ECR before setting MCC in run mode. Also the FE's must be "quiet" before receiving the LV1 signal, otherwise, when the MCC goes to run mode, it starts seeing hits from previous events and it creates corrupted events.
- *Run → configuration mode:* when a slow command is issued, while the MCC is in run mode, it is possible to spy MCC internal registers, ReceiverFifo and PendingLv1Fifo, but the MCC should not resume the run mode without previously resetting the data path (ECR).

Note: The signals from the FE's to the MCC Receivers are active only if the MCC is in run mode and not in play back mode (for the current MCC-I1 chip the play back mode did not block the input from the FE's).

SimPix and MCC verification: Carlo is running the old scripts on the MCC-I1 verilog behavioural of and he is adding new scripts for detecting the unseen bugs of the submitted MCC-I1 chip. He will put the information on a WEB page and he will keep it updated periodically. This page is:

<http://www.ge.infn.it/ATLAS/Electronics/home.html>

Paolo will make a CVS depository to use for the different internal releases of the MCC verilog code.

Schedule: We have defined the task and milestones. Each one contributing to the design will fill with the estimated time to complete his task. Next week we will discuss the obtained plan and we will release the schedule. At each weekly meeting we will check the advancement of the design.

2. Irradiation analysis and new irradiation.

Guido has written a preliminary draft with the results of the MCC irradiation with the aim of getting an ATLAS note. He will fill the missing parts and then he will contact Kostas to make a simulation of the standard cell flip-flop and of the SRAM memory cell to see if this can explain the SEU cross-section ratio we have obtained from the chips operated at 1.8 and 2.2 V.