

# Minute of the MCC-DSM Design Meeting held on 5<sup>th</sup> of February 2003

(Periodic meeting on MCC project progress)

Present: *Roberto Beccherle, Giovanni Darbo, Guido Gagliardi, Paolo Morettini, Carlo Schiavi.*

## 1. MCC-I2.

Status of MCC-I2 specs and implementation: Roberto makes a summary of what is already updated in the verilog code released in the CVS depository and what is still to be done (for rev.1 and 2). We also discussed on small different options in the implementation of architecture and on the additions of new functionality. The main points are:

- *Reset:* The structure of resets should be now fix in the verilog. Roberto modified as well the EVB state machines adding a reset and each "@posedge CK" state. This should avoid the manual correction of the synthesised code. The ECR now works also in configuration mode.
- *Exit from run mode:* in case of a slow command the MCC will exit from the run mode immediately. If the MCC is building an event this is truncated. In case the event is truncated before issuing an "enable data take" it is necessary to issue and ECR. If the EVB is idle when interrupted the MCC can be put to run mode without a prior reset of the data path. (Action: Roberto will implement those specs, Carlo will generate test vectors to verify them.)
- *EVB disable:* We decided to add a bit (EVBDIS) in the CSR to disable the EVB. In case EVBDIS=1, when the MCC is in run mode, the LV1 are generated in response of trigger commands and the PendingLv1FIFO is loaded with BCID and L1ID, the hits from the FE's are stored in the ReceiverFIFOs, the scoreboard is incremented, but no output is generated. At this moment is either possible to read the content of all ReceiverFIFOs, PendingLv1FIFO and scoreboard register or the EVBDIS bit can be cleared and then put back the MCC in run mode. In this last case the unreconstructed events are outputted. The user must be careful in case he reads the FIFOs: in this case a ECR should be issued before rearming the system. Also in case of events partially received the MCC cannot be rearmed before an ECR reset. (Action: Roberto will implement this mode, Carlo will test it)
- *Disable of Warning:* We decided to add two 16-bit wide registers (WBITD (warning bit disable), WRECD (warning receiver disable). If WBDIS<i>=1 (or WRDIS<I>=1) the warning bit (or the warning from the receiver) is disabled. The two bits and the two registers will be triplicated. (Action: Roberto will implement, Carlo will test it)

Test vectors: Carlo has corrected some test vectors. Also the high level C++ MCC-I2 model is going ahead and some bugs of the C++ model of the MCC-I1 have been fixed by Carlo (like the wrong increment of the BCID counter).

### SimPix:

Paolo has put in the CVS repository a SimPix update that fixes:

- Association of multiple LV1 in the analysis module;
- Output association of RD\_FIFO;
- Some correction to better check the results of FE configuration. Now test vectors in the file TEST-03-A.spx works correctly. I.e. no anomalies are reported and dump results correct.

In the to do list:

- FE-FLAG handling;
- Better analysis of CK, LD and DAO;
- Test of equal LV1;
- Consistence check of LV1;
- Tuning of the BCID counter such that in case of BCR both the verilog and the C++ have the same content of BCID. (This would simplify the test of the Verilog MCC model).

## **2. Irradiation analysis and new irradiation.**

Guido showed a draft of what he will present at the Pixel Week on the status and plans of MCC irradiation at PS. Guido will use the issues coming from the discussion to prepare the final presentation.