

Minute of the MCC-DSM Design Meeting held on 1st of March 2003

(Periodic meeting on MCC project progress)

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MCC-I2.

- Status of MCC-I2 specs and implementation: Some further changes have been decided in the MCC-I2 specs:
 - Changed the meaning of the two CSR bits used to report of error check: CSR[11]=LV1ChkFail is now used to flag errors in the check of BCID word amongst FE's. CSR[12]=EoEChkFail is now used to flag errors in the check of L1ID word amongst FE's.
 - Register WFE (address=3) records warning flags coming from FE chips.
 - Register WMCC (address=4) records warning generated by the Receivers (Hit overflow, EoE overflow and LV1 check errors)
 - The selection of which FE/MCC flags are reported in output data stream and in the WFE/WMCC registers is made by two 16 bit registers (WRECD and WBITD) and by a bit in the CSR (CSR[2]=RECD) which select two possible way of pairing WRECD and WBITD in the final selection of the bits to be reported. In more detail:
 - WBITD[12:0] : Selects which of the FE flags (WBITD[7:0]) and which of the MCC flags (WBITD[12:8]) are disabled.
 - WRECD[15:0] : Selects which of FE/Receiver flags are disabled.
 - CSR[2] = RECD: if '1' it disables flag generation from all the selected (WRECD[i]=1) FE/Receivers, while for the receiver not selected (WRECD[j]=0) the flag generation is controlled WBITD. If '0' the selection of the bits not generating flag is active only for the FE/Receivers disabled (WREC[i]=1).
- Status of SimPix and test: A new version of SimPix is available which fixes problems in the run of the TEST-08-xx.spx vectors. Also some new rules are imposed in the writing of the scripts:
 1. Have an event for each trigger;
 2. Align LV1 for the two MCC (C++, "Real").

Rule 1 means that in case of contiguous triggers only one event block must be used with as many hits_eoe as the number of contiguous triggers. Also, if a LV1 is skipped an empty event must correspond to:

```
EVENT
END_EVENT
```

With the new SimScript version it is possible to have loops inside event blocks:

```
WR_REGISTER LVL1 0F00
LOOP I 0 100
200 TRIGGER
  EVENT
    LOOP J 1 16
      HITS_EOE FFFF 1 0
    END_LOOP
  END_EVENT
END_LOOP
```

Instead of

```
HITS_EOE mask hits_avg hits_sigma lvl1_num
```

can be used the construct

```
HITS mask hits_avg hits_sigma lvl1_num
HITS_WNG mask hits_avg hits_sigma flag lvl1_num
EOE mask lvl1_num
WNG mask flag lvl1_num
```

where WNG e HITS_WNG are new keywords and are for writing the FE flags.

Rule 2 means that the `addedlatency` parameter in the `default.dat` file must be correctly set for proper functioning. This parameter depends on the kind of connection to the MCC used: MCCexerciser, pattern generator, verilog. For the verilog the correct value is 8.

Paolo tried to reproduce situations similar to what have been seen and reported by Kevin by SimPix, but nothing anomalous have been seen. We decide to reproduce and study them in the lab.

Module test.

The signal splitter (see previous MCC meeting) TPCC/TPLL/MCCex (MTT) will be designed in the next weeks.