Spatial resolution predicted for the BTeV pixel sensor

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- Physics processes modeled in the simulation
- Some detailed studies
 - Effect of different thresholds
 - Advantages of analog readout
 - Sensitivity to digitization accuracy
- Reality check: a comparison with our test beam data

Physics processes modeled in the simulation



- Energy deposition by charged track along its path length. Spread of the electron cloud due to diffusion.
- Drift in **E** corresponding to doping and bias voltage.
- **E x B** (our sensors will be in dipole field of 1.6 T).
- Realistic parameters of the front end electronics (noise, threshold, digitization accuracy).

Simulation of electron-hole creation



- Charge track path length, divided into ~30 µm slices
- E_{dep} in each slice fluctuates according to experimental straggling distribution(Bichsel, Rev. Mod. Phys. 60, (1988) 3.)
- Resultant charge distribution has FWHM ~10 Ke
 - Tail truncated (δ rays ignored)

Hypotheses and caveats

- The algorithm implemented is quite general
- Most of the results will use parameters tuned to the proposed BTeV experiment:
 - Pixel cell 50x400 μm
 - Analog readout with 1 flash ADC/cell
 - Peaking times of the order of 100 ns (⇒ we can assume full charge collection)
 - Collected charge carriers are electrons (n⁺np⁺ sensors)

What we did not include so far

- Non-Gaussian tails due to δ rays
- Effects of possible lateral **E** field distortion
- Time dependent effects due to the electron current pulse shape
- Capacitive coupling effects between pixels

Charge spreading due to diffusion

• The diffusion coefficient is associated to the carrier mobility through:

$$D_e = \frac{kT}{q} \mathbf{m}_e$$

• We assumed $m_e = 1450 \text{ cm}^2/\text{Vs} \Rightarrow$

$$\left< \sqrt{\Delta r^2} \right> = \sqrt{2D\Delta t} \approx 12\mu m$$

Charge spreading due to diffusion and its interplay with the magnetic field



- Lateral spread due to diffusion
- Interplay between B field and diffusion
 - At normal incidence

– For an angled track

Simulation of front end electronics

- Key elements
 - intrinsic noise (expected to be very small throughout the detector lifetime for fpix2)
 - discriminator threshold
 - digitization accuracy for analog readout

Advantages of analog readout

- Analog readout improves spatial resolution using charge weighting, and allows more effective monitoring of sensor and readout chip performance.
- Effectiveness depends upon electronic noise, threshold and digitization accuracy.
- Interplay between these effects will be discussed

Sensitivity to different front end electronics thresholds



- Noise and digitization resolution effects neglected
- Slow degradation of the resolution for relatively low thresholds and analog readout

Optimization of position reconstruction algorithm-small θ



Analog information can be used to interpolate between pixel centers Non-linear nature of diffusion requires a correction factor $f(x_{rec}, \theta)$

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Optimization of the position resolution – medium θ



- When angle spreads the charge among several pixels, charge division becomes
 linear and effect of correction negligible
- Limitations of binary readout more evident

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Sensitivity to digitization resolution

2 bit ADC 8 bit ADC (FPIX0 readout) 3 bit ADC (logarithmic)



• 3 bit ADC with thresholds scaling in In ratio has a performance comparable to an 8 bit **ADC**

> \Rightarrow Our front end electronics is optimized for BTeV needs

Magnetic field effects



- Si thickness assumed 280 µm
 - Magnetic field induces
 a shift of about 17 deg
 in the charge
 orientation in the bend
 plane

Reality check: a comparison with test beam data

- The BTeV pixel group has recently collected an impressive amount of beam test data on n⁺np⁺ sensors bump bonded to two different front end devices (see G. Chiodini's talk)
- We can perform a direct comparison of the resolution predicted from this simulation and experimental data with various experimental parameters (bias, track angle, digitization resolution..)

A quick reminder on our test beam set-up



- 5 pixel planes tested (n⁺np⁺ sensors, with p-stop and pspray insulation)
- We learned a lot of things, here I will focus on the measured resolution for two different front end electronics devices: FPIX0 (analog output connected to external 8 bit ADC) and FPIX1 (2 bit on chip FADC).

Comparison of FPIXO data with the predicted spatial resolution

8 bit ADC data
 binary data



Track Angle (deg)

- Input parameters:
 - 280 mm thick detector (n⁺np⁺) with p-stop interpixel implantation
 - Average threshold 2.5 Ke
 - 8 bit ADC external to the chip
- Same data analyzed with only binary interpolation and with analog interpolation with nonlinear correction

Comparison of FPIX1 data with simulation

- threshold = 3.78 Ke

threshold = 2.5 Ke



- Input parameters:
 - 280 mm thick detector (n⁺np⁺) with p-stop interpixel insulation
 - Average threshold 3.78 Ke
 - 2 bit on chip FADC
- We show also the predictions with 2.5 Ke threshold to disentangle effect of higher threshold from effects of coarser digitization

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Conclusions

- The simulation tool developed gives results in good agreement with test beam data and allow us to tune the sensor and front end electronics parameters for optimum performance
- It is quite general: can be used for other applications
- A more detailed study of the effects neglected (δ rays, imperfect knowledge of s-curve correction etc.) and may lead to a more complete understanding of the test beam data.