

Roland Baur

PIXEL 2000 Conference

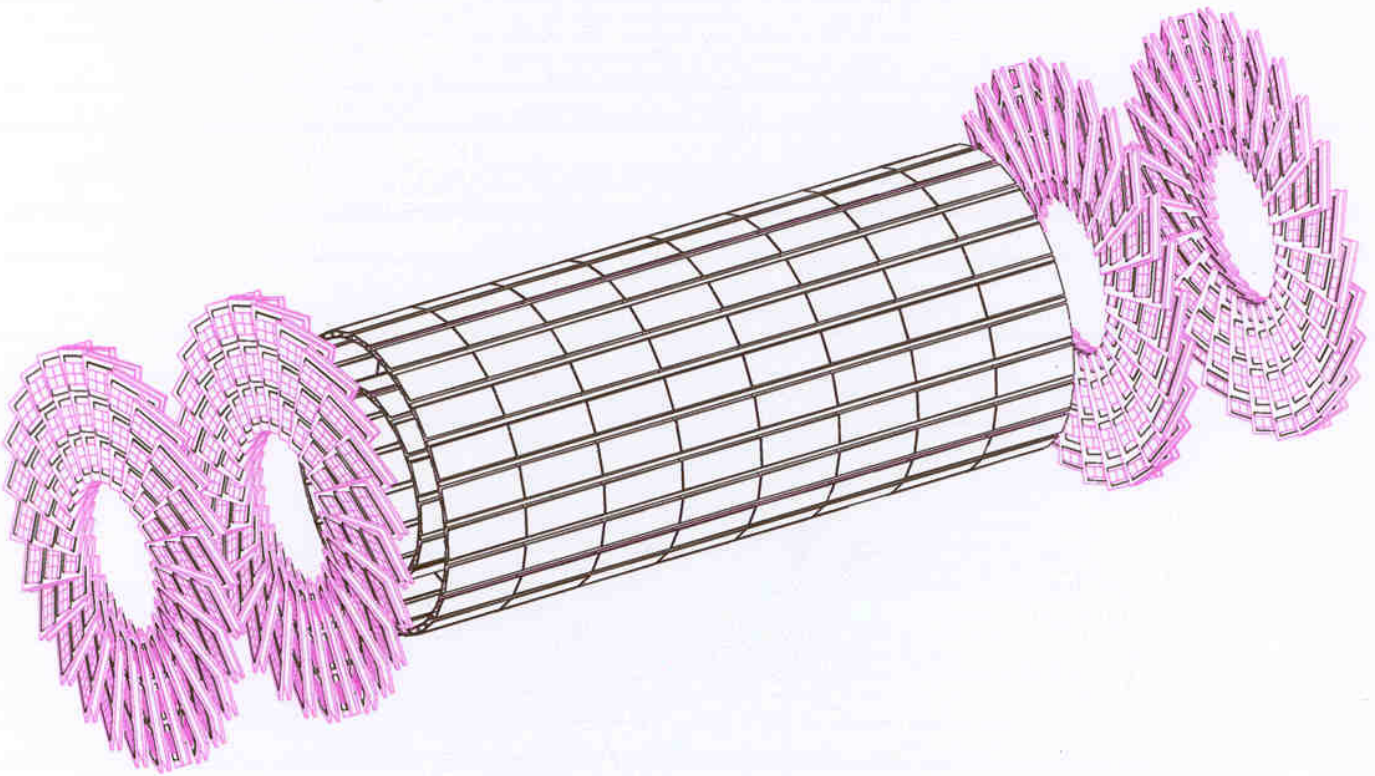
Genova June 5.-8.



Readout Architecture of the CMS Pixel Detector

1. Introduction
2. Pixel Cell and Column Periphery Architecture
 - analog block
 - data buffer
 - analog data transfer
 - data format
 - timestamp buffer
 - data losses
3. Single Event Upset Measurements
 - Comparison DMILL/Honeywell
4. Conclusion

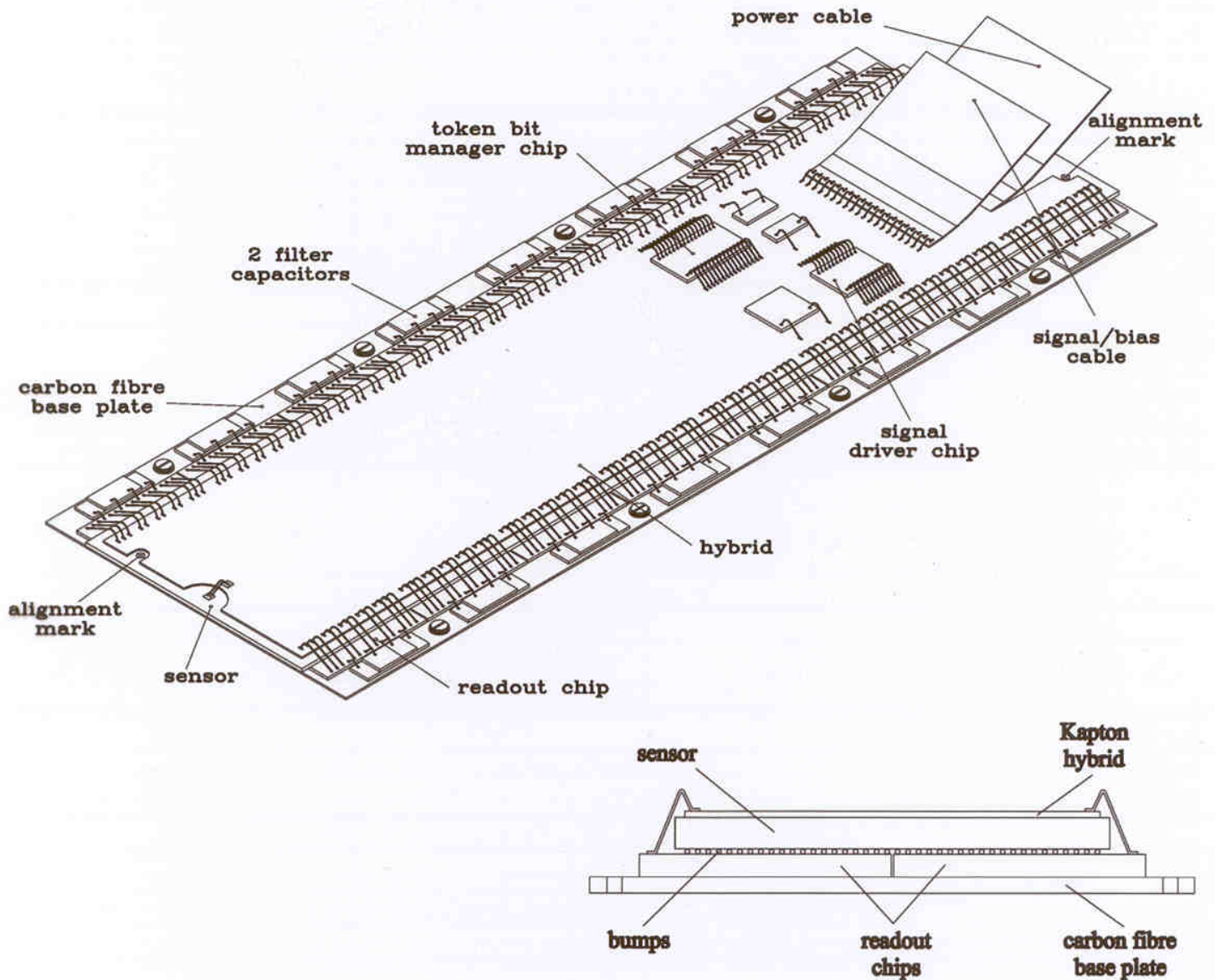
CMS PIXEL Detector



- 3D - tracking points
- $\sigma(z) \sim \sigma(r\phi) \sim 15\mu\text{m}$ for precise impact parameter in $r\phi$ & z
- LAYERS: $r =$ 4.3cm 7.2cm 11.0cm
 Low Lumi high Lumi
- replace layers after $6 \times 10^{14}/\text{cm}^2$
- readout electronics of all layers and blades identical
- modules based on a 53×54 pixel readout chip

BARREL PIXEL MODULE

- Silicon sensor $16 \times 64\text{mm}^2$, $250 \mu\text{m}$ thick, $150\mu\text{m}$ square pixels
- 16 Readout chips (52×53 pixel) \rightarrow $\sim 44\text{k}$ pixel \rightarrow 2.4 Watt
- $\sim 1\% X_0$



BARREL & FORWARD PIXEL

Table 1: Parameters of CMS Pixel Barrel

	Configuration	Radius [mm]	Faces (*)	full/half Modules	Chips	Pixels	Area [m ²]
Layer 1	low lumi	41 - 45	18	128/32	2304	6.35×10^6	0.15
Layer 2	low & high lumi	70 - 74	30	224/32	3840	10.6×10^6	0.25
Layer 3	high lumi	107 - 112	46	352/32	5888	16.2×10^6	0.38

(*) Two half faces are counted as one face

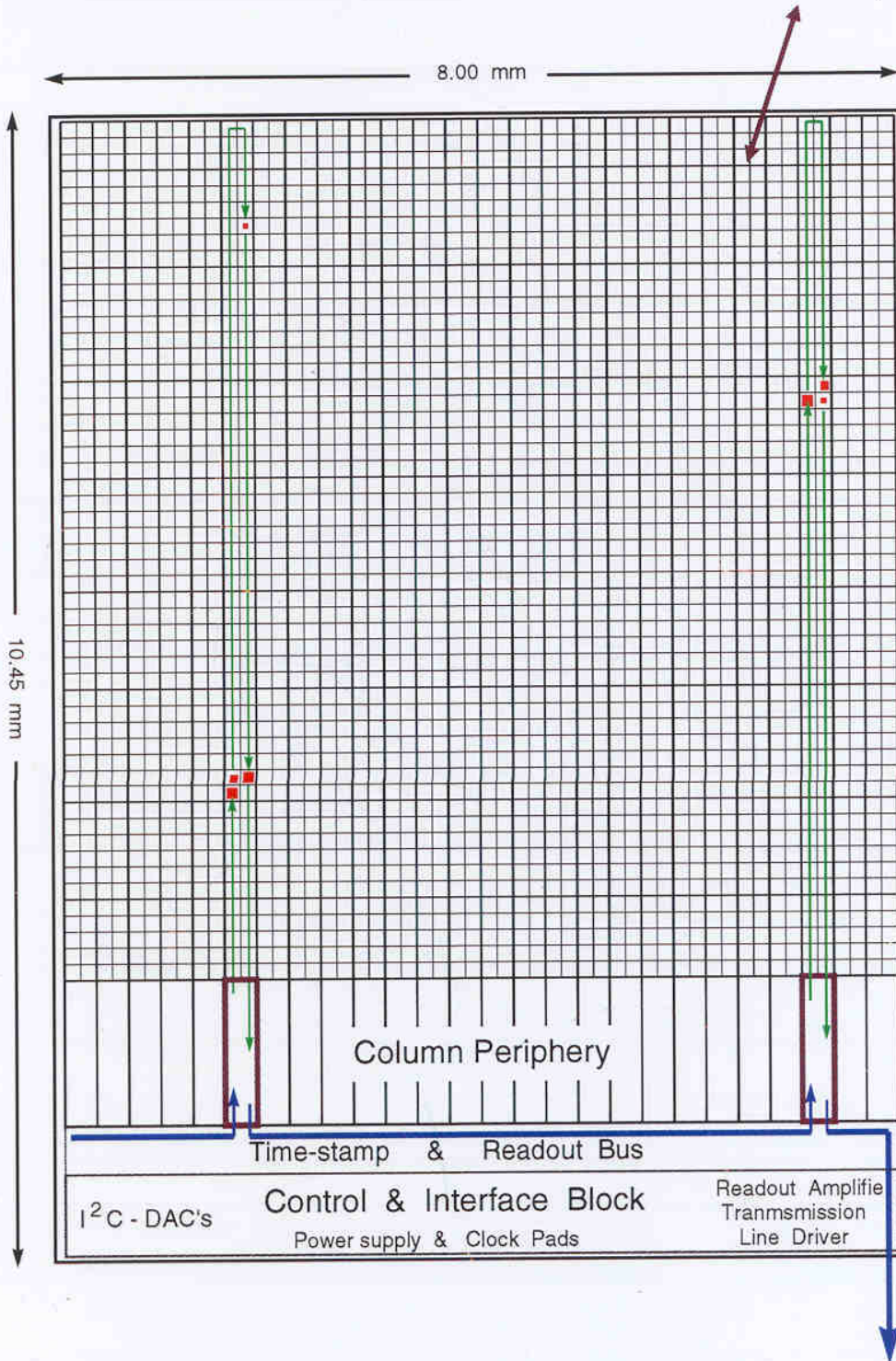
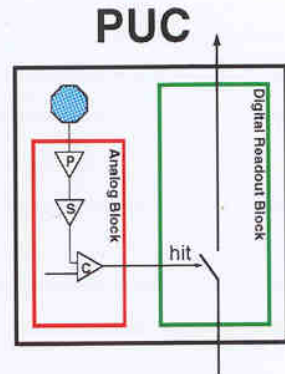
Table 2: Parameters of CMS Pixel End Disks

z cm	Radius mm	Blades	Sensor Modules	Chips	Pixels	Area m ²
± 32.5	60 - 150	24	7	1080	3.0×10^6	0.07
± 46.5	60 - 150	24	7	1080	3.0×10^6	0.07

PIXEL READOUT CHIP

- 52 x 53 pixels PUC: 150 μ x 150 μ

Data flow of pixel hits in
Column Drain Architecture

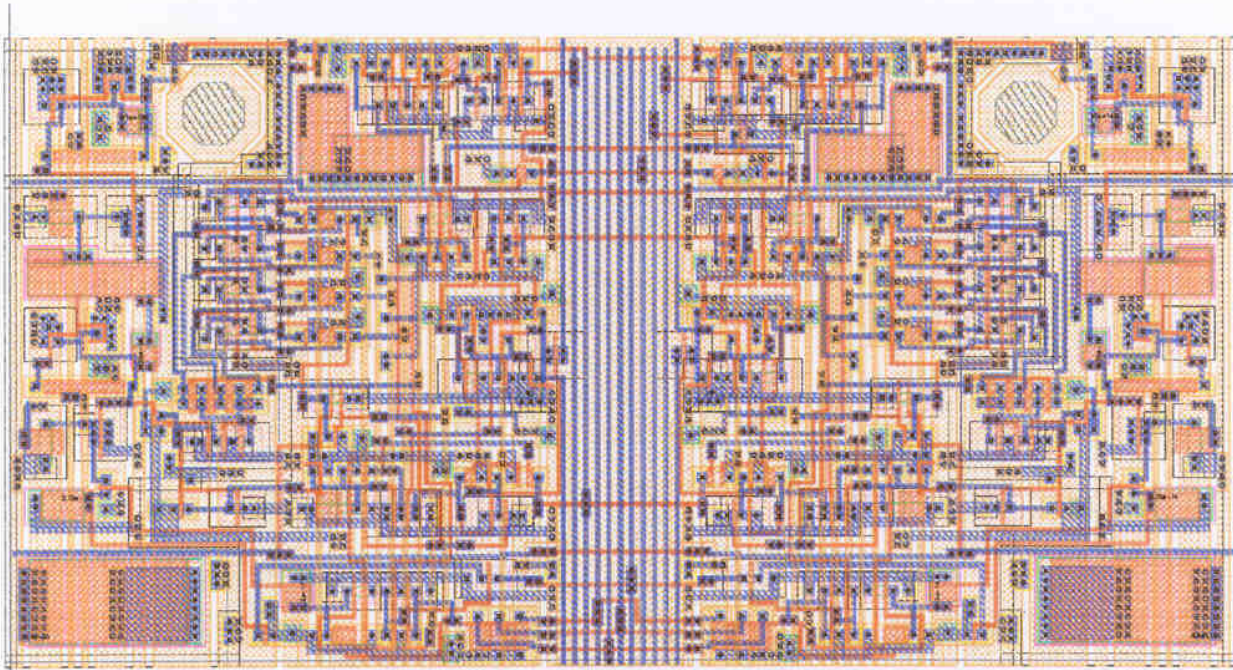


PIXEL UNIT CELL

DM_PSI41

(Subm. July 2000)

- PUC of final Read Out Chip ! (150 μ x 150 μ)
- Complete Column Drain Architecture

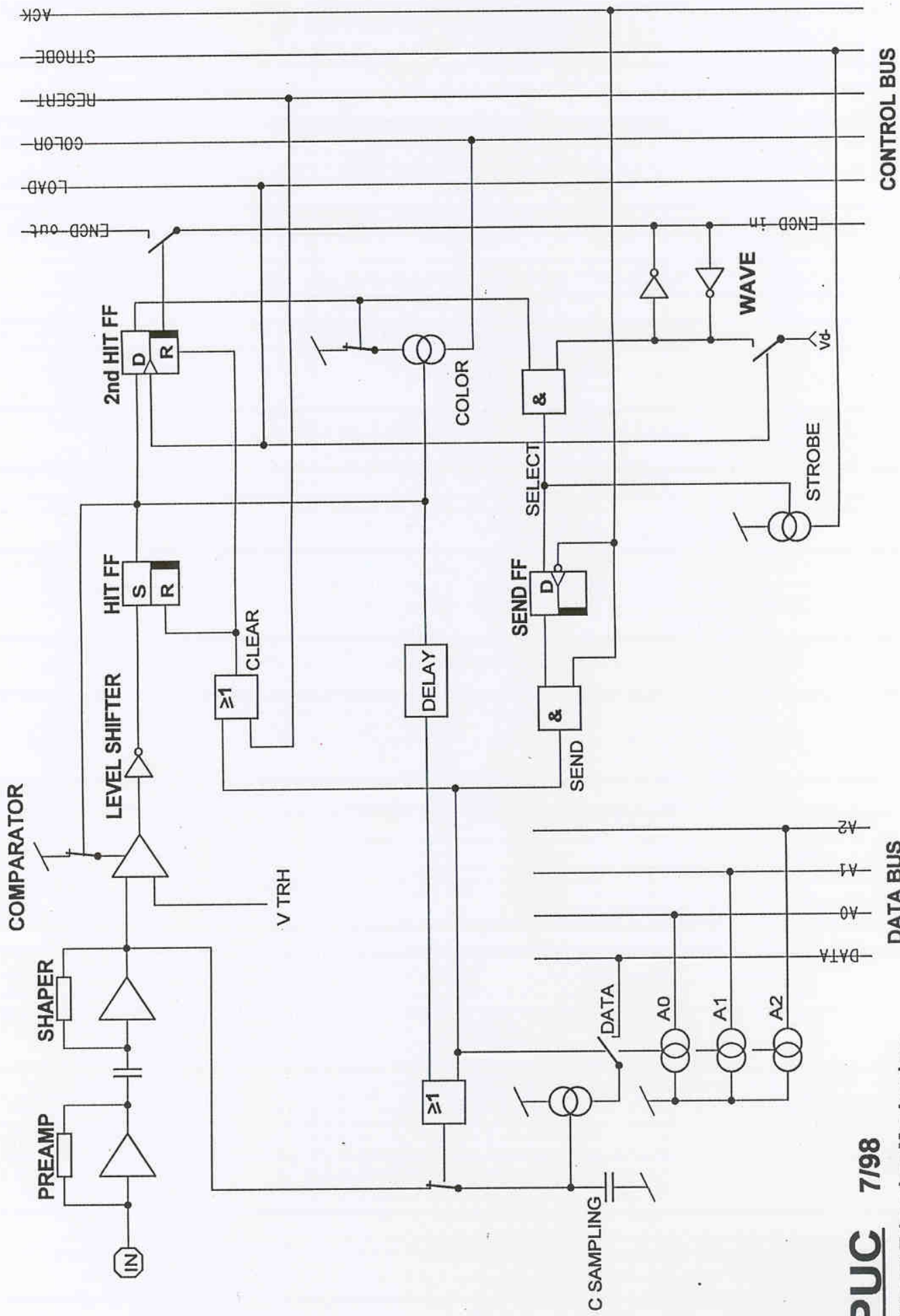


- Yield tolerant pixel design → Separate mask bit, mask at digital level
- New programming mechanism → robust programming, iniform DAC
- Fast Analog Block (DM_PSI35) and improved Comparator
- Improved CDA skip mechanism → expect 25% more speed (~ 1.8GHz)

Devices / pixel

→ 125 Total

- 64 PMOS
- 54 NMOS
- 7 Caps

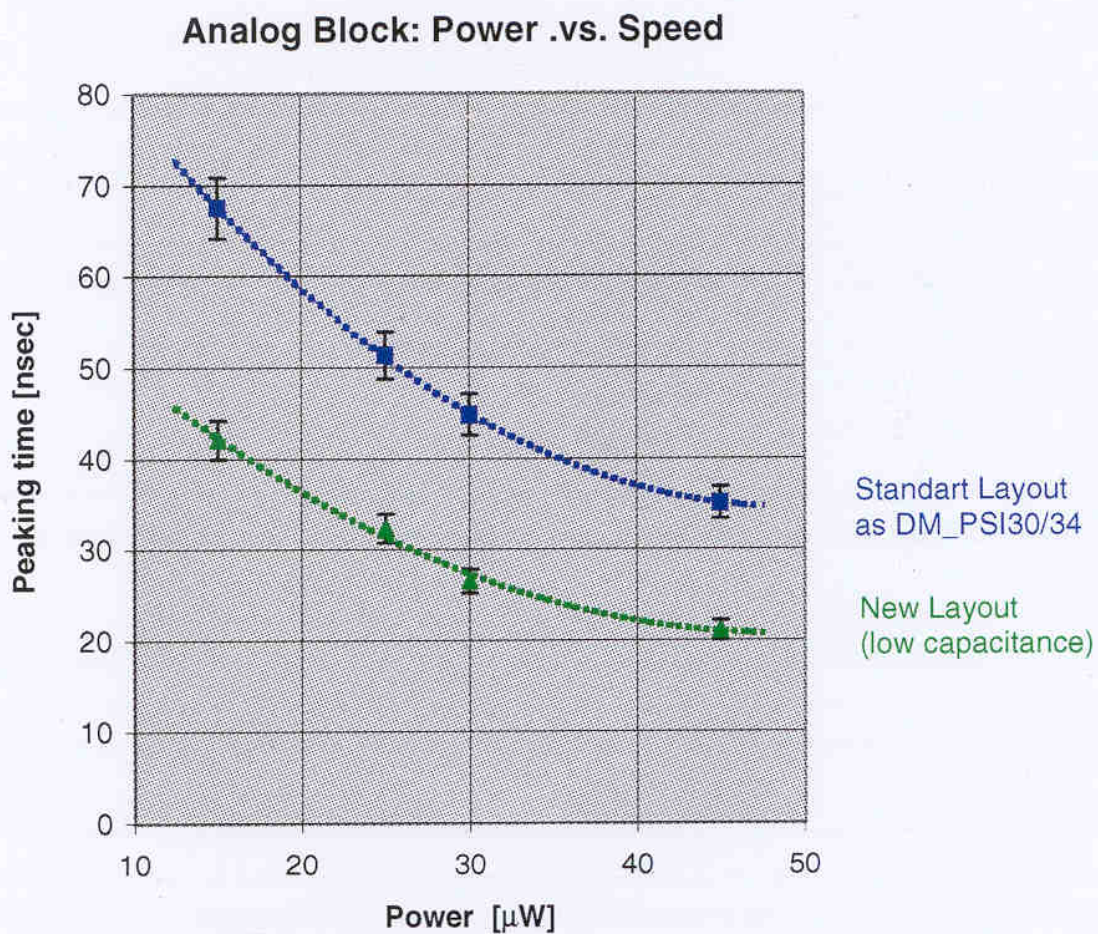


PUC 7198
without Trimming Mechanism

ANALOG BLOCK SPEED

DM_PSI35 tests various Analog blocks (bipolar & CMOS)

Analog Block speed improved by **low capacitance layout**.



- Adjust shaping for equal signal amplitude as in old layout.
- Both designs with about same noise of 115 - 140 electrons

At equal speed : save ~ 20μW power per pixel!!!! --> material budget !!!

ANALOG BLOCK: peaking time

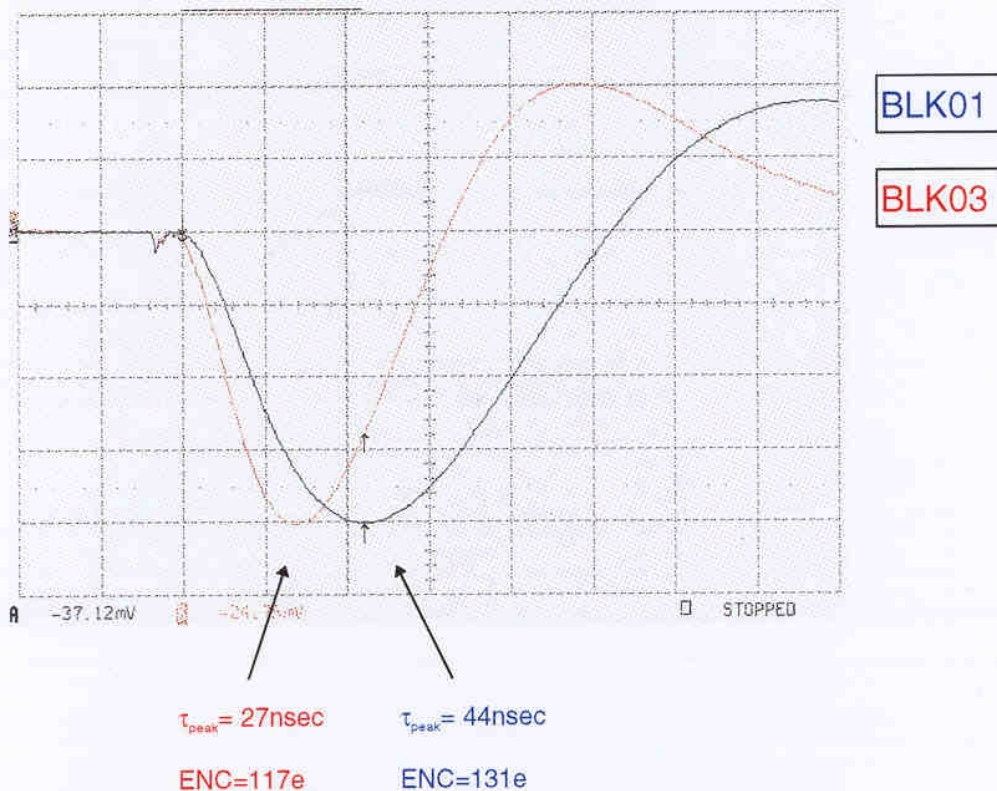
PSI35 (DMILL) Test various preamplifier & shaper designs.

BLK01 : Standart Preamplifier & Shaper as used in DM_PSI30/34

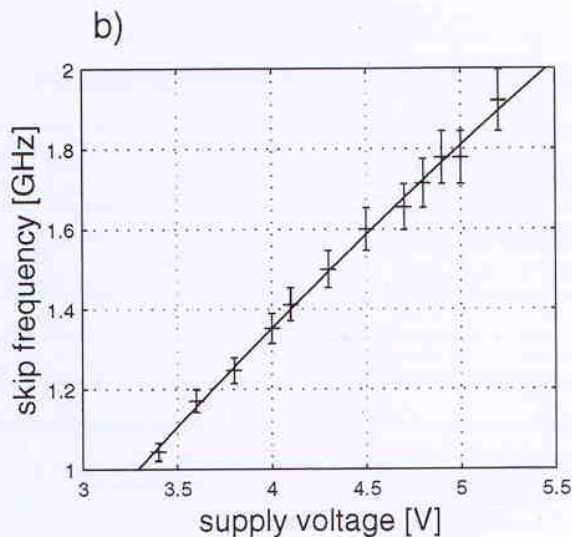
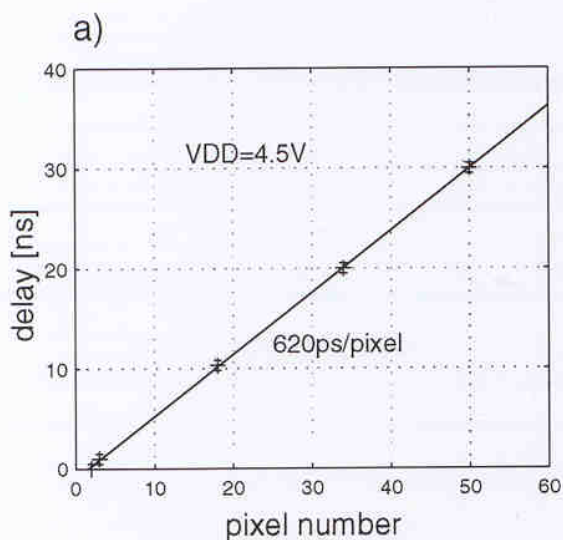
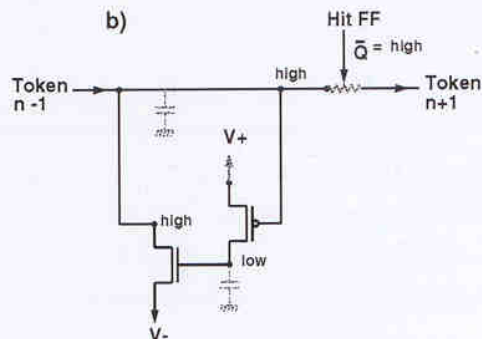
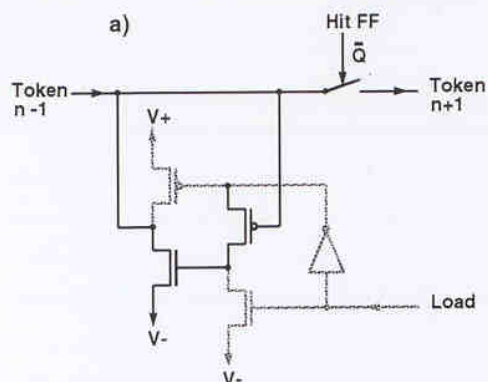
BLK03 : Circuit as BLK01 but optimized, **low capacitance layout !!!**

Operating conditions for both:

- Power = 31 μ W
- equal Pulseheight (shaping adj.)
- Signal = 6000e
- non irradiated measured



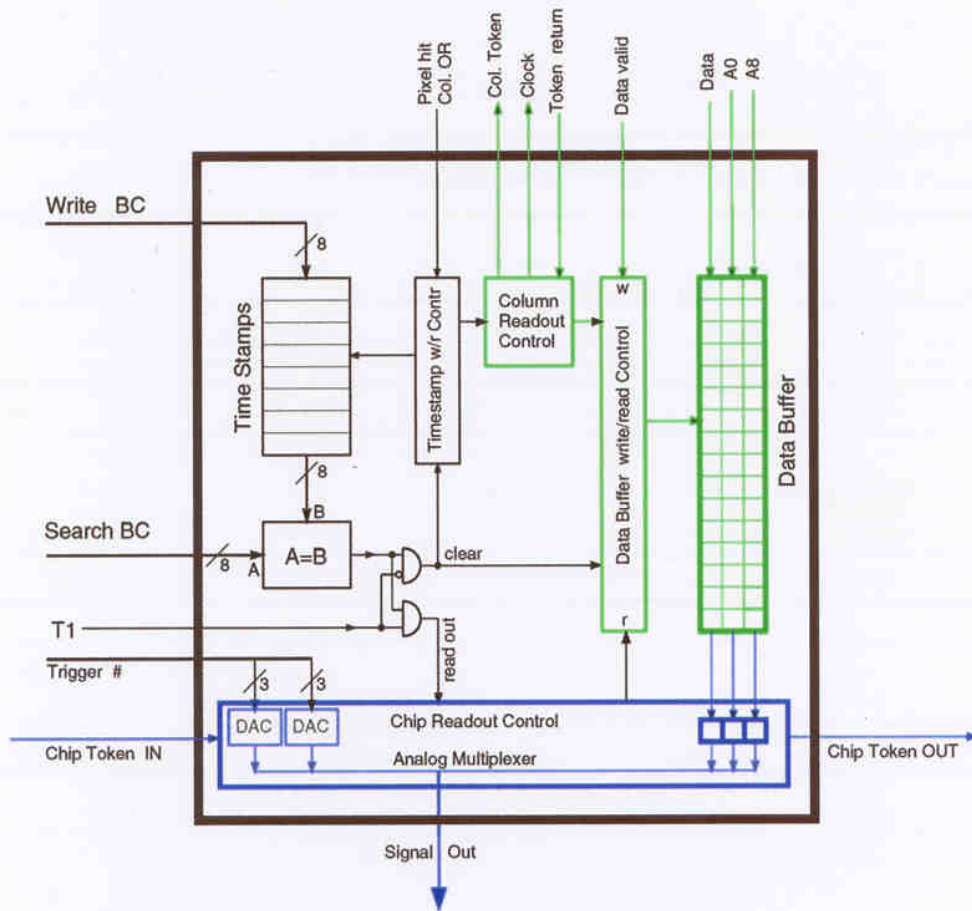
TOKEN BIT SCAN



Token Bit takes 66 ns to travel through empty double column.

Crosstalk from Token Bit travelling through pixel to pixel input pad <750 electrons.

COLUMN PERIPHERY



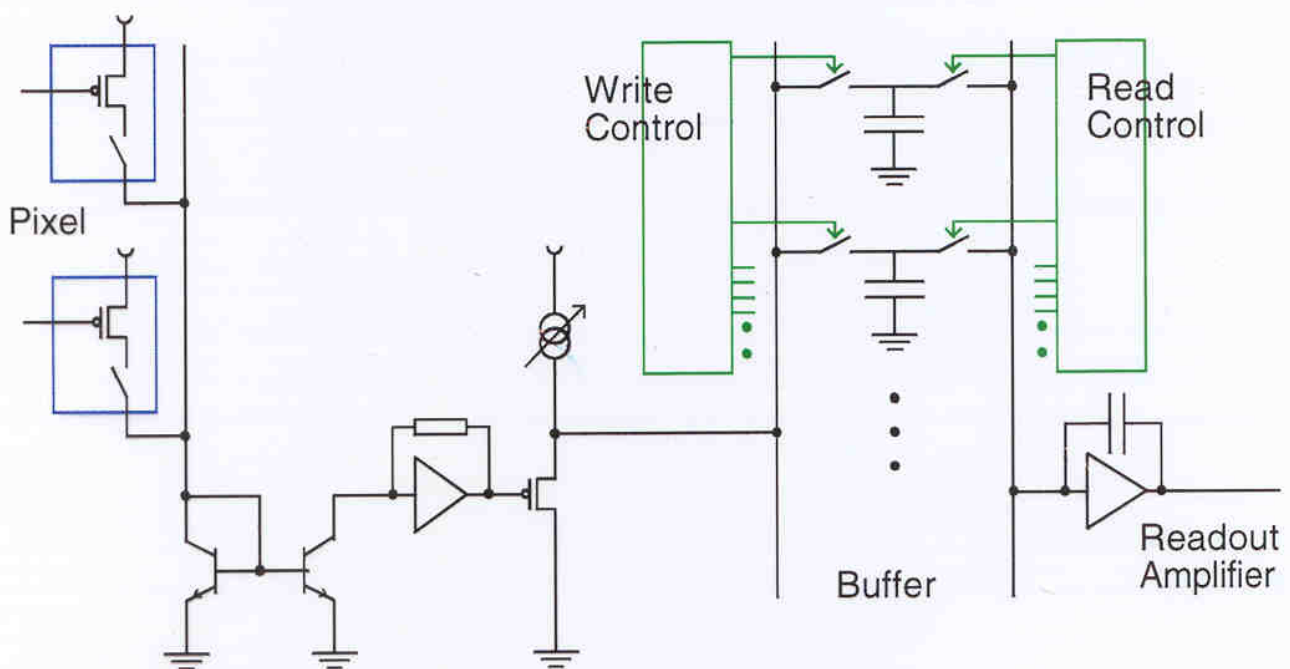
- Dual-ported hit buffer (**Column Drain** <--> **Chip Readout**)
- Time-stamp verification with T1 trigger
- Data formatting and readout of T1-verified hits with analog coded pixel address header
- 8 Timestamp buffers & **24 Pixel hit buffers**
- **fixed format readout (6 clk)** of pixel hits

ANALOG DATA TRANSFER FROM PIXEL TO COLUMN PERIPHERY

DM_PSI34 (DMILL) rec. Dec. 98

- Test chip with pixel column of correct length and 24 periphery buffers and readout chain.
- Analog coded pixel addresses (A_1, A_5, A_{25}) and pixel pulse height transferred to periphery buffers.
- Addresses & Pulseheight with same circuits (4 SC/buffer)
- Speed, uniformity, droop rate

Simplified Schematic



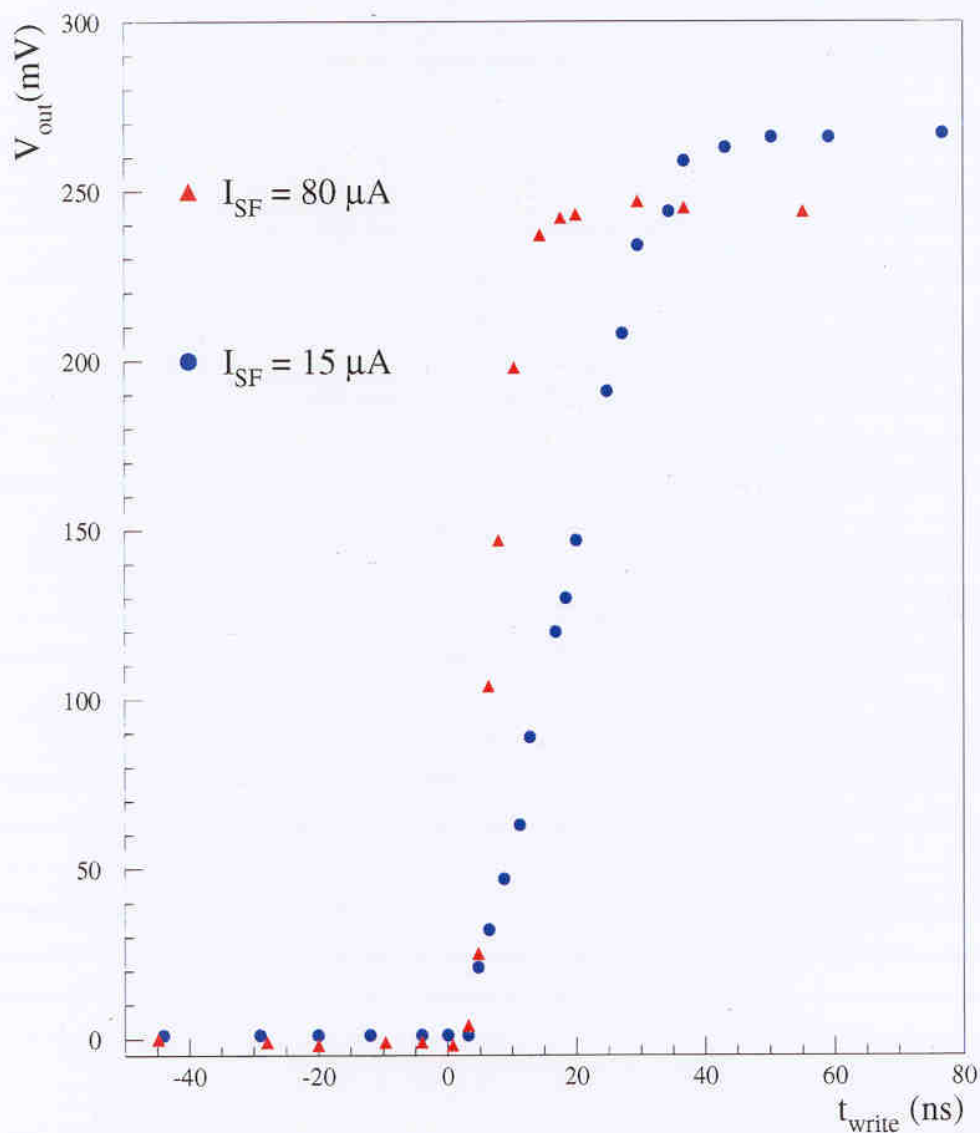
SPEED OF ANALOG PIXEL TO PERIPHERY TRANSFER

DM_PSI34 (DMILL)

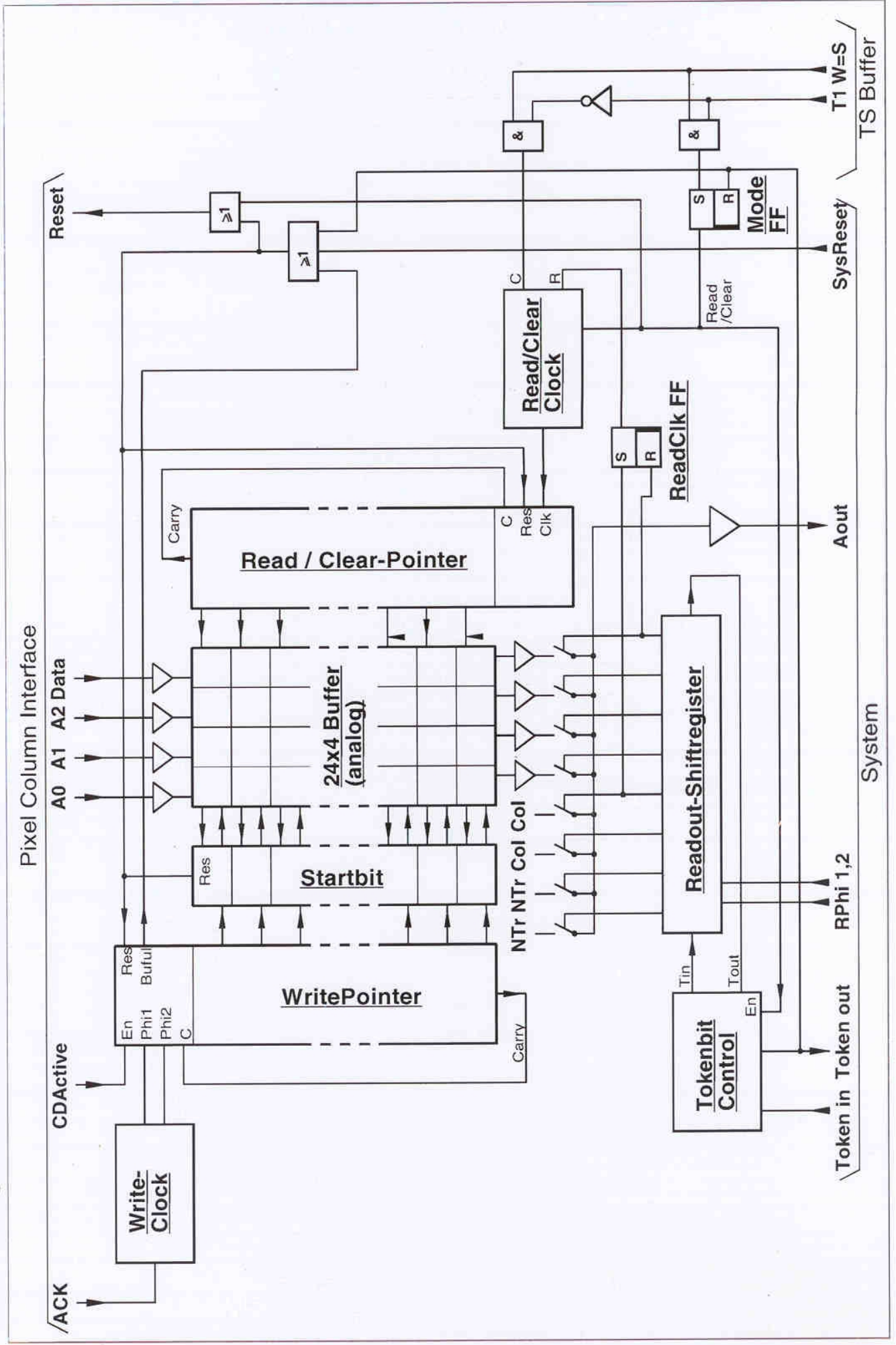
- Analog data transfer speed currently limited by source follower.
- CDA mechanism active ~10% of time ----> ~0.4 μ W/pixel

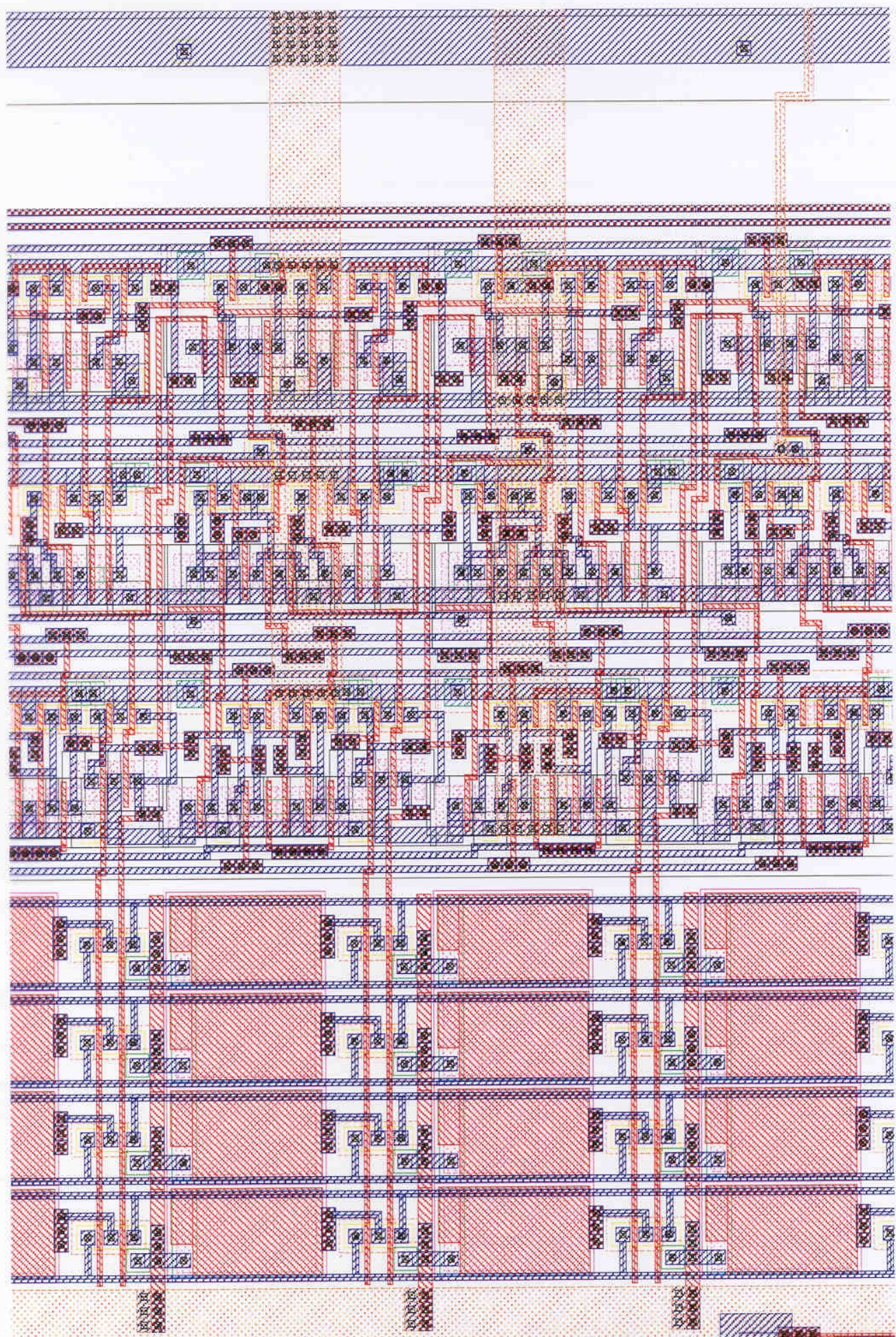
Analog Data Transfer Pixel \rightarrow Buffer

W. Erdmann
M. Hilgers
Jan 99



Block Diagram: Data-Buffer (DB)



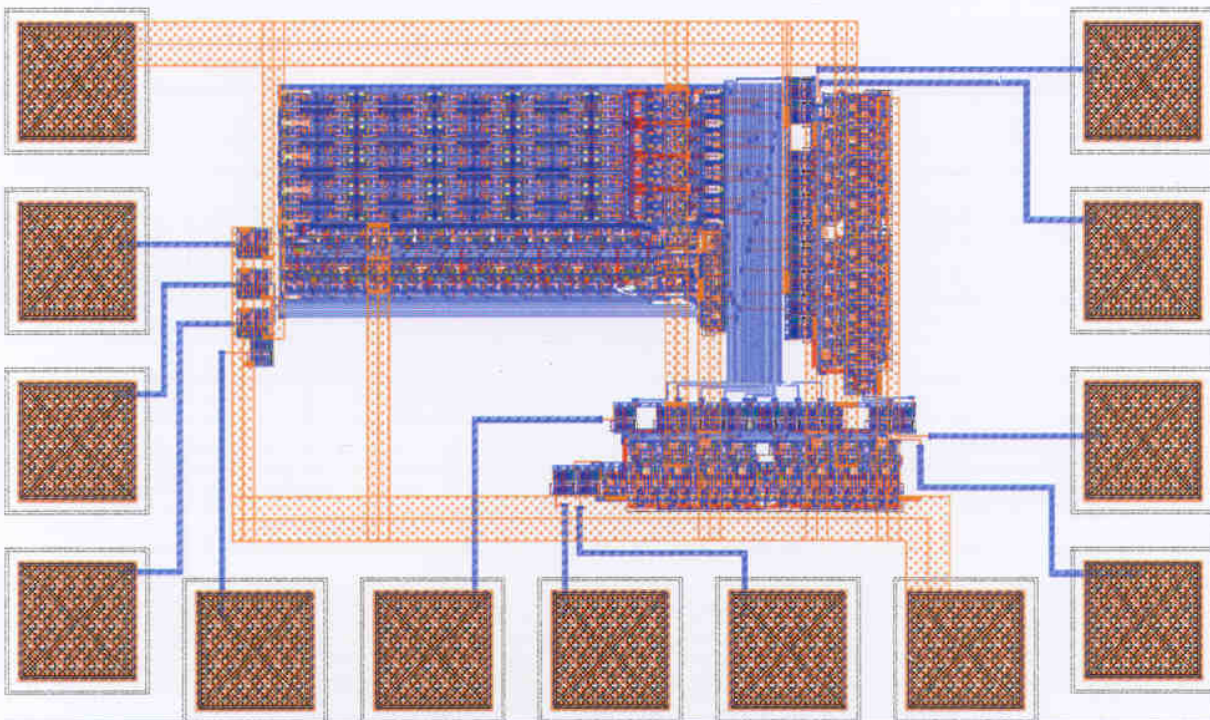


TIMESTAMP MECHANISM FOR PIXEL READOUT CHIP

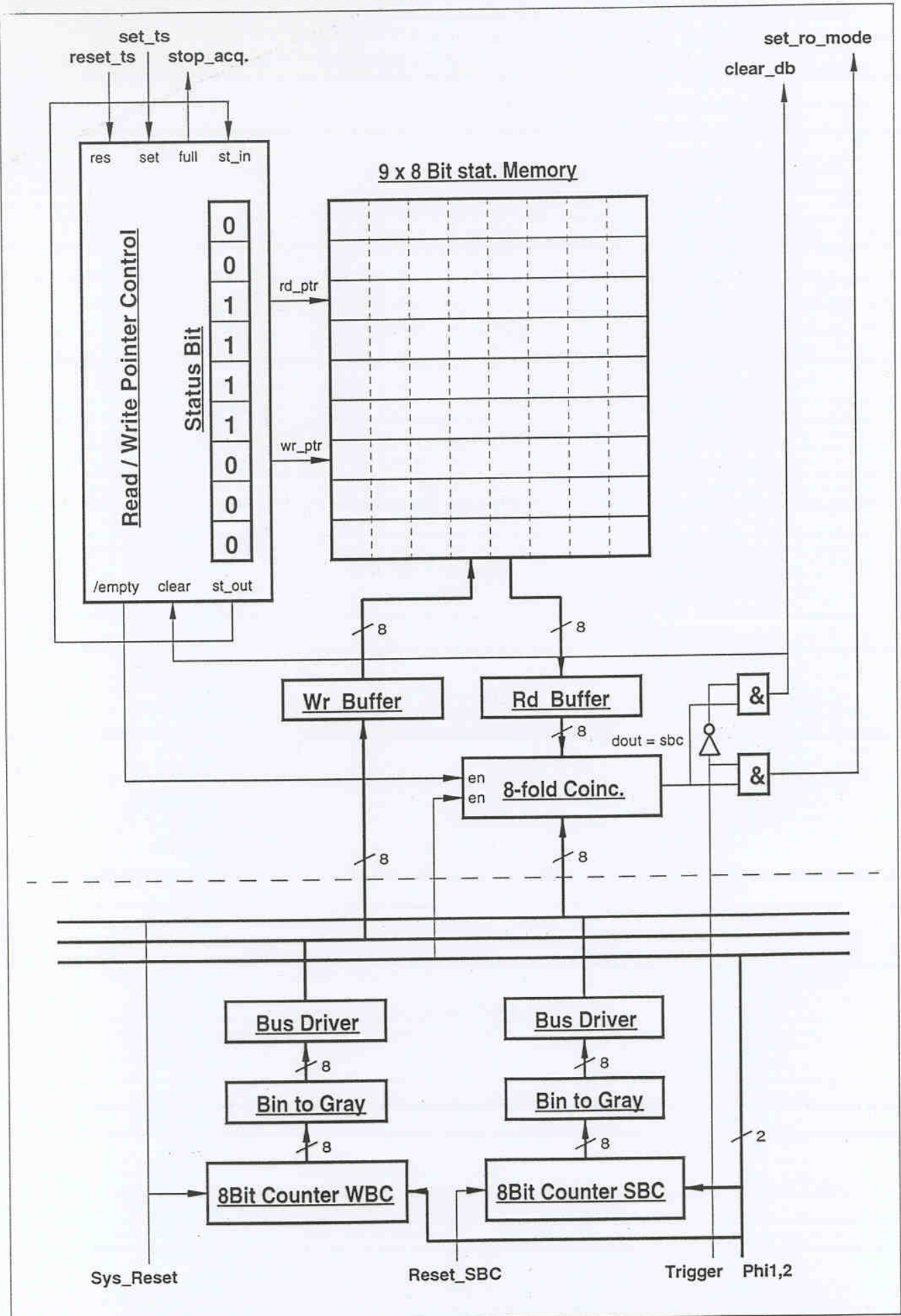
(functional blocks developed in 98/99)

DM_PSI38 (rec. April 2000)

- 9 timestamps of 8 bits with corresponding pointer mechanism
- Gray-Boudot Counters for WBC & SBC
- 8 bit (256 bc) trigger delay possible (programmable)
- Double column wide layout for final use (i.e. 300 μm wide)
- First tests with 20 MHz show successful operation
- Max. clock frequency after irradiation will be measured soon

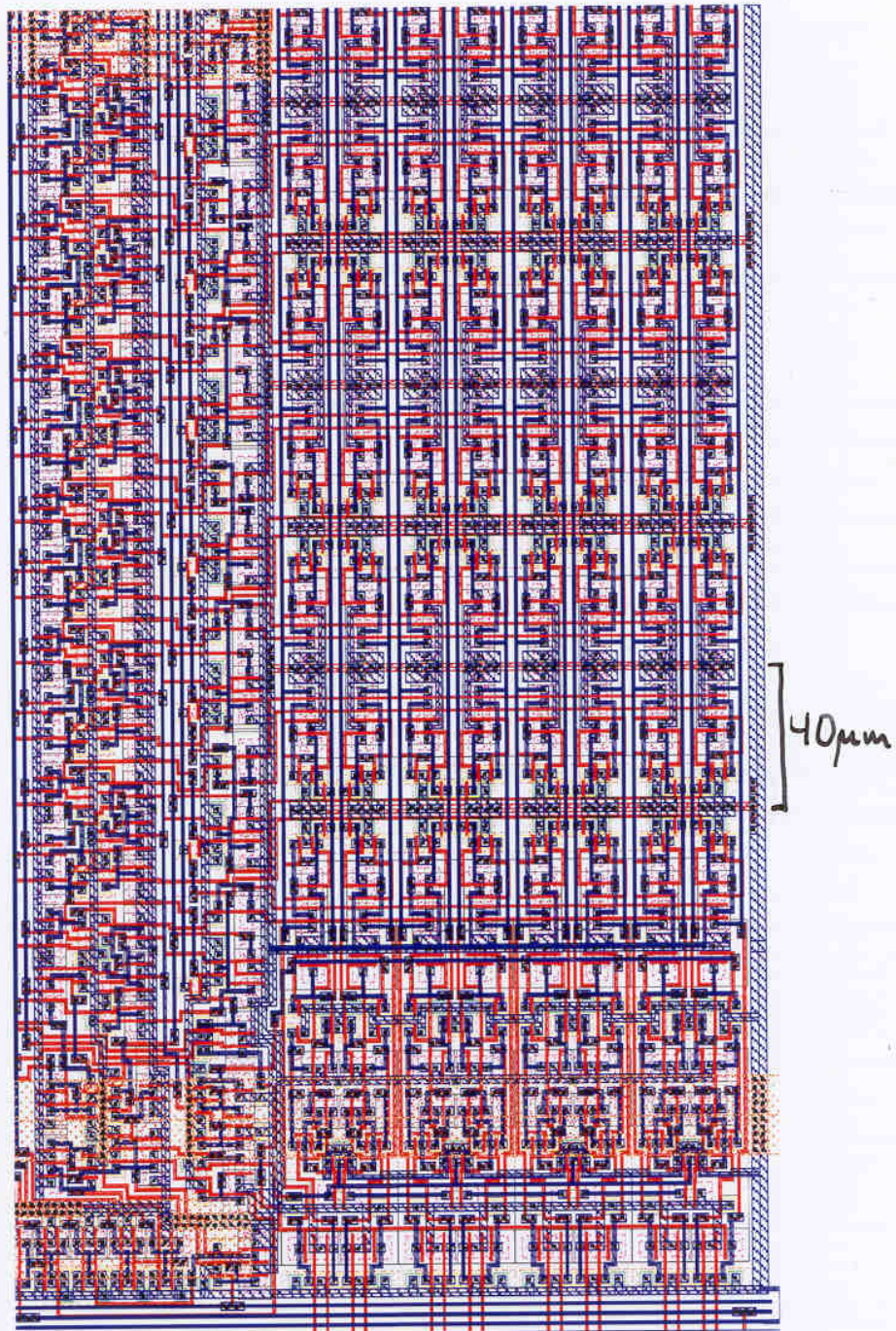


Block Diagram: Timestamp-Buffer (TS)



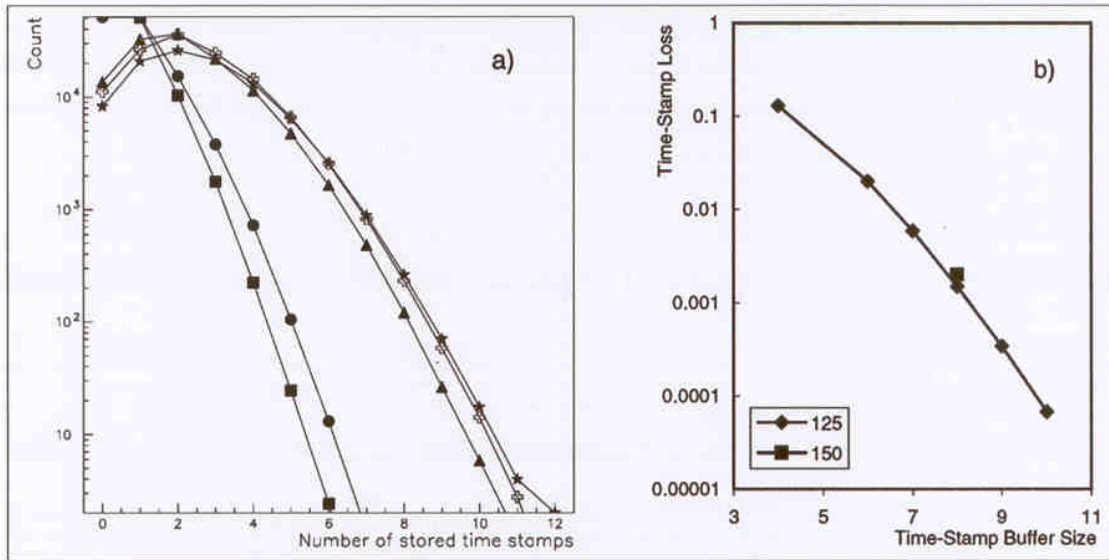
Timestamp Buffer

Detailed View

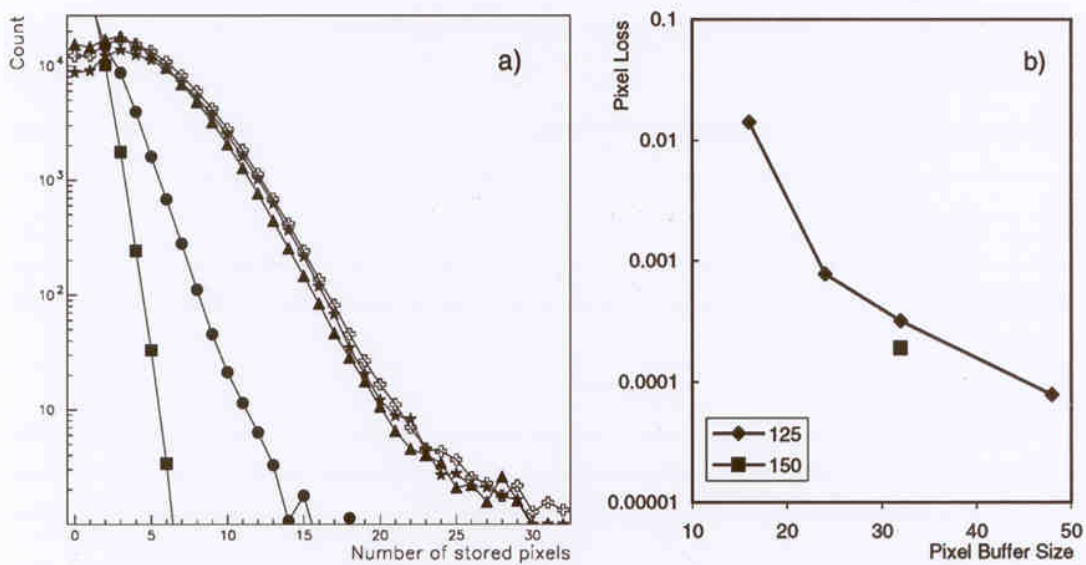


BUFFER SIZE REQUIREMENTS

Time Stamp Buffer

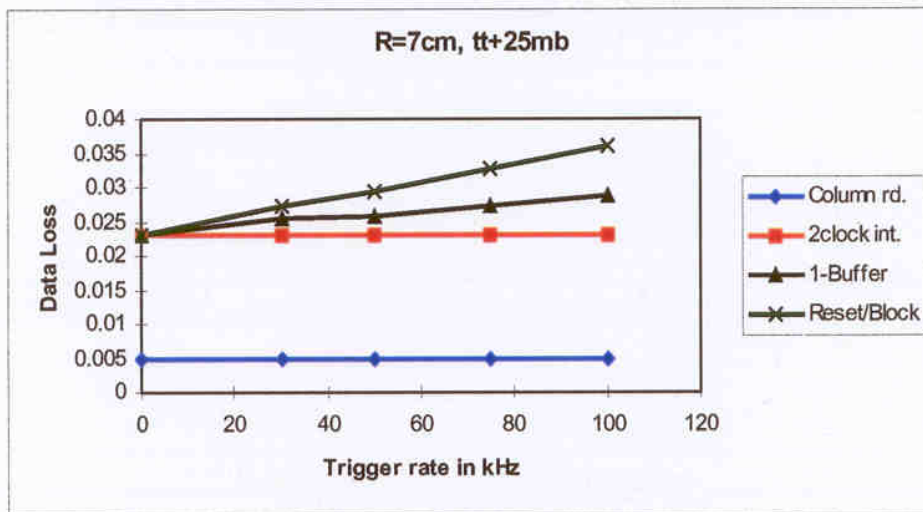


Pixel Data Buffer



READOUT DATA LOSS

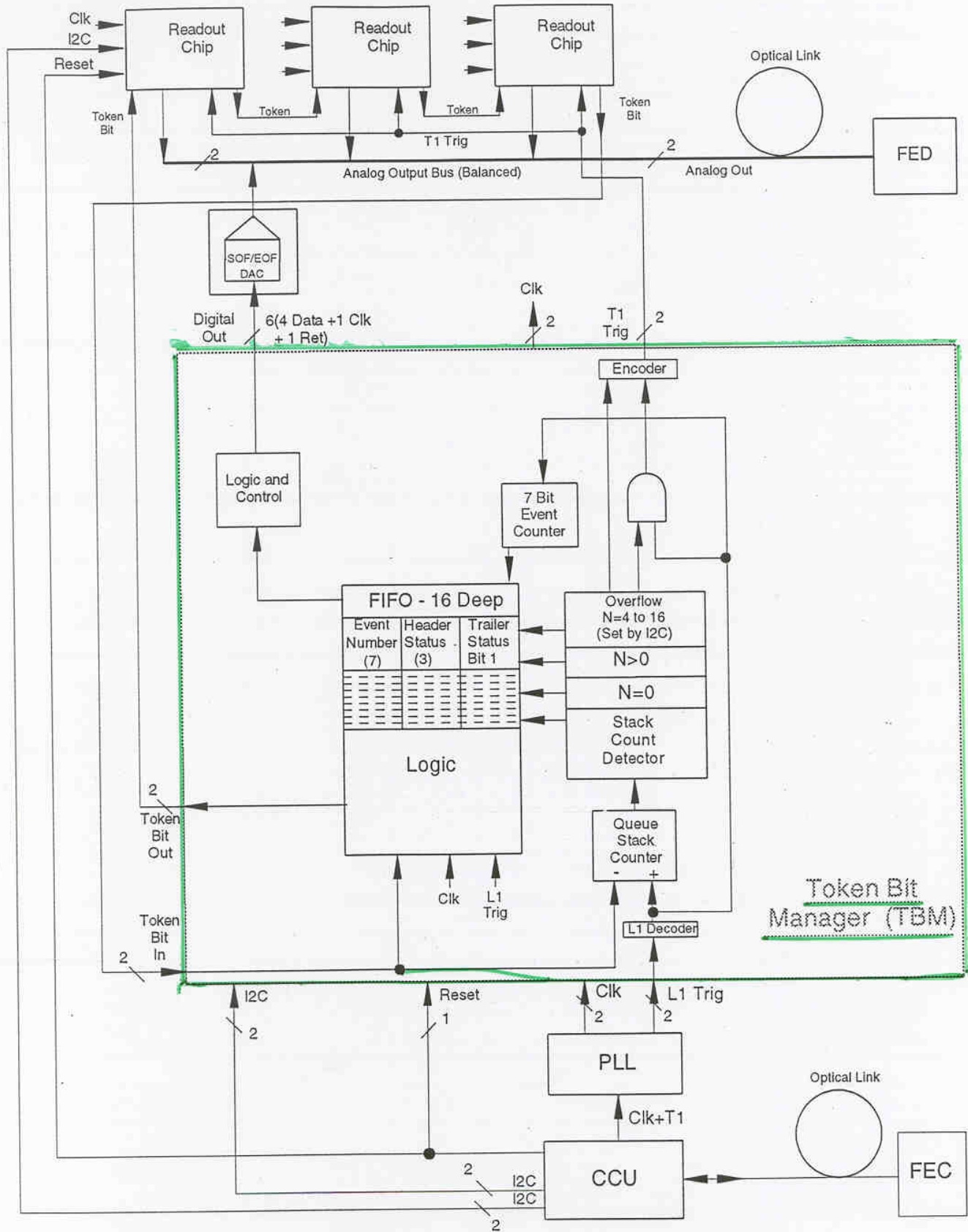
Pixel Barrel Layer at 7cm, full LHC luminosity



Sources of data loss :

1. Column readout losses e.g. pixels overwritten, column busy, time-stamp and data buffers full.
2. Readout data buffer overflow, a column can store only one 1LT trigger confirmed time stamp.
3. After readout the column is reset, all time stamps are lost.
4. Dead time of 1 clock (25ns) to setup the column readout mechanism after this column was hit.

(Improvement in the final design possible!!!)



Token Bit Manager Detail
Forward Pixel Block Diagram

Rev 6 10/8/98 File:(TBM-R6)
<http://www.physics.rutgers.edu/hex/cms>

Analog Coded Pixel Addressing

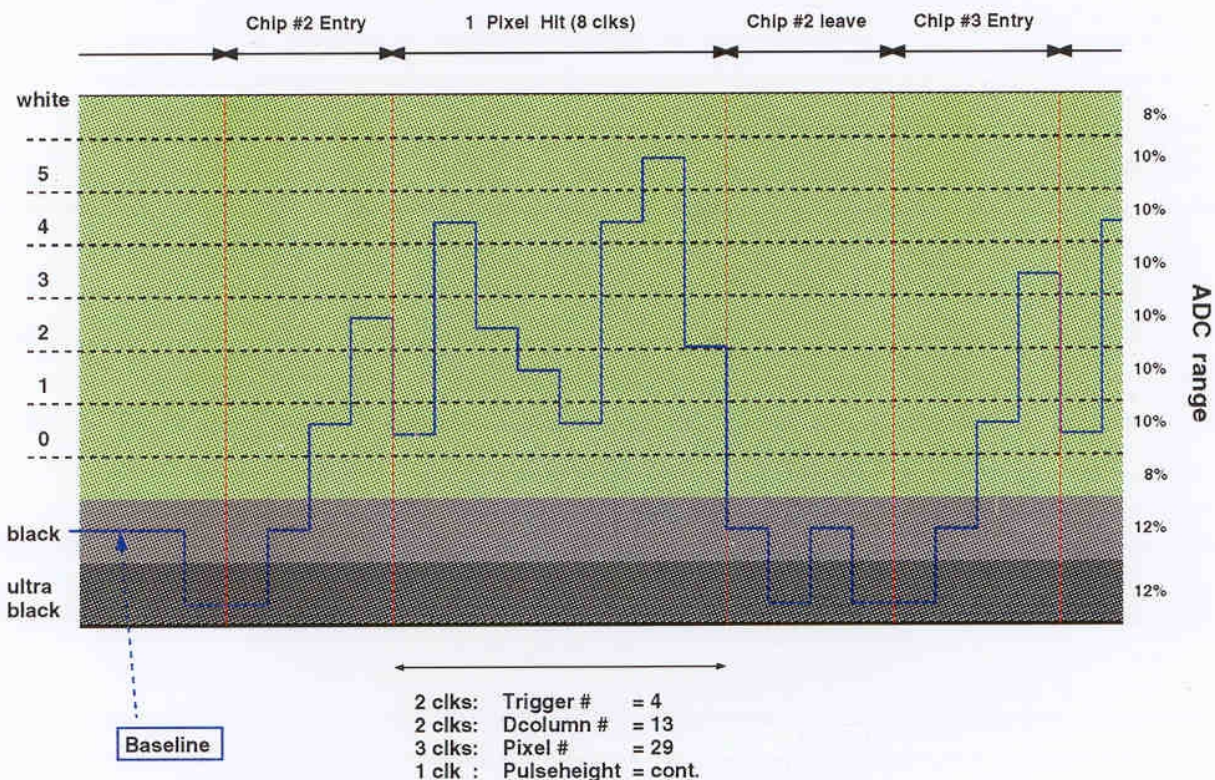
- Groups of 6 readout clocks for all records
 - fixed readout format for each pixel hit:
 1. Column number
 2. Column number
 3. Pixel Address
 4. Pixel Address
 5. Pixel Address
 6. Pixel Pulse Height
 - Begin of chip & end of chip record
 - TBM records
- use safe analog coding (5 & 6 valued)
 - > chip variation & rad. damage

Pixel Data Structure and ADC range

Alternative structure of signal composition !

like : TV-composite video signal

- Assume total range of 9 bits for analog coded data transmission.



- Baseline is at **black** level. TBM is guardian of token bit and keeps analog bus active to almost lowest level (black level) while waiting for the next readout scan (typ. 80% of time).

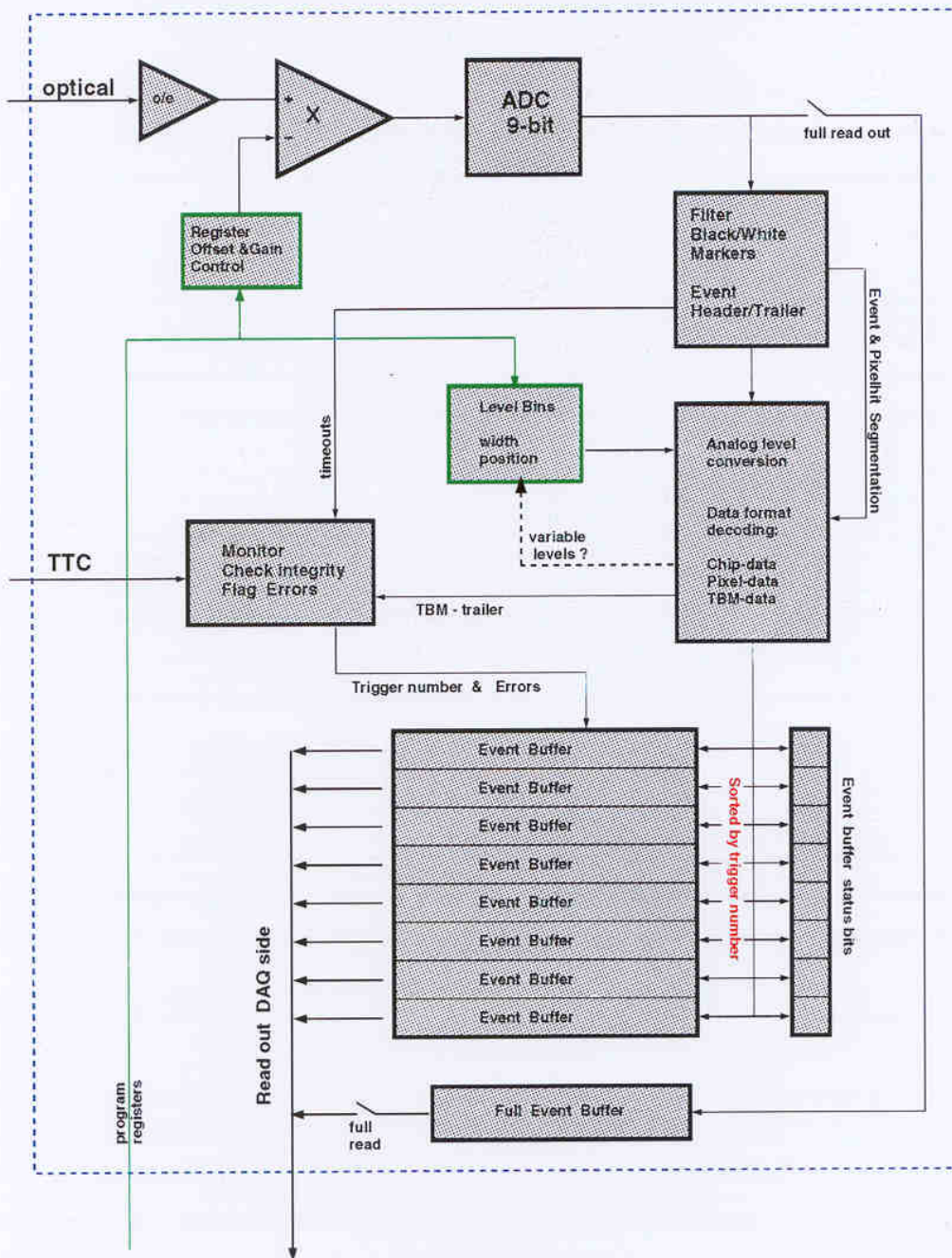
→ Laser drivers wait at almost lowest power levels for new event.

- For data segmetation use **ultra black** signal.

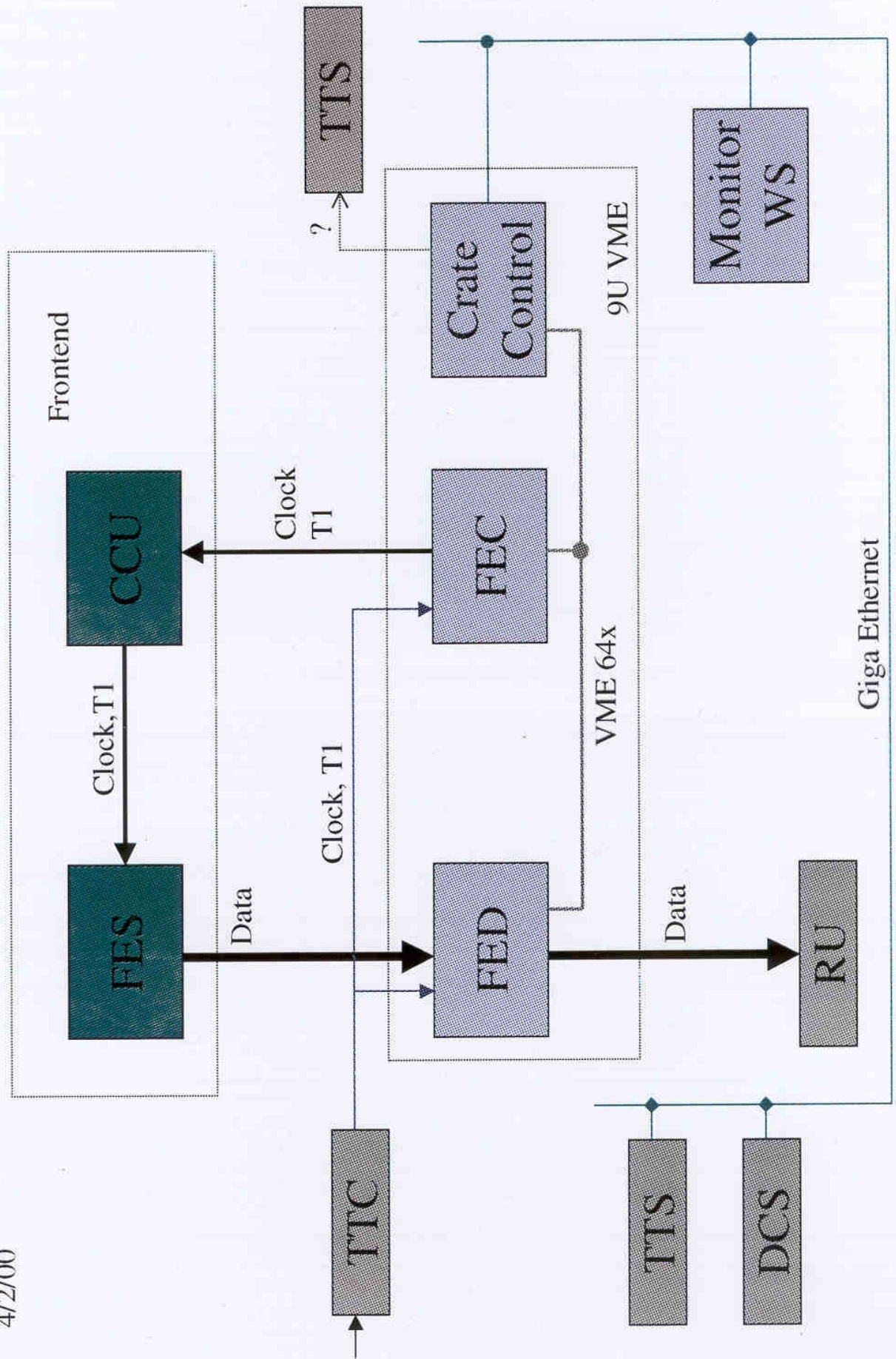
FED Module for Pixel Detector

- Zero suppression of pixel chip requires different FED module than APV readout!
- FED module for pixel readout performs Address & Timestamp Decoding of hits!

Conceptual schematic of pixel data flow in FED Module

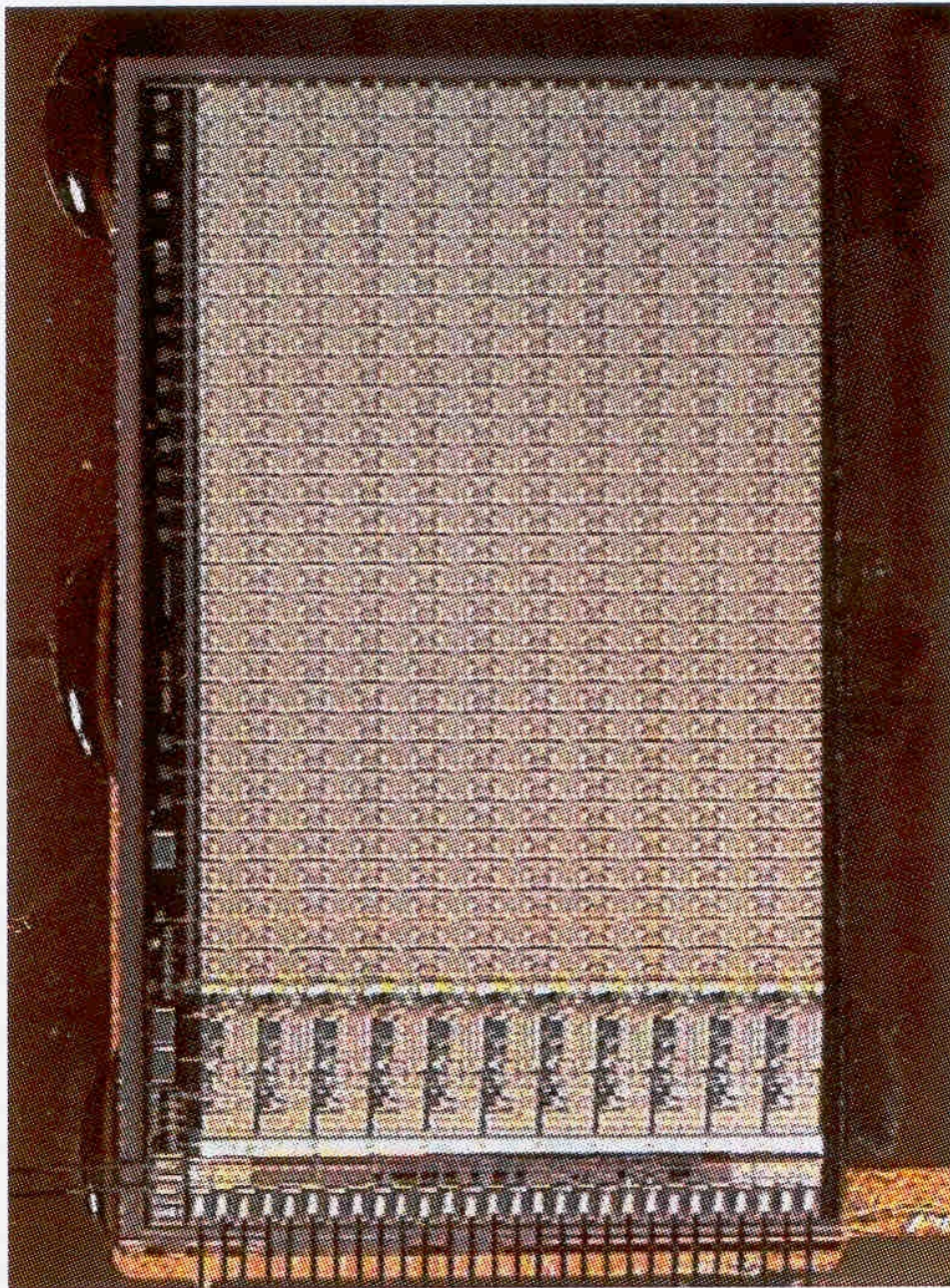


- Finite state machines for event decoding will be tested in separate VME prototype module with simplified DPM buffers.

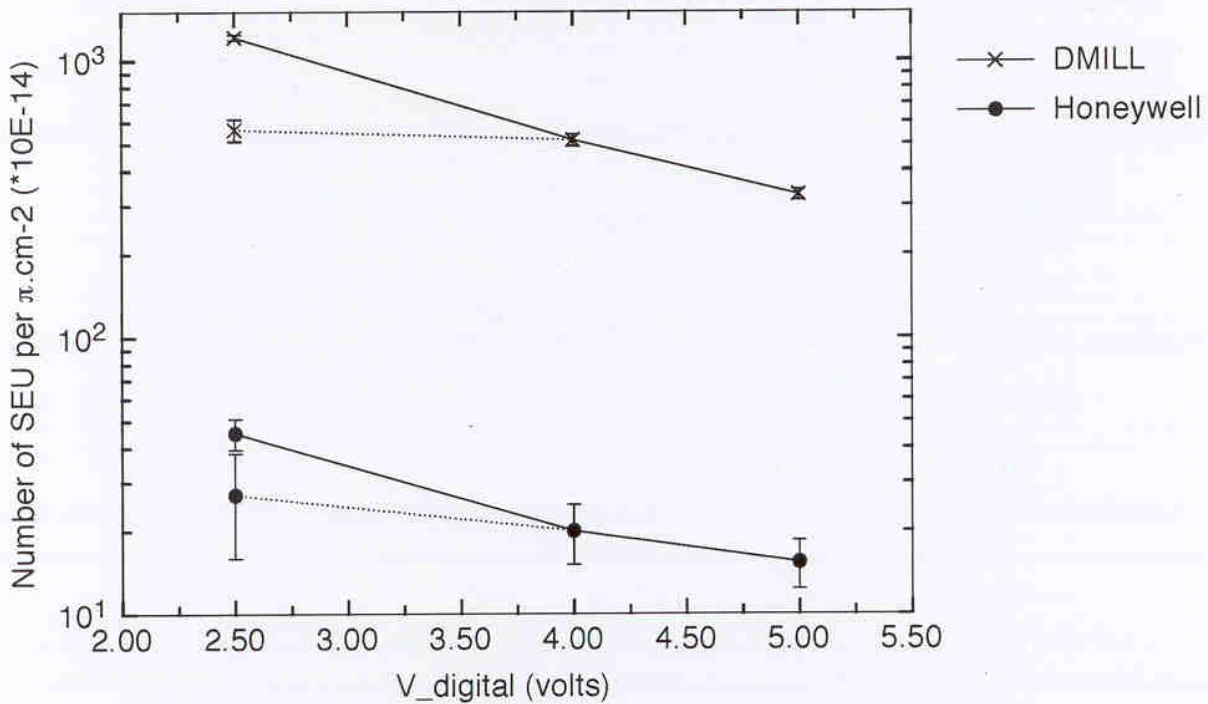


DMILL Read out chip 22x30 pixels

- Pixel size 125 μ m x 125 μ m
- Analog block with threshold trim (3-bit & mask)
- Reduced Architecture (1 timestamp/column)



Overview DMILL / Honeywell



- DMILL / Honeywell:
a factor 20 to 25 was found.

- Voltage dependency:
measurements at 2.5 Volts show an increase of a factor 3 to 4
when compared to measurements at 5 Volts.

Consequences

-> On chip calibration data (trimbits):

3 trimbit = 3 FF, 2.5 Volts.

8268 FF / chip.

At full luminosity, $r=7.5$ cm, $2 * 10^7$ $\pi / (\text{cm}^2.\text{s})$

$12 * 10^{-14}$ SEU / (FF. π .cm²)

1 FF \leftrightarrow $24 * 10^{-7}$ SEU / sec

for the chip?

=> $1.98 * 10^{-2}$ SEU / (chip.sec)

for the barrel, 7.5cm, high lum? (224 mod, 3584 chips)

=> 70 SEU / sec

when will 1% of the pixels lost?

after 22 minutes

=> Frequent download of information, manageable if necessary mechanism is foreseen.

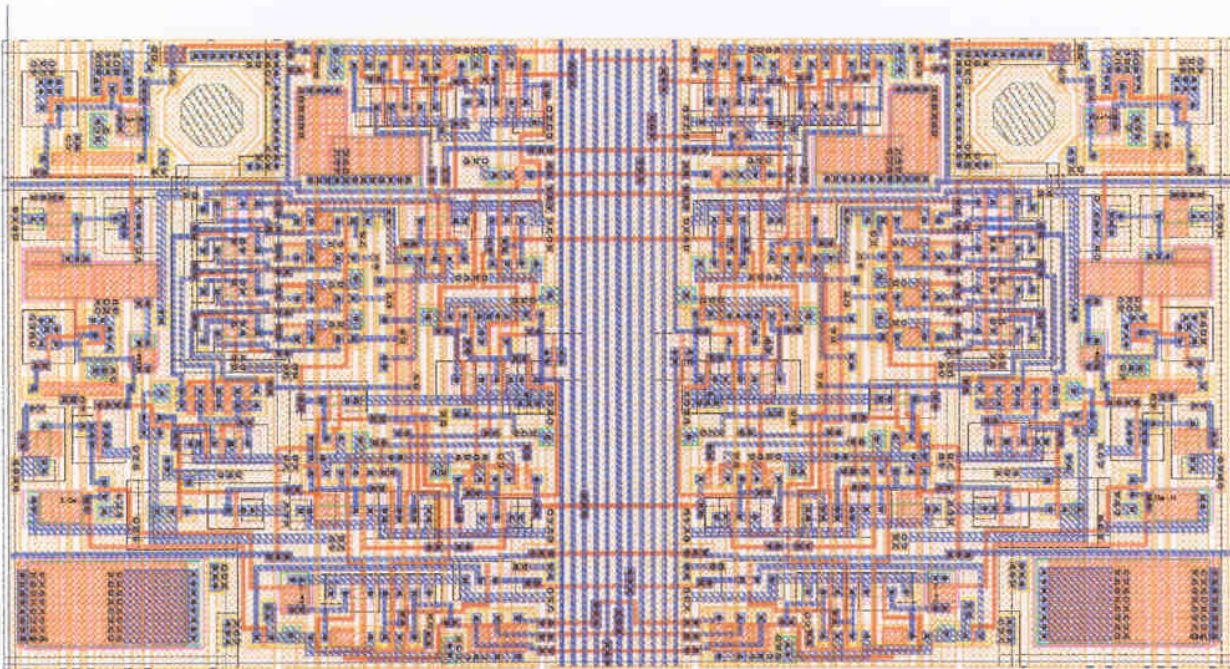
-> Digital control section:

needs to be studied.

=> reset of important blocks (?).

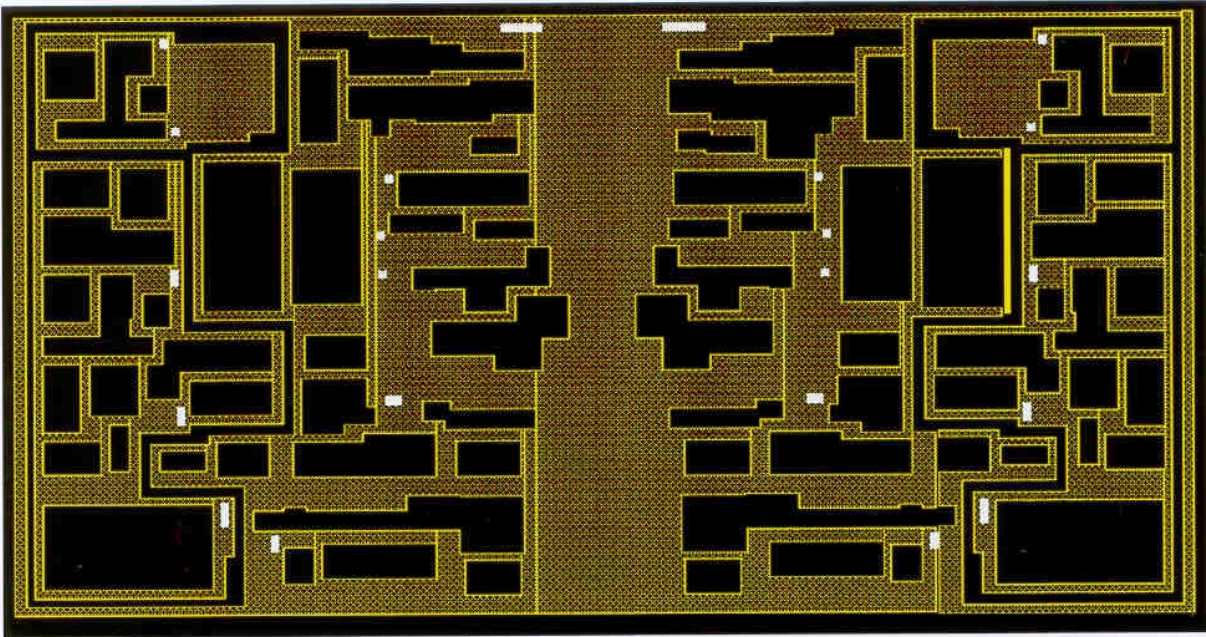
PIXEL UNIT CELL

- Complete Column Drain Architecture
- Cross talk skip mechanism → analog block
- Previous measurement < 700 erms

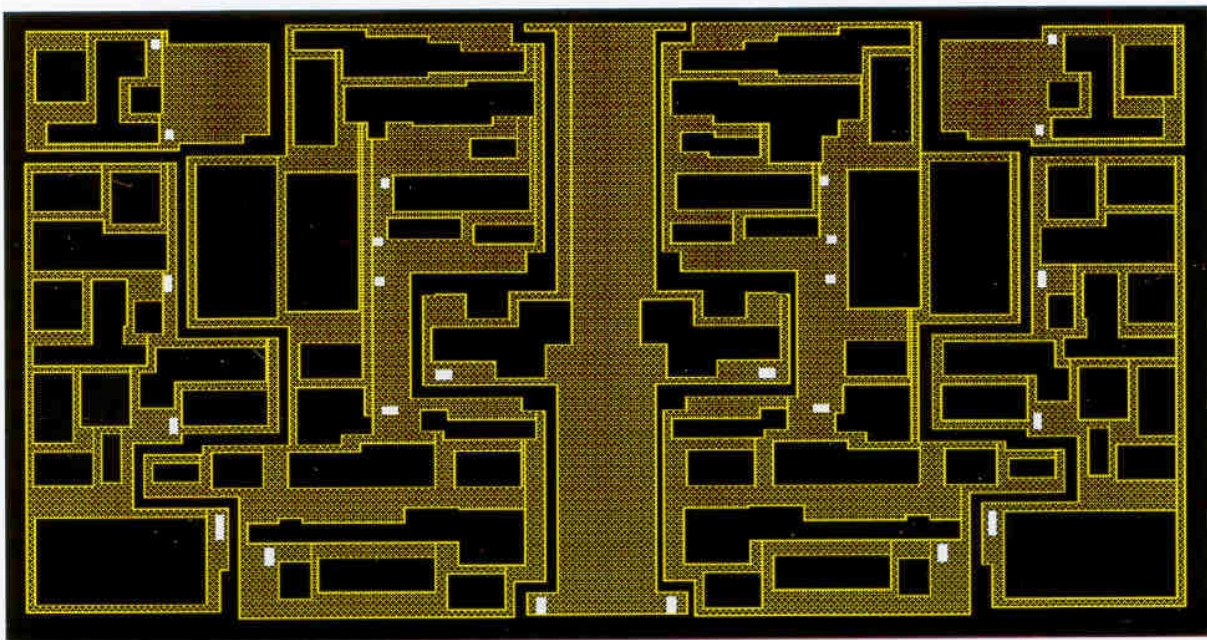


- Study this problem in detail (thesis R. Schnyder)
 - Measure resistance and capacitance of trenches
 - Try to model cross talk and back side silicon coupling
 - Compare different layouts and power routings

Coupling through "lost silicon"



Layout without and with trench between digital bus lines and analog block



Pixel Read Out Chip (ROC) size

R.S/R.H 991208

Column Periphery

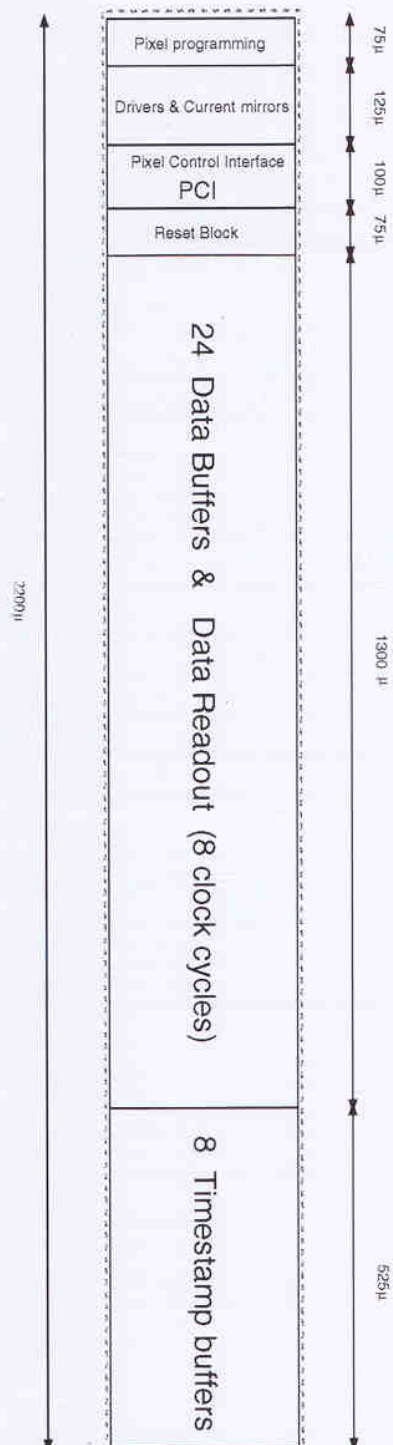
Width:

Frame & rim	=	75μ
52 pixel of 150μ	=	7800μ
Pixel programming	=	35μ
Frame & rim	=	75μ
Total	=	7950μ

Height:

Frame & rim	=	75μ
53 pixel of 150μ	=	7950μ
Column periphery	=	2200μ
Control & Interface	=	450μ
Supply Bondpads	=	200μ
Frame & rim	=	75μ
Total	=	10950μ

ROC Area = 87.05 mm²



Conclusion and Outlook

- New Preamplifier/Shaper shows improved performance.
- Many blocks for the column periphery designed and tested.
- Layout constraint in maximum size fulfilled.
- SEU measurements indicate that for DMILL and Honeywell safe operation requires some precautions, but no major system changes.
- Design of final chip very advanced
Production mid July