

Fabrication of ATLAS pixel detector prototypes at IRST

M. Boscardin, G.-F. Dalla Betta, P. Gregori, M. Zen, N. Zorzi

Centro per la Ricerca Scientifica e Tecnologica (ITC-irst),
Località Pantè di Povo, 38050 Trento, Italy

Outline

- Introduction
- Description of the fabrication technology
- Fabrication of 1st and 2nd prototypes:
experimental results and problems
- Conclusions

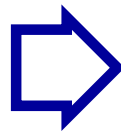
Introduction

- In the last few years, IRST has been involved in the development of silicon microstrip detector technologies within an R&D project supported by INFN.
- Starting from fall 1998, we have fabricated silicon pixel detectors oriented to the ATLAS experiment (prototypes 1 and 2).
- We present the main processing issues and report some selected results from the electrical characterization of detectors and test structures carried out before detector delivery.

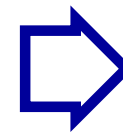
Process/Layout Constraints

PROCESS

IRST microstrip
technology
p-stop



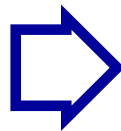
n-on-n pixel detector
isolation with p-spray
(or moderated p-spray)



develop
a new process

LAYOUT RULES

IRST microstrip tech.
no overlap between
n&p regions



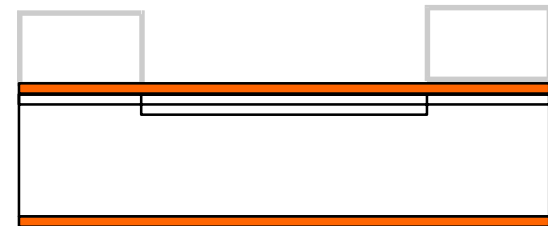
BIAS dot
overlap n⁺-region and p⁺-region
overlap contact hole and n⁺- region

Process Flow (1/3)



initial oxide growth (200nm)
p-spray implantation
B 4.5E12 70KeV

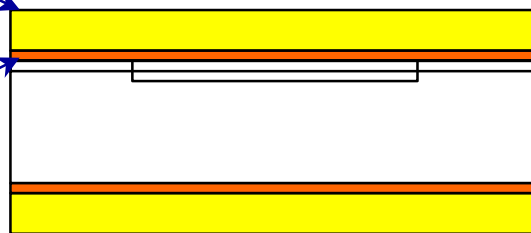
define moderated p-spray
moderated p-spray implantation
B 4.5E12 70KeV



resist

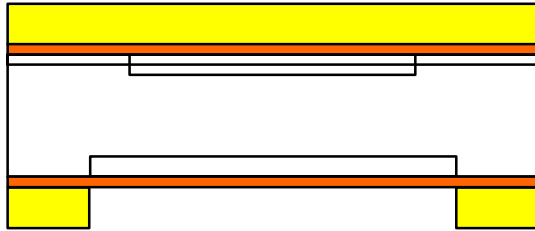
TEOS

termal oxide



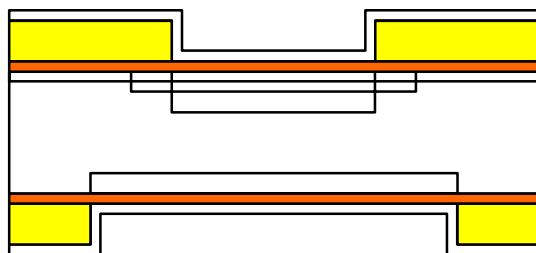
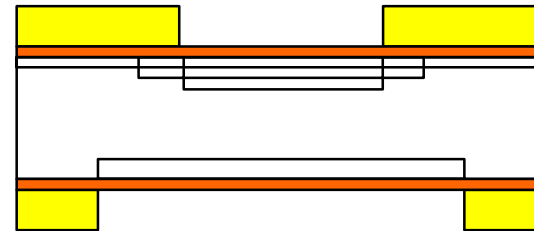
TEOS deposition (800nm)

Process Flow (2/3)



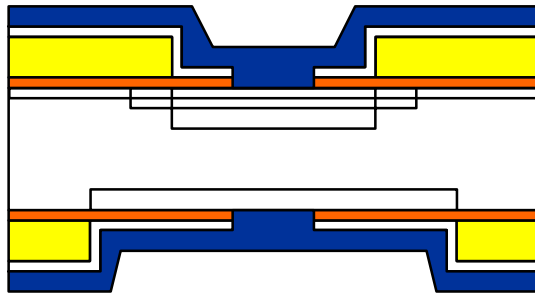
define p⁺ region
implant oxide growth (40nm)
p⁺ implant (B 5E14 70KeV)

define n⁺ region
p⁺ drive-in (900°C in dryO₂)
n⁺ implant (P 5E15 120KeV)



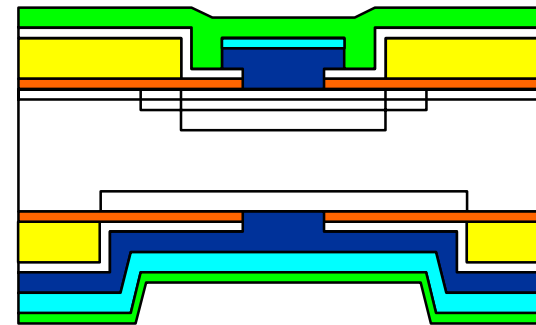
n⁺ drive-in (975°C in dryO₂)
TEOS deposition (300nm)
low temperature annealing

Process Flow (3/3)



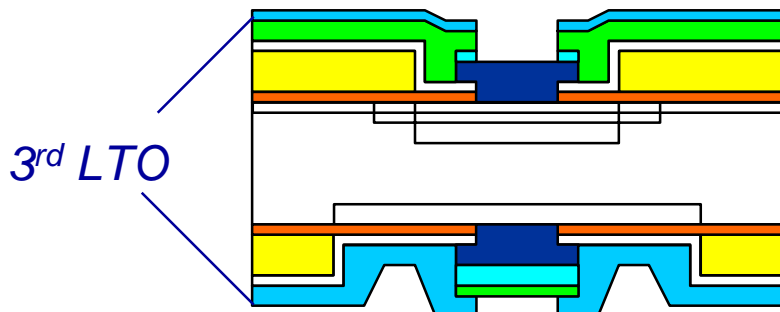
define and open contact holes (n&p side)
metal deposition (1 μ m Al 1%Si)

1st LTO deposition (500nm)
define metal (n-side)
etch LTO and metal
2nd LTO deposition (500nm)



1st LTO

2nd LTO



3rd LTO

define metal (p-side)
etch LTO and metal
3rdLTO deposition (500nm)
define and open passivation (n&p side)
sintering

Detector Fabrication: critical steps

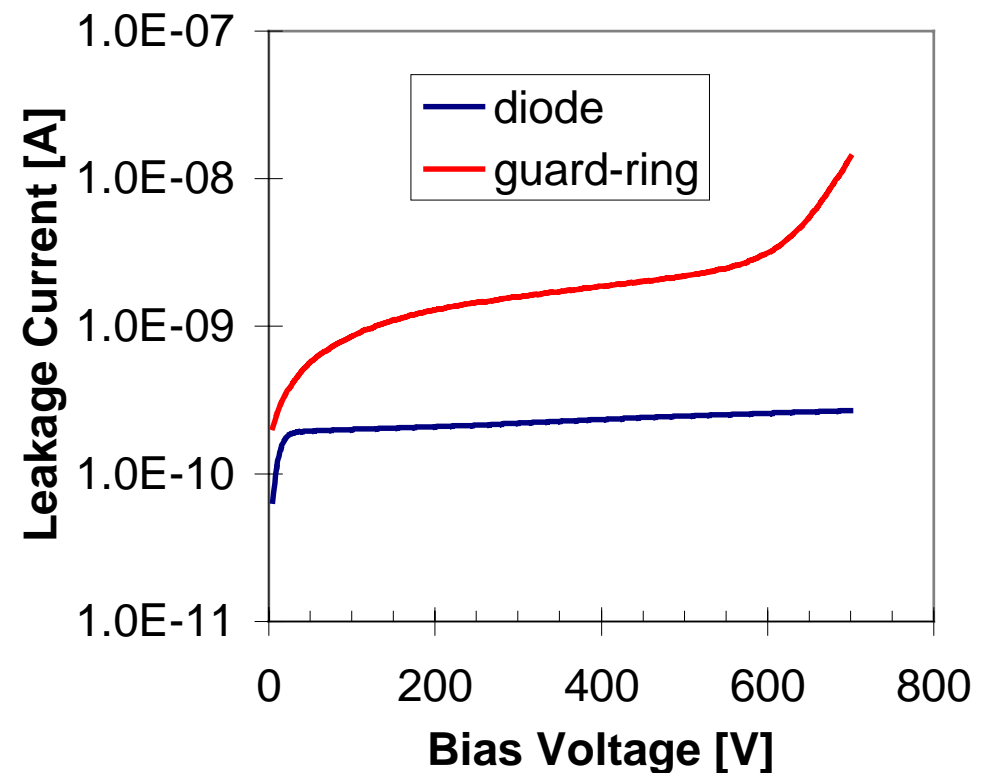
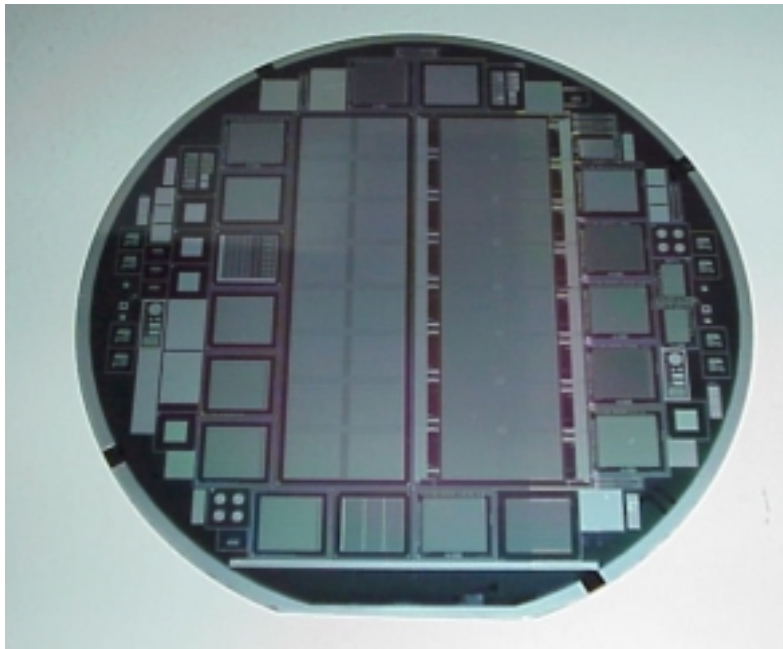
- moderated p-spray** two separate implantations
p-spray = blank
+ moderated p-spray = p-stop like
- p⁺ and n⁺ region** implantation through a screen oxide
using a thick oxide layer as implant mask
- low temperature annealing** increase gettering efficiency
- metal and passivation** LTO oxide to protect metal layer

Prototype 1: Experimental results

Test Structures

diode 4mm^2 $I_{\text{leak}} \cong 300\text{pA}$ @ full depletion

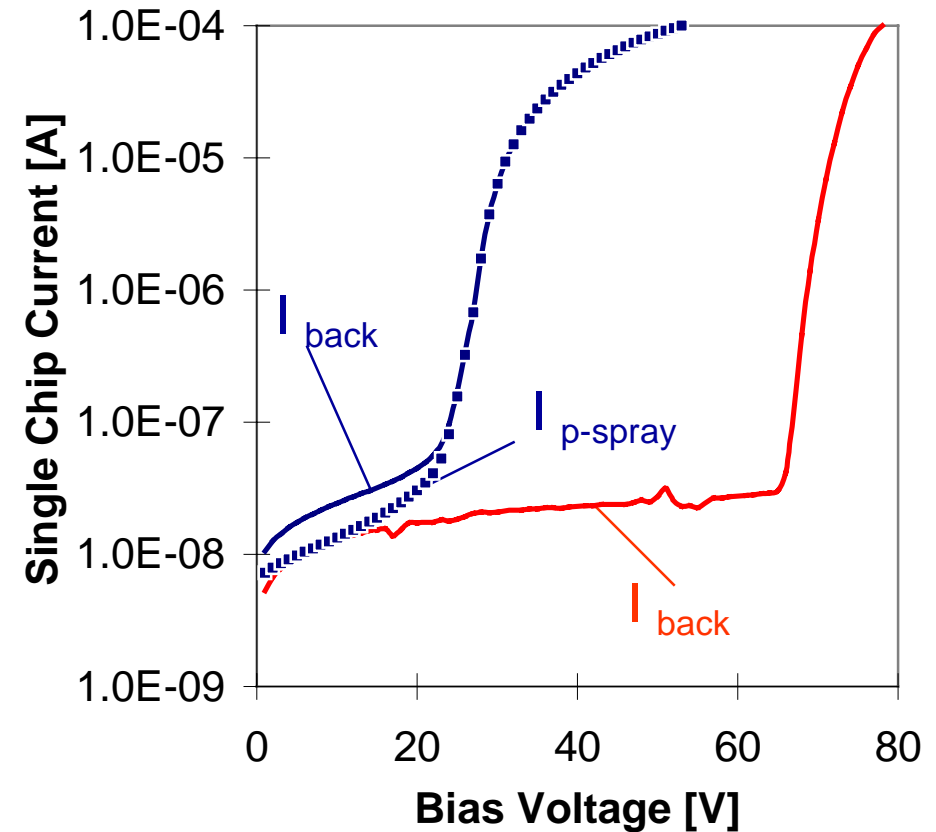
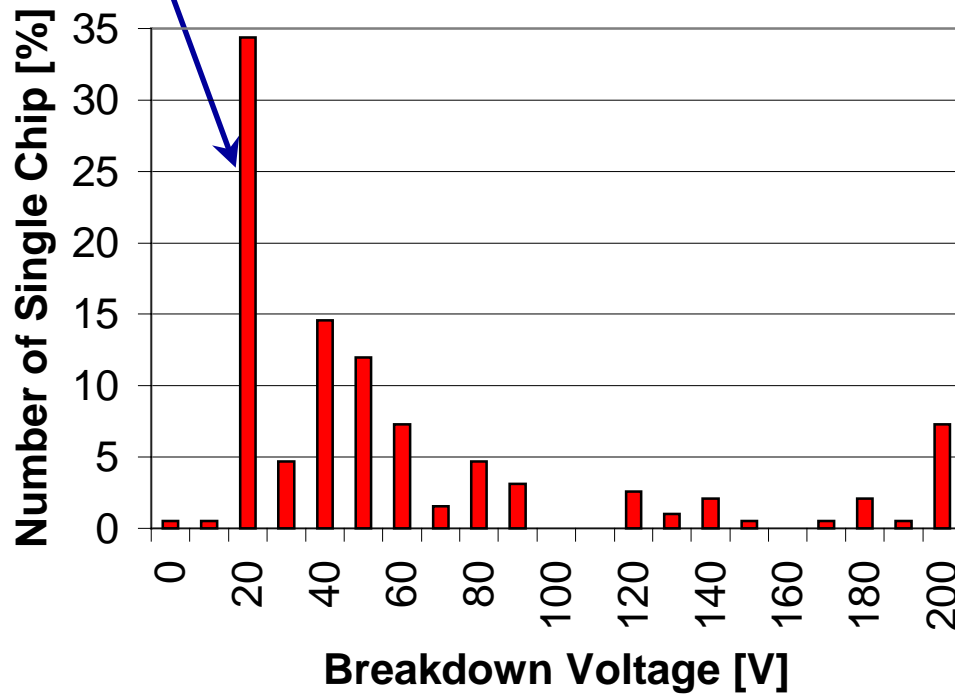
gated diode $s_0 \cong 30\text{ cm/sec}$



IV curves of multiguard diode
(area 2.2mm^2)

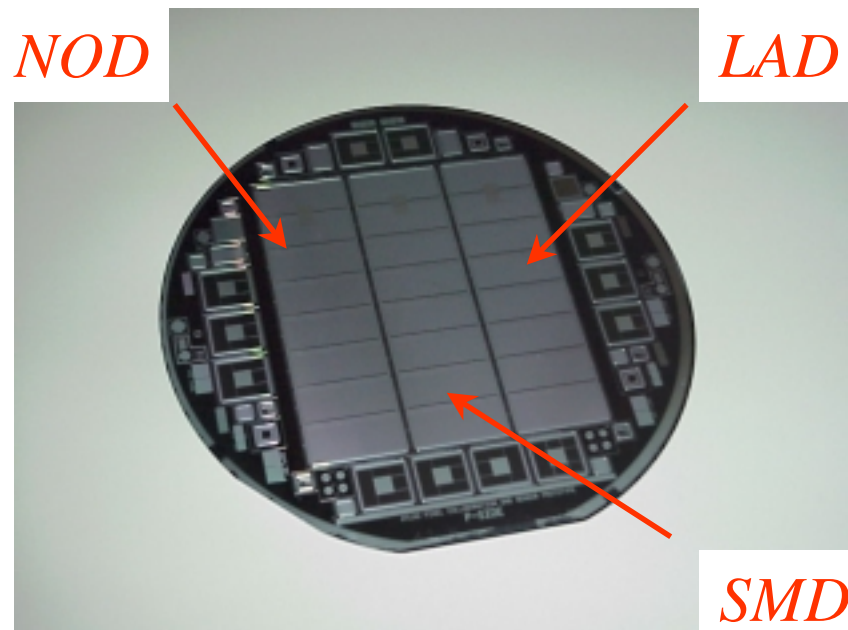
Prototype 1: Experimental results

V_{bk} at low voltage (about 20V)
probably due to a misalignment
between contact and n-diff region



I_{back} , $I_{p-spray}$ with p-spray @ $V=0$
 I_{back} with p-spray floating

Prototype 2: Experimental results



layout

overlap between contact
and n⁺ region = 2,5 μm

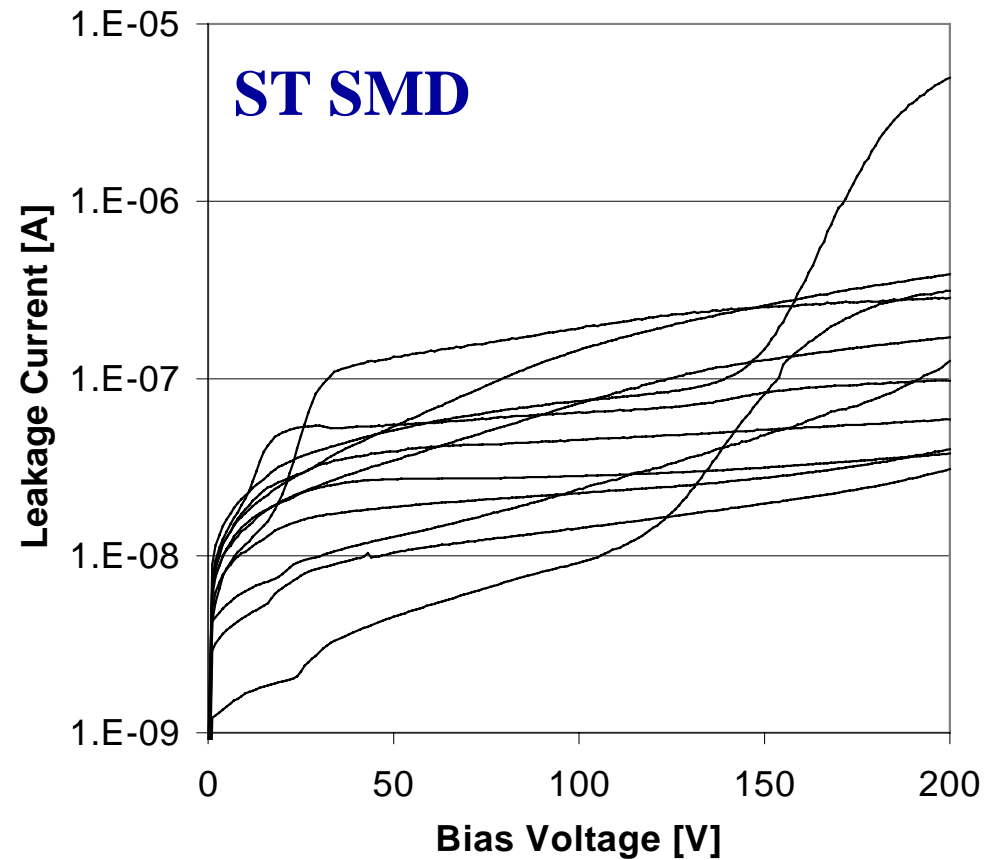
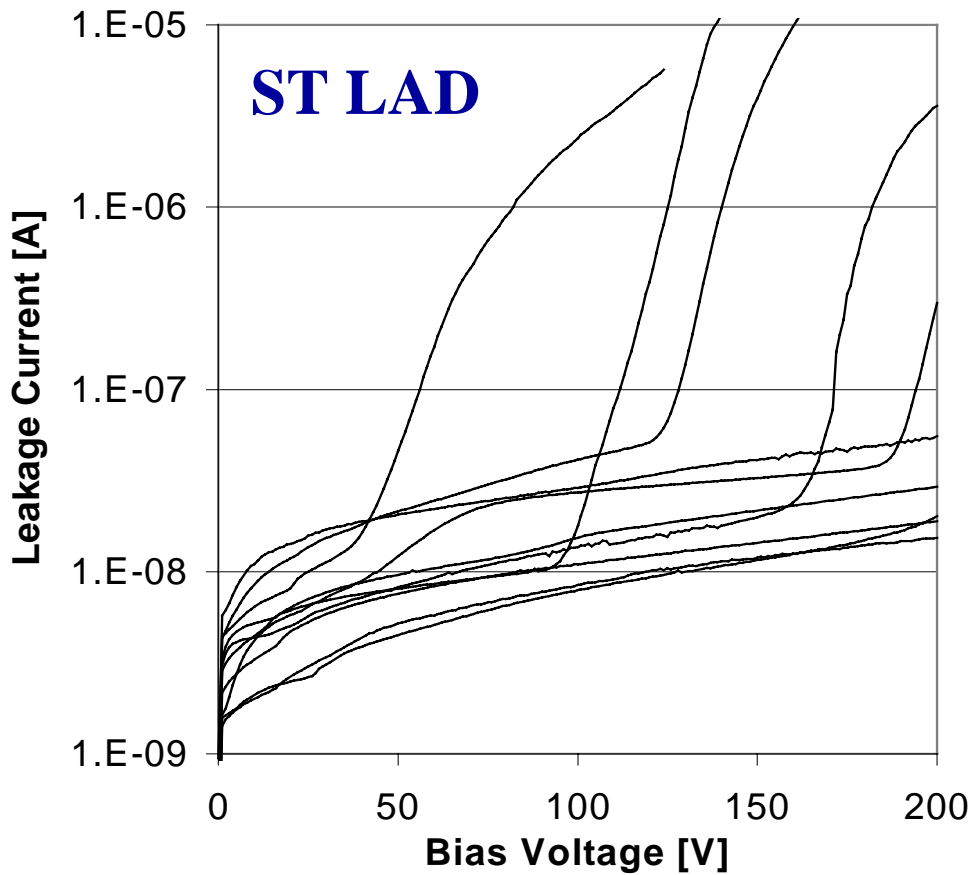
leakage current

on single chip (ST SMD)

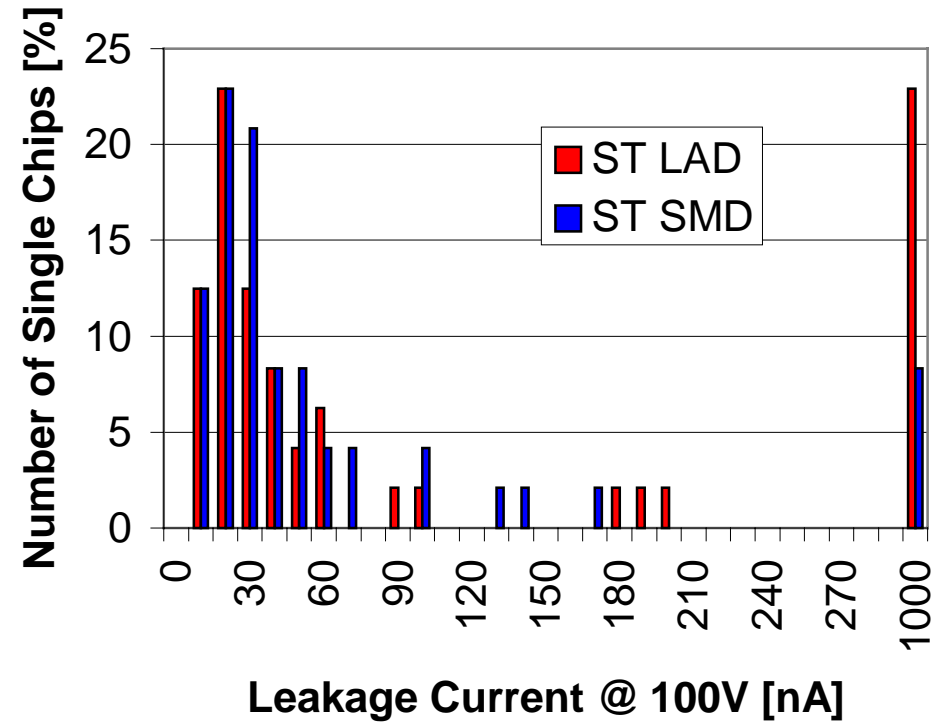
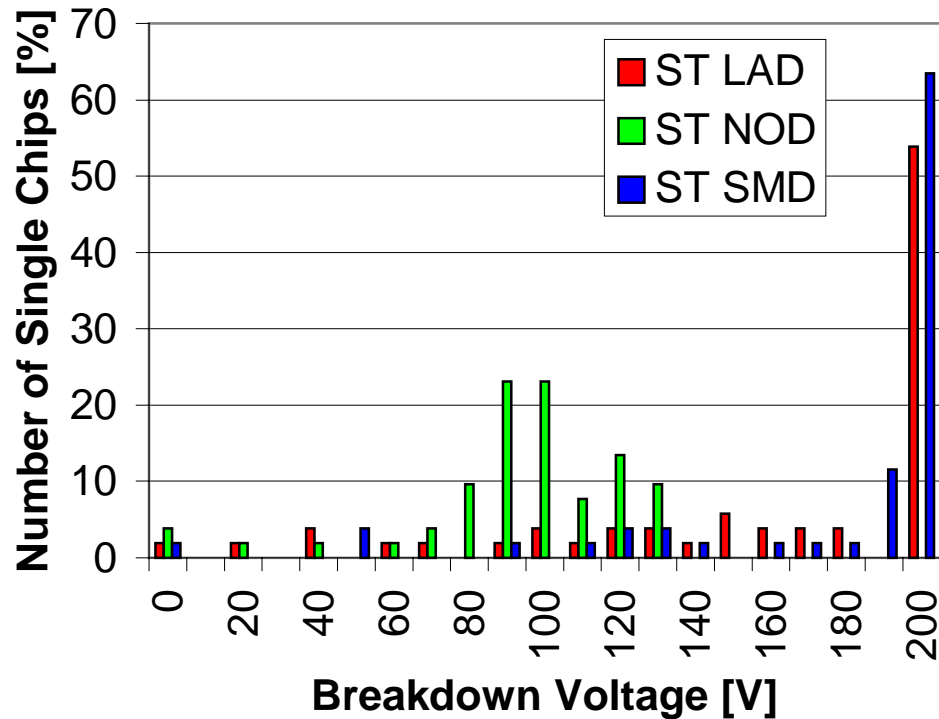
$$I_{\text{leak}} \cong 7.5\text{nA @ } 50\text{V}$$

To increase the **radiation hardeness** of detectors, wafers have been **oxygen enriched** via a dedicated process step (24h oxidation process at 1150°C).

Single Chip: IV curves



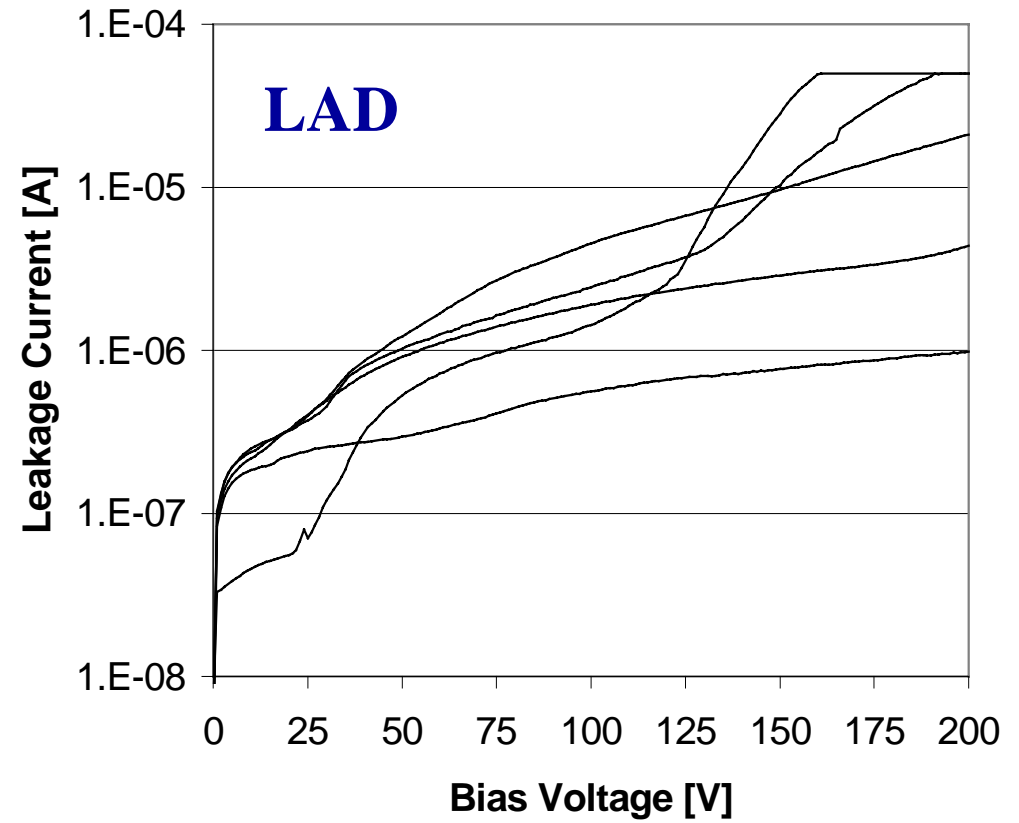
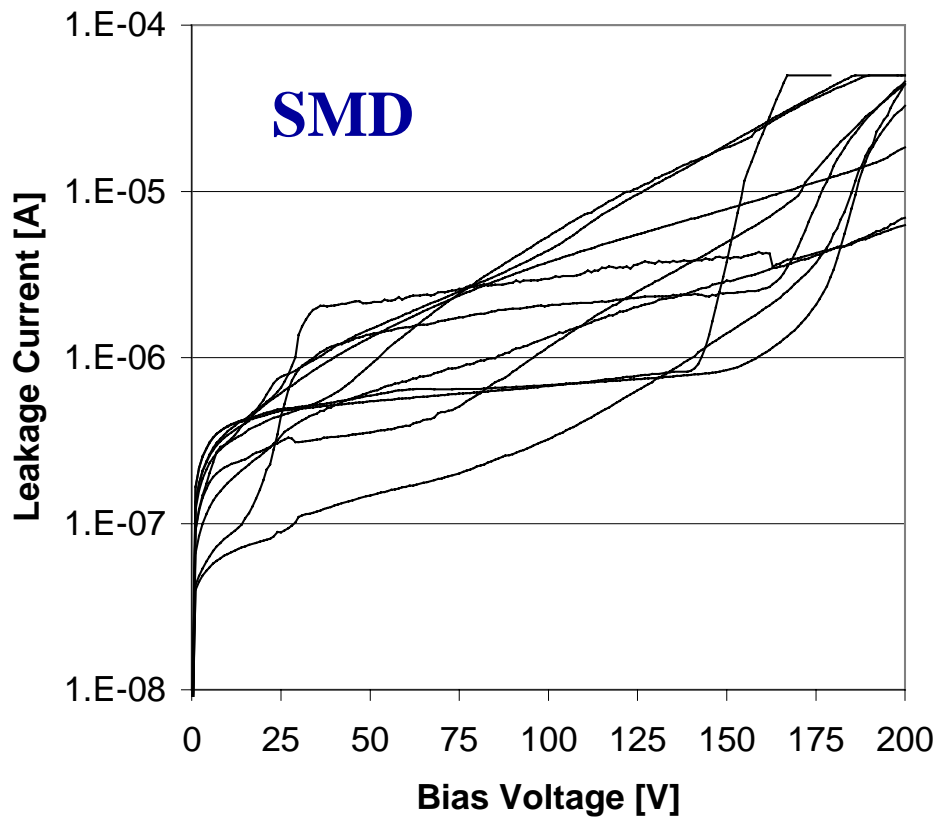
Single Chip: V_{BK} & I_{leak} distributions



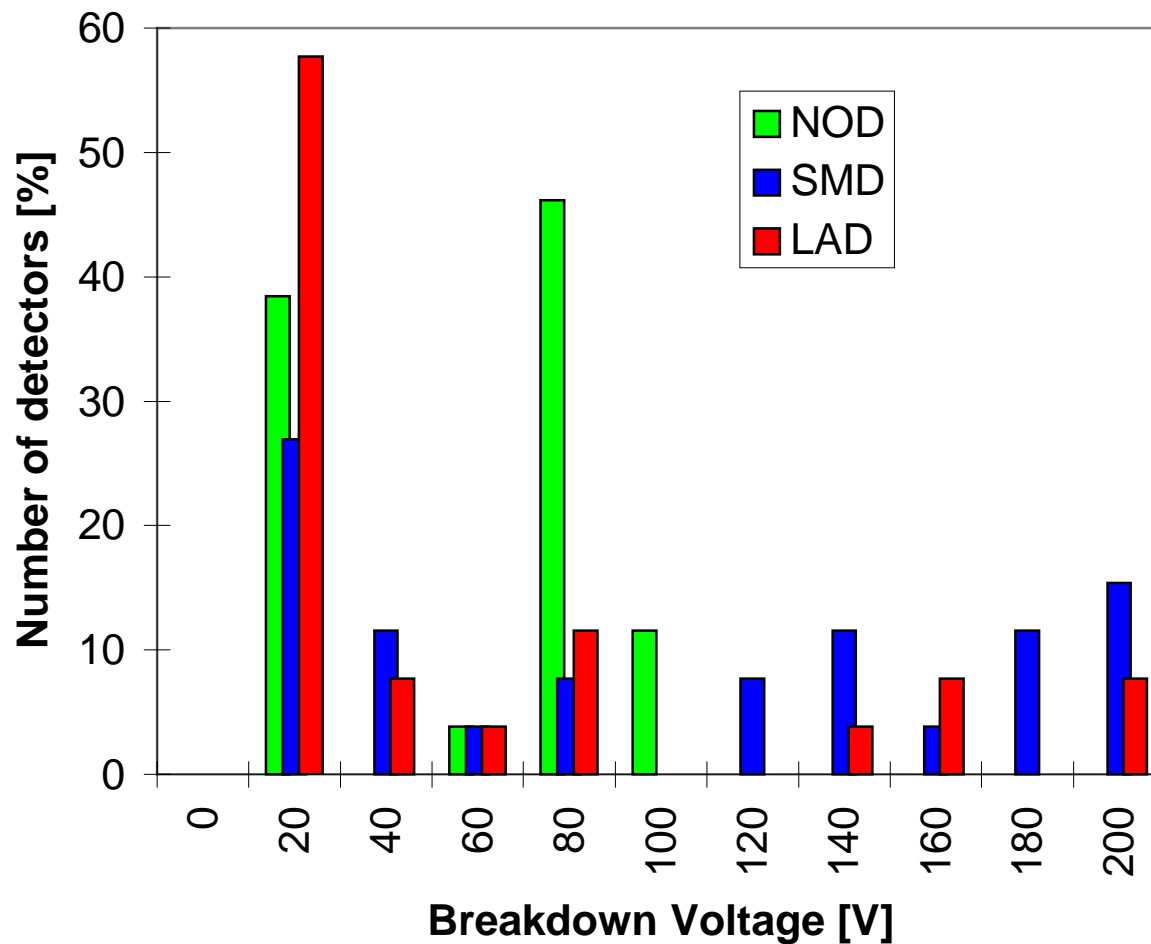
Breakdown of ST NOD < 140V

Average Leakage Current
@ 100V of ST SMD & LAD
about 30 nA

Tiles: IV curves



Tiles: Breakdown Voltage Distributions



Tiles with a $V_{BK} > 150V$

NOD	0
SMD	8
LAD	4

Tiles with a $V_{BK} = 20V$

NOD	10
SMD	7
LAD	15

Conclusions

- We have processed some prototype batches of silicon pixel detector oriented to the ATLAS experiment.
- To this purpose, a dedicated technology has been developed.
- The electrical characterization of single chips and related test structures have evidenced that IRST technology is potentially adequate for the fabrication of these detectors.
- However, results from tiles measurements have shown that the number of process-related defects should be decreased in order to fulfill the detector specifications (in particular in terms of breakdown voltage) with a satisfactory fabrication yield.