

## Pixel Detector for the Protein Crystallography Beamline at the SLS

### PSI

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## Data collection in protein crystallography

### Spot size:

- Beam divergence
- Mosaicity of the crystal
- Distance sample-detector
- Point spread function of detector

### Crystal rotation

- 30-180 degree for complete data set
- Currently: Discrete rotation, integration over certain rotation angle
- Future: Continuous rotation, integration determined by detector frame rate (**Fine phi slicing**)

Crystallized Protein

Beam

### Beam

Energy: 5-17.5 keV  
Intensity: ~10 /s  
Focal spot size: Adjustable to 25 x 15 μm  
Divergency: 150 μrad x 28 μrad (FWHM)

### Diffraction data

- reflect crystal symmetry group
- orientation of the crystal → orientation matrix
- High dynamic range: >10 between strong and weak reflections
- Intensities need to be determined accurately (1%)
- Determination of amplitudes and phases leads to electron density maps

### Resolution:

$$2d \cdot \sin(\theta) = \lambda$$

For  $d=1\text{\AA}$  and  $\lambda=1\text{\AA}$ ,  $\theta=60^\circ$

Diffacted beam

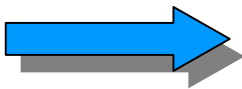
X-ray Detector

Diffraction pattern

$\theta$

### Detector requirements:

- Large area (40 x 40 cm) and/or large number of pixels
- Detect a high number of reflection orders (>500)
- Accurate determination of integrated intensities
- Wide dynamic range (>16 bit, i.e. single photon counting detector)
- Fast readout (<0.1s)

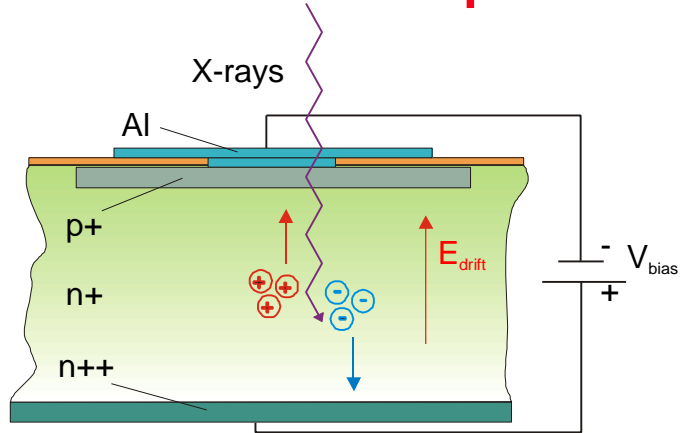


# Pixel Detectors

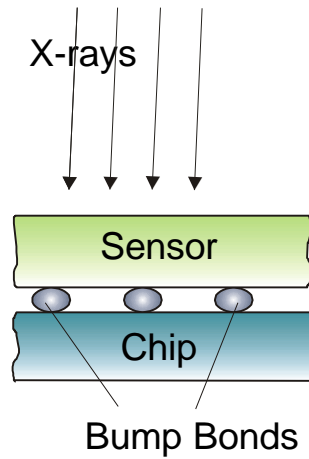
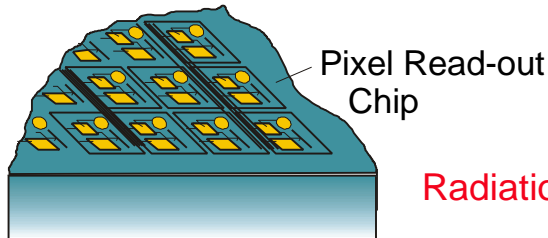
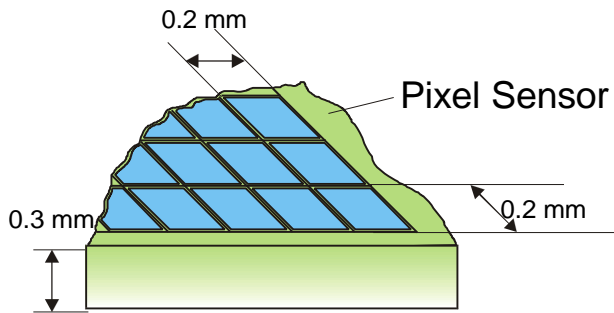
# Pixel Detectors: Principle

## Si pn-junction

3.6 eV to create 1 eh-pair

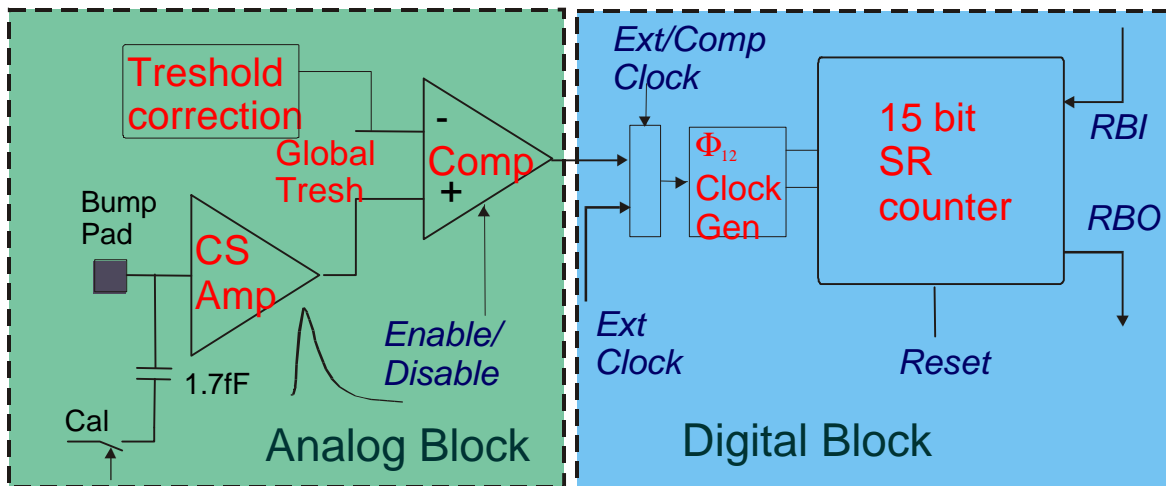


## Detector



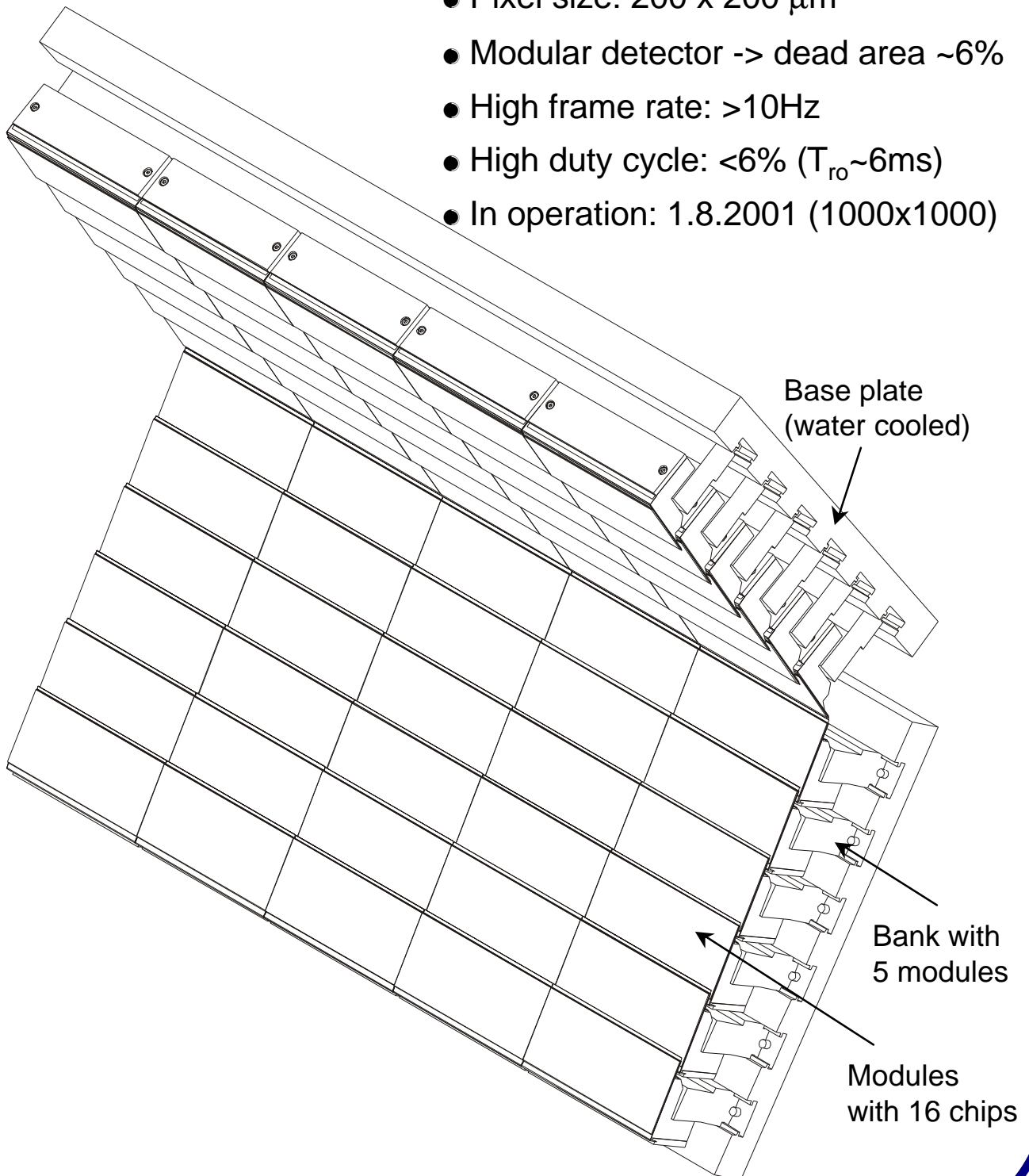
Radiation hard

## Pixel electronics

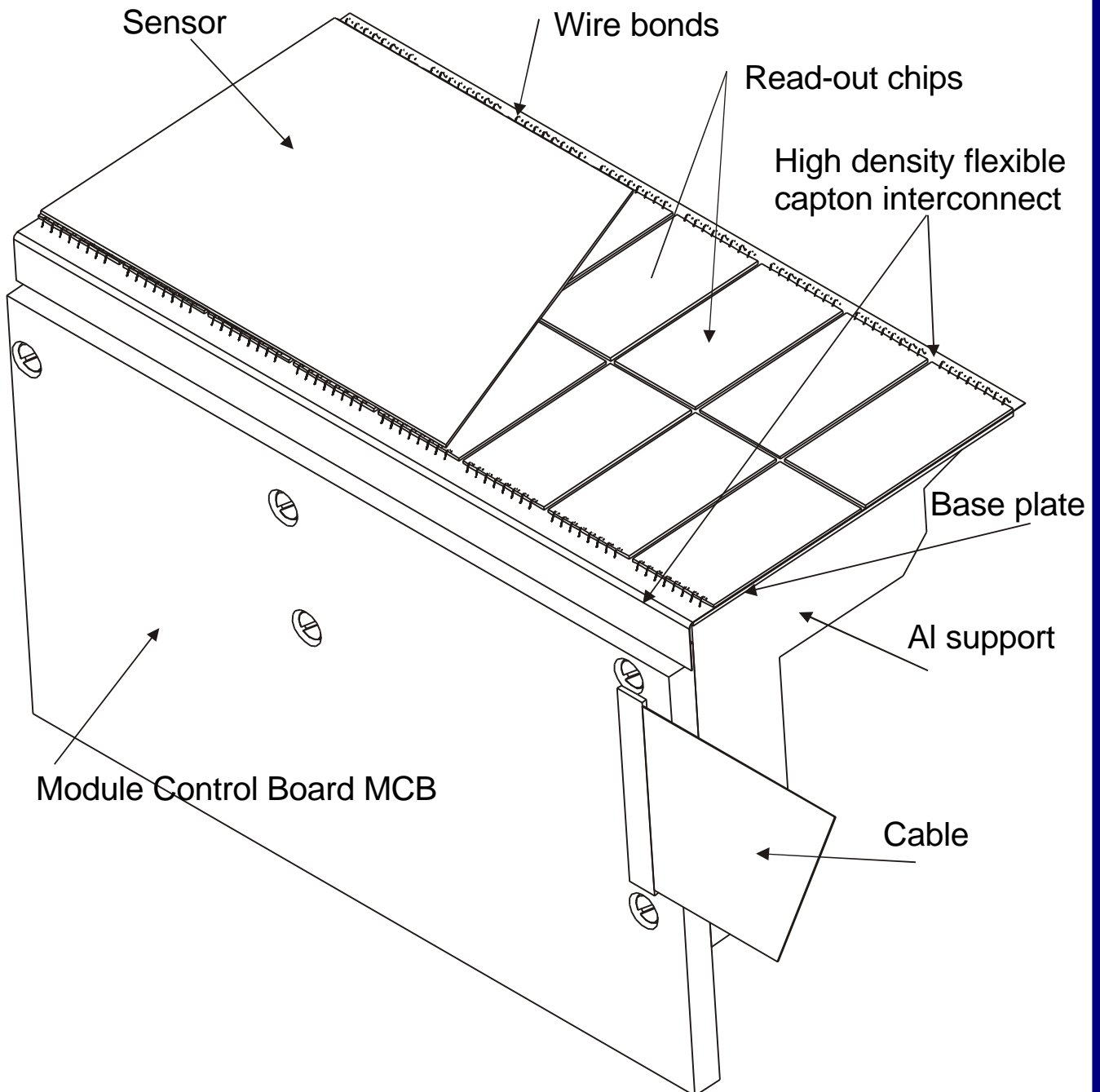


## The SLS Pixel Detector

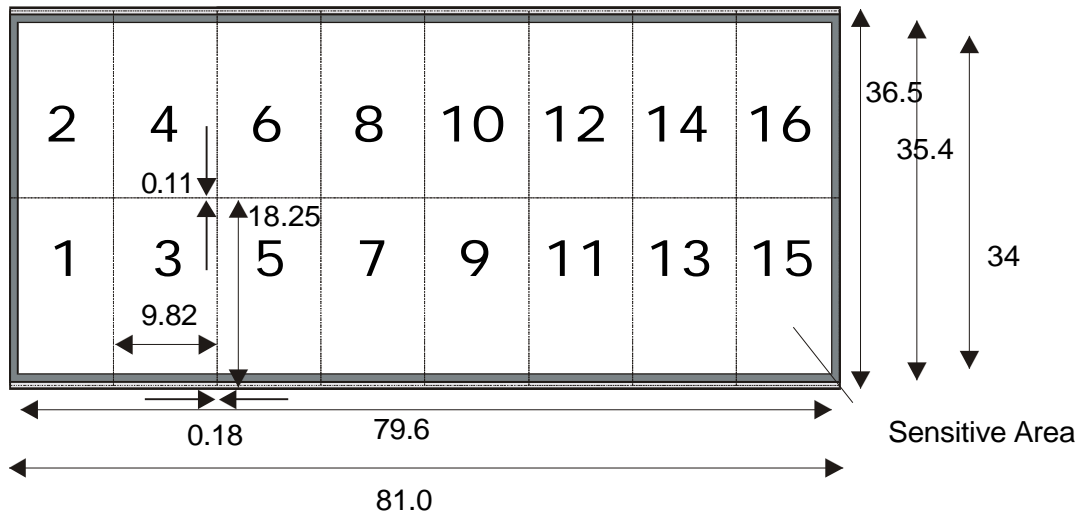
- Size: 40 x 40 cm<sup>2</sup> (0.16m<sup>2</sup>)
- 2000 x 2000 pixels
- Pixel size: 200 x 200 μm<sup>2</sup>
- Modular detector -> dead area ~6%
- High frame rate: >10Hz
- High duty cycle: <6% (T<sub>ro</sub>~6ms)
- In operation: 1.8.2001 (1000x1000)



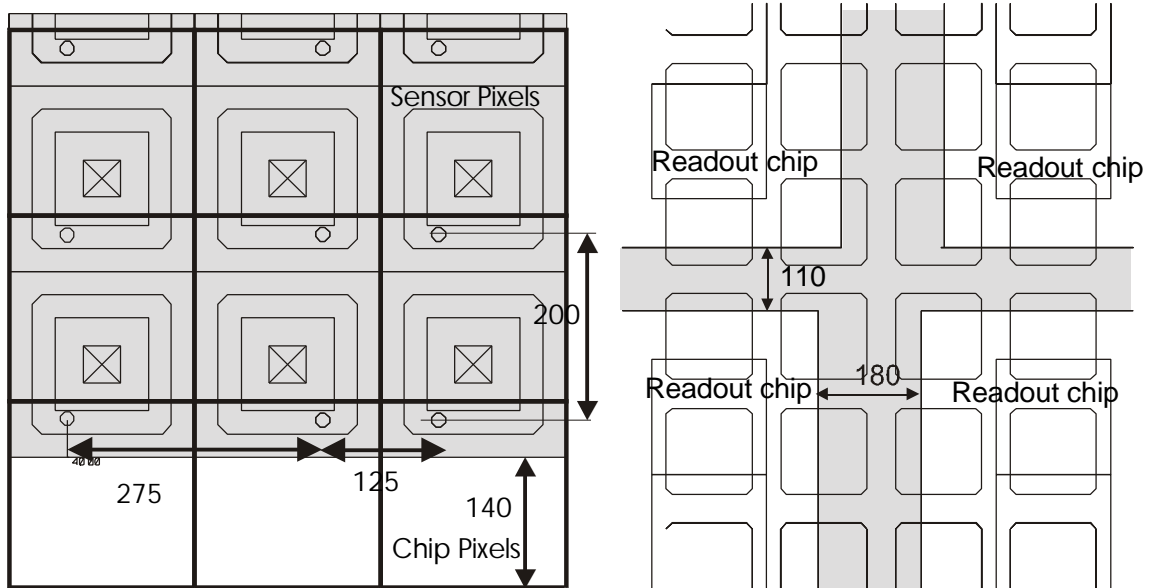
## SLS Pixel Module



## Module Geometry



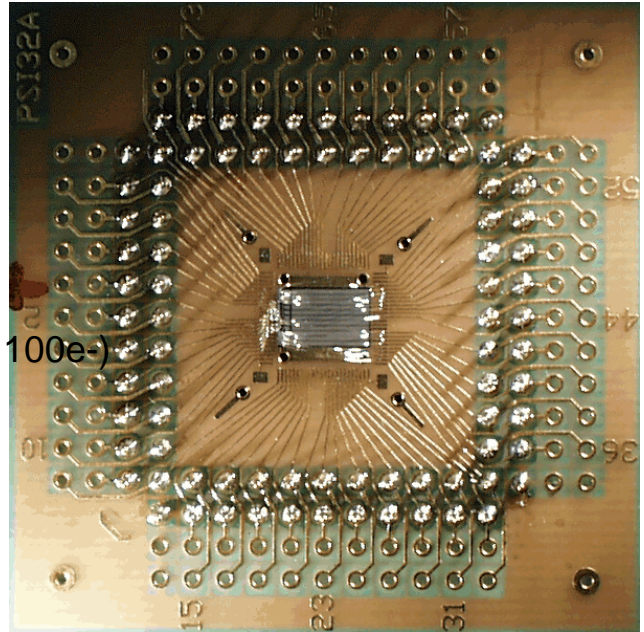
	Horizontal	Vertical		Total	
Pixel size	0.2	0.2	mm	0.04	mm <sup>2</sup>
Chip Nr of pixels	48	85		4080	
Chip size	9.82	18.25	mm	179.215	mm <sup>2</sup>
Sensor Nr of Pixels	398	170		67660	
Nr of double pixels	14	170		2380	
Sensor active area	79.6	34		2706.4	
Module outside dim	81	36.6	mm	2964.6	mm <sup>2</sup>



## Read-out electronics

### Main parameters

- Low noise analog block (ENC tot < 100 e<sup>-</sup>)
- Shaping time  $t_{sh} = 100 \text{ ns} \rightarrow 1 \text{ MHz}$
- Radiation tolerant
- power consumption < 100  $\mu\text{W}/\text{Pixel}$
- Robust comparator
- Individual threshold adjustment
- Low overall threshold variation ( $\sigma < 100e^-$ )
- 15 bit pseudo random counter
- Large size (20 x 10 mm<sup>2</sup>)



### Prototypes

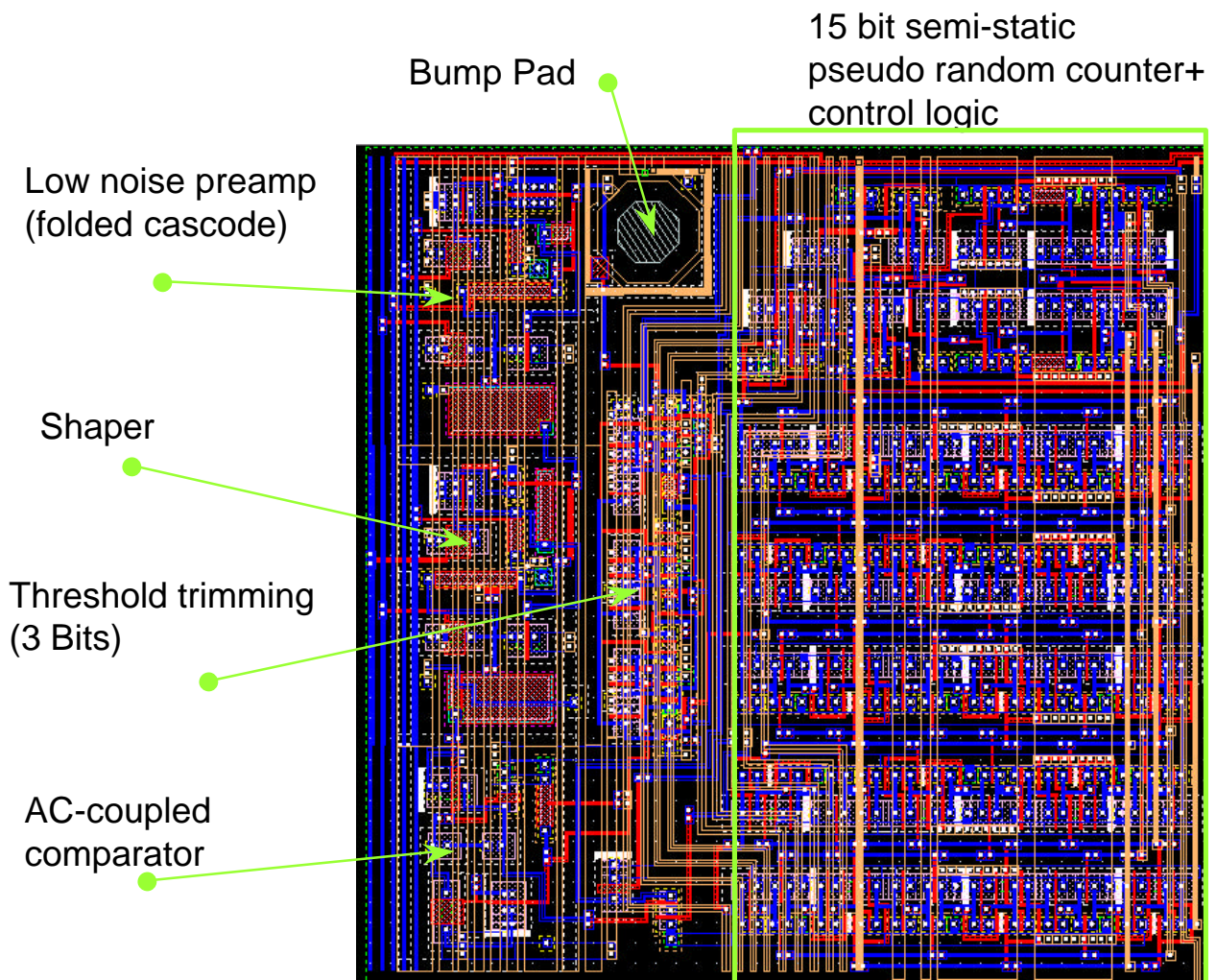
Name	Size	Pixel Architecture	Chip Architecture	Subm.	Receiv.
SLS01	8x2 array	Analog, comparator, counter	-	Dez 98	April 99
SLS02	22 x 30	Analog, <b>comparator!</b> , counter, trimbits	Indiv. Column architecture	May 99	Nov 99
SLS03	1 x 90	As SLS02, final length column	-	Aug 99	Mar 00
SLS04	22 x 30	As SLS02 but with correct comparator	As SLS02	Dez 99	Exp May 00
SLS05	30 x 30	As SLS04, improved trimbit mechanism	Indiv. Pixel Architecture (Yield tolerant design)	Feb 00	Exp July 00
SLS06 (Final chip)	48 x 85	As SLS05	As SLS05	Exp Oct 00	Exp Feb 01



## Pixel Layout

Designed in radiation hard DMILL technology (R. Baur, Ch. Brönnimann)

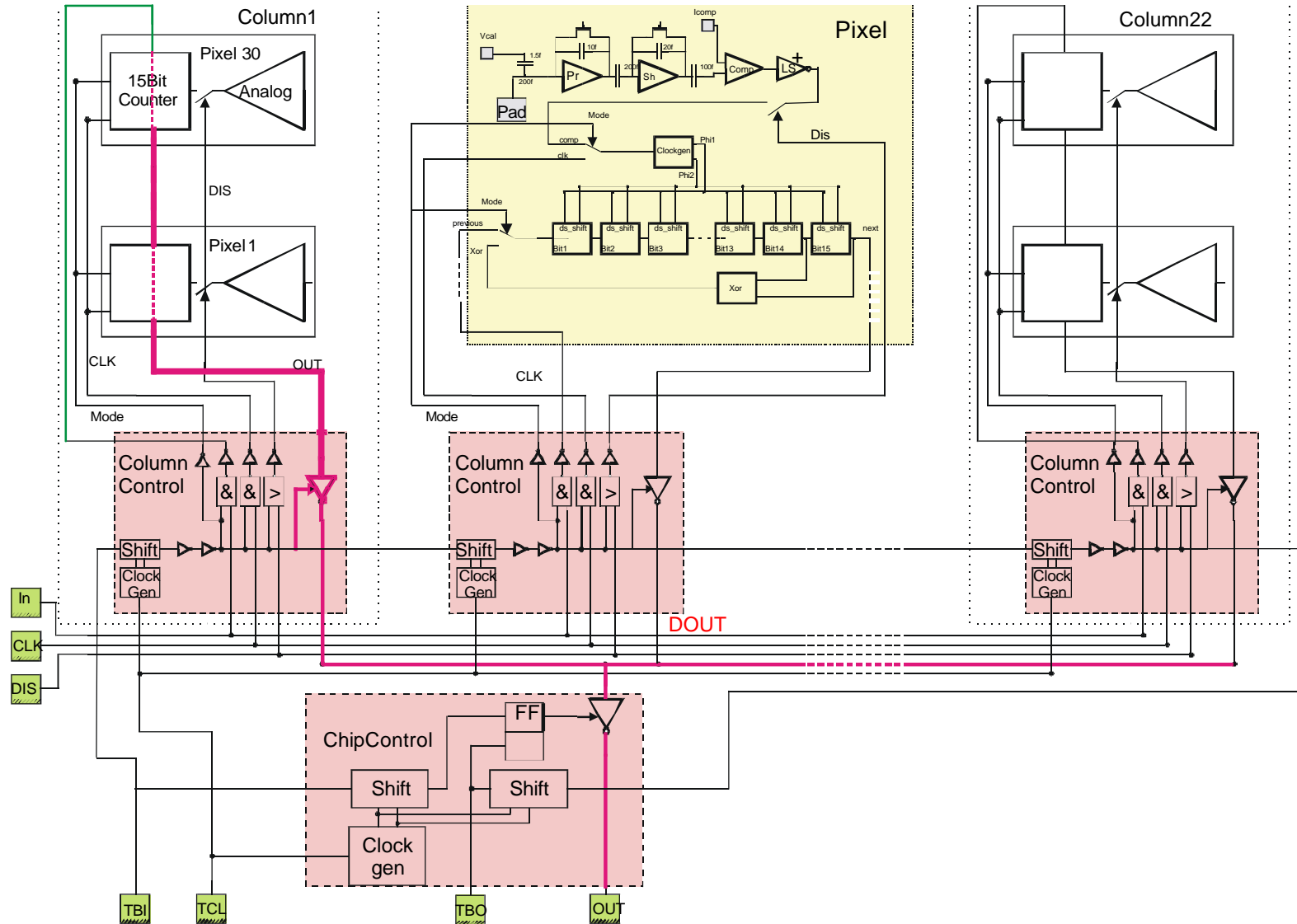
Size: 200 x 200  $\mu\text{m}^2$



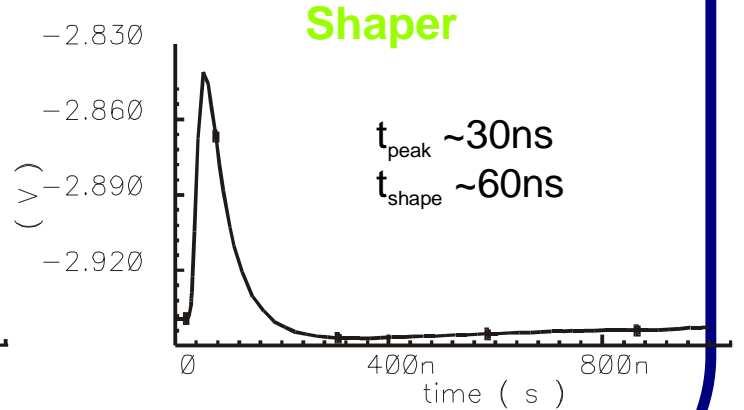
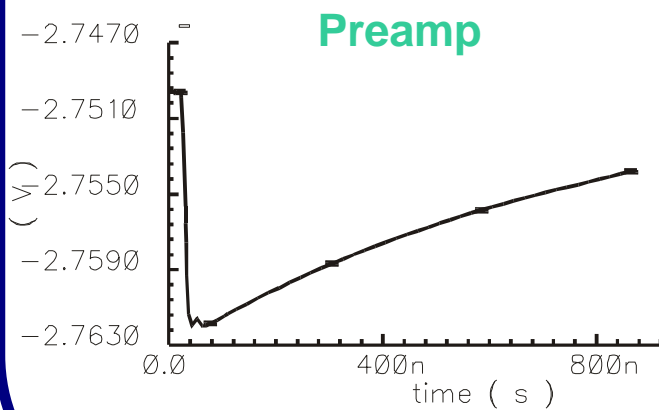
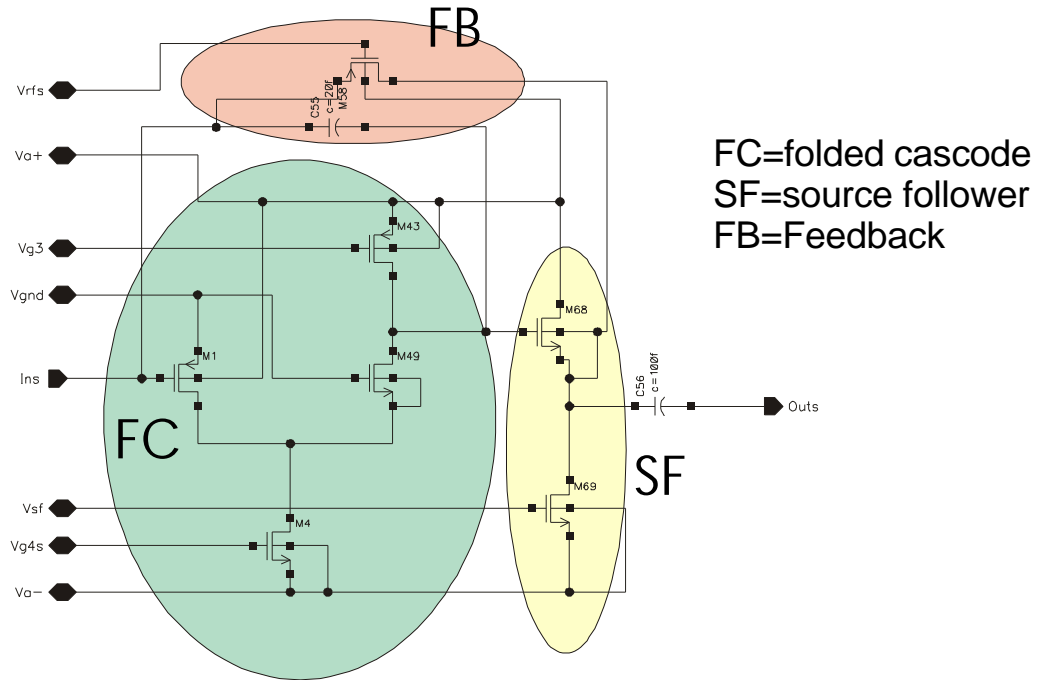
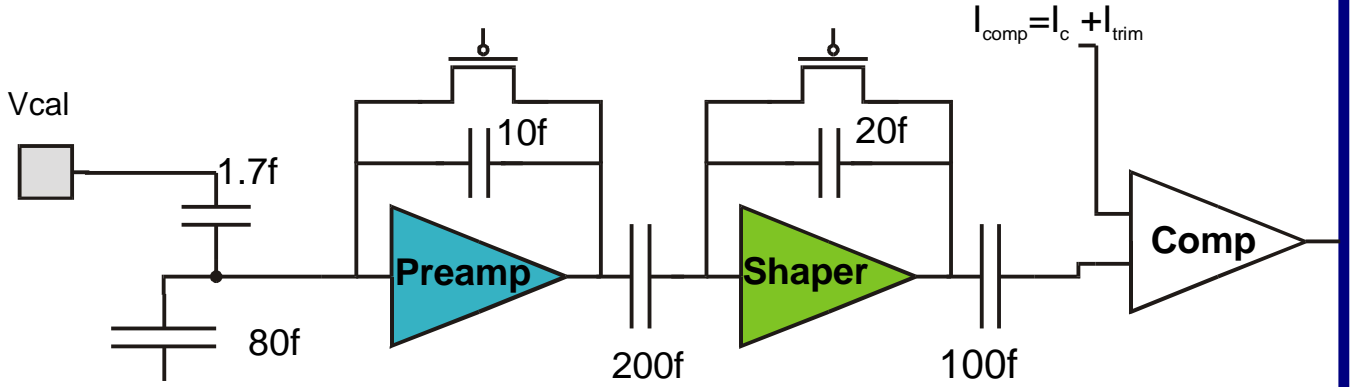
Size 200 x 200  $\mu\text{m}$



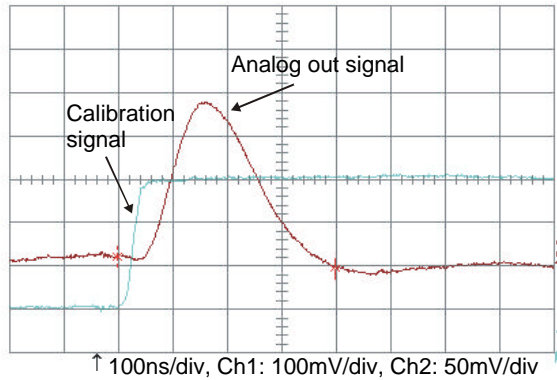
# SLS02 Architecture



## Pixel: Preamp-Shaper



## SLS02 Analog Part Results



- Noise measurements (without detector):

ENC ~50e- ( $P=75 \mu\text{W}/\text{pixel}$ ,  $t_{\text{sh}} = 100 \text{ ns}$ )

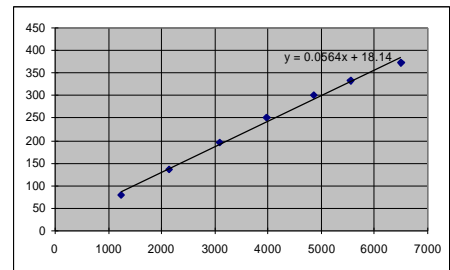
- Amplification:

~60mV/1000e-

- Linearity limit:

~6000e- (21keV)

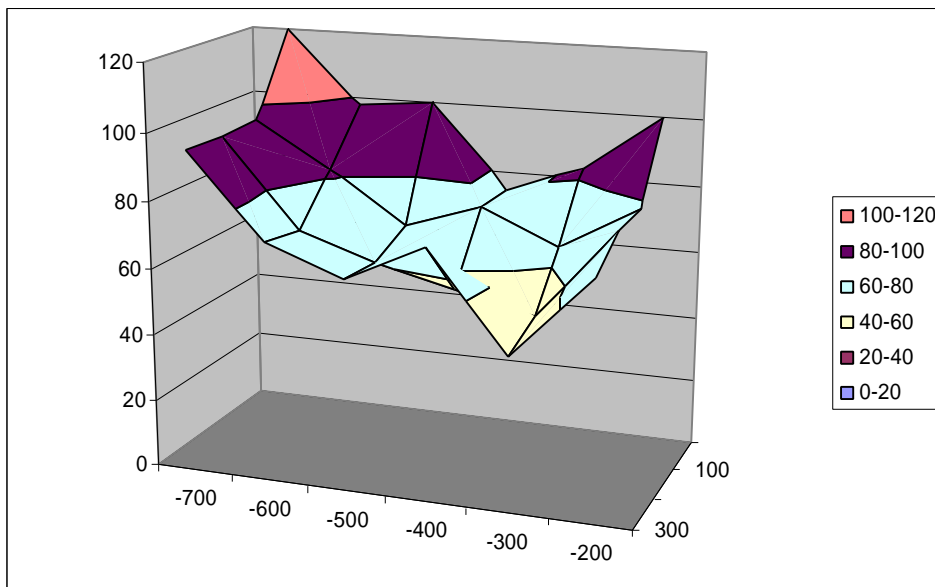
Analog Output [mV]



### Noise dependence on feedback resistors settings

VRFVRF5	-700	-600	-500	-400	-300	-200
300	96	71	63	74	45	70
200	95	69	61	56	50	77
100	96	82	67	75	64	78
0	120	98	100	75	83	100

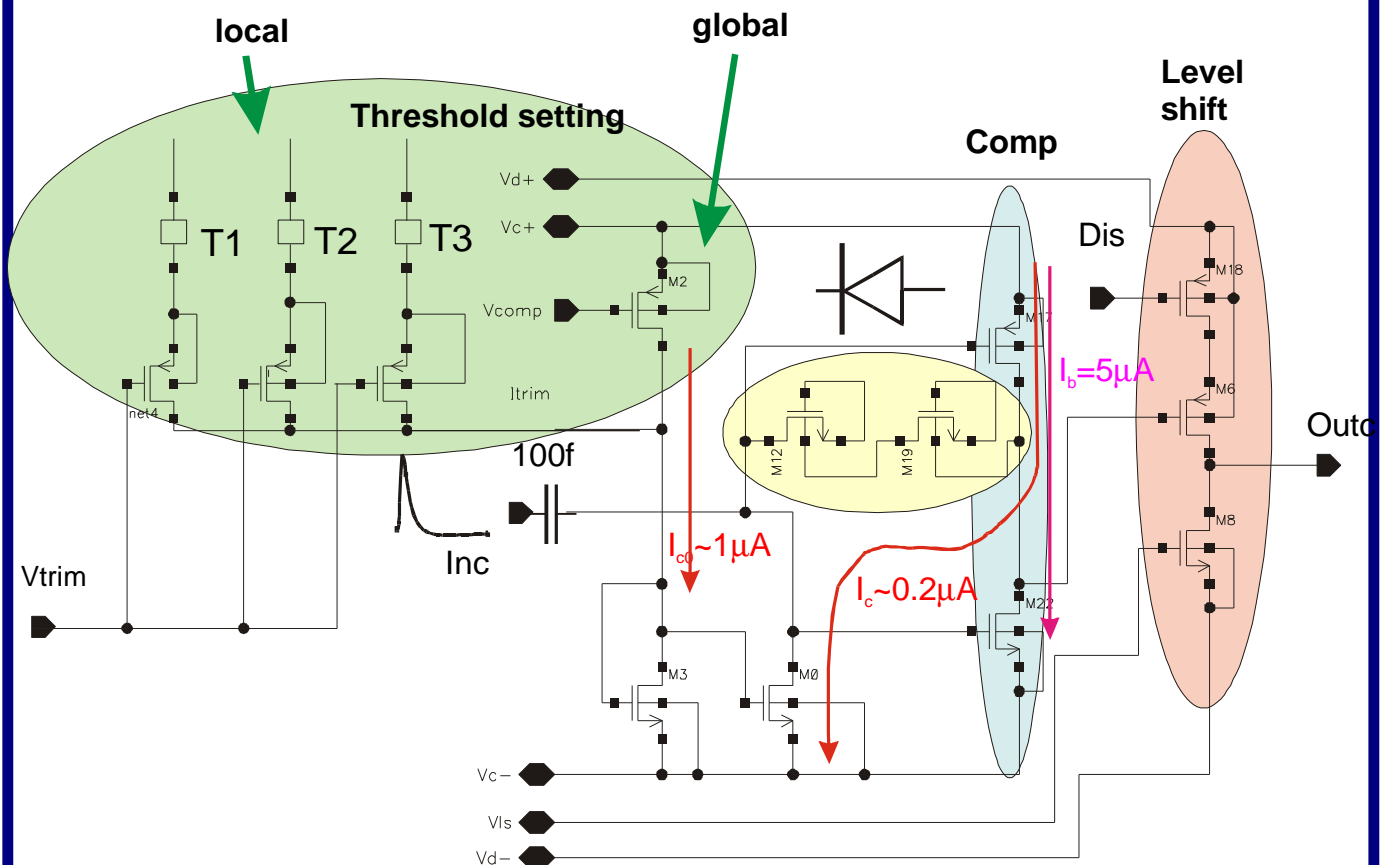
Signal charge



## Pixel: Comparator and trimming

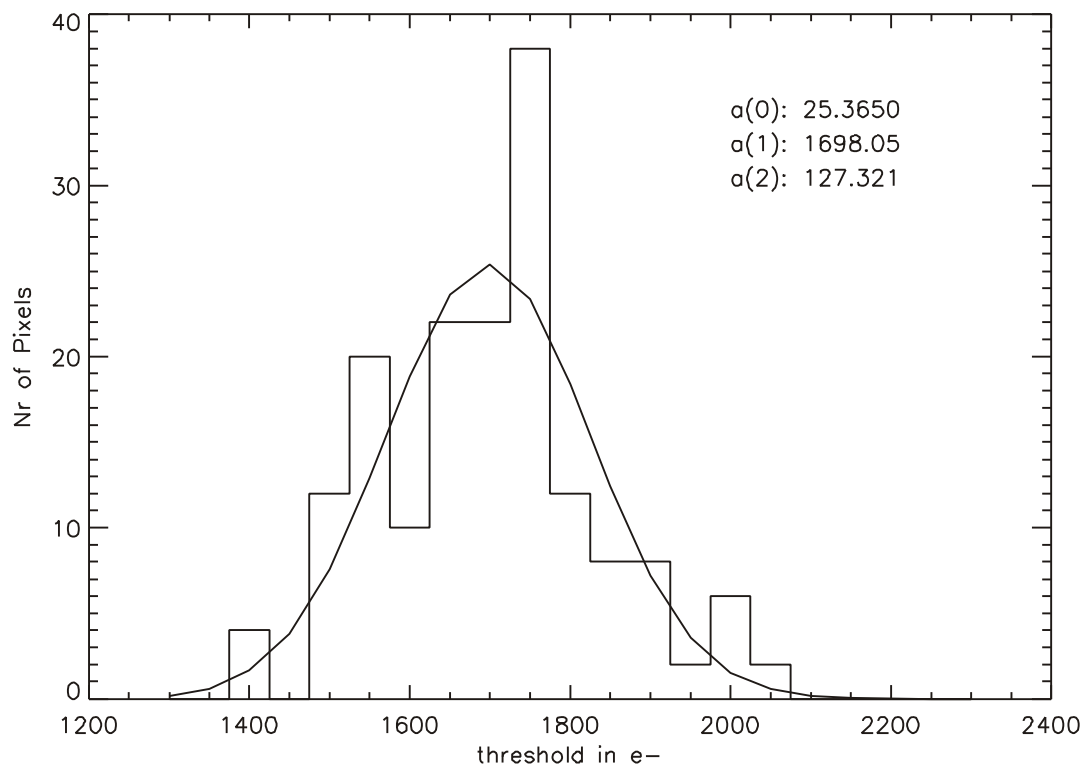
AC-coupled comparator with diode feedback

- simple inverter as comparator
- comparator biasing done via pn-junction of the diode -> expect lower threshold variations on the chip
- radiation insensitive
- low power consumption



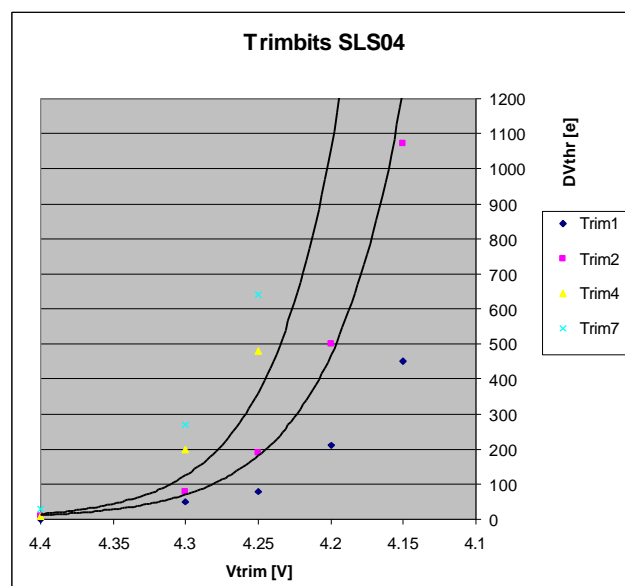
## Comparator Results

- Minimum Threshold  $< 700e^-$
- Threshold variation: 130  $e^-$  untrimmed

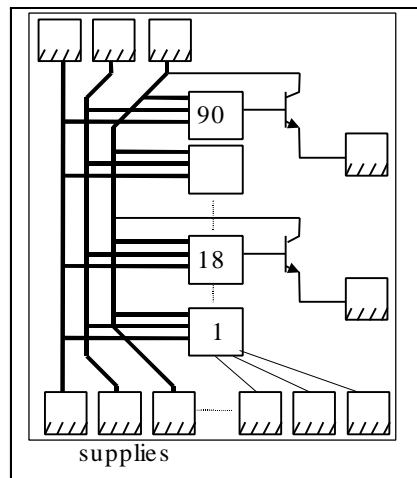


Threshold trimming:

Very low trim currents

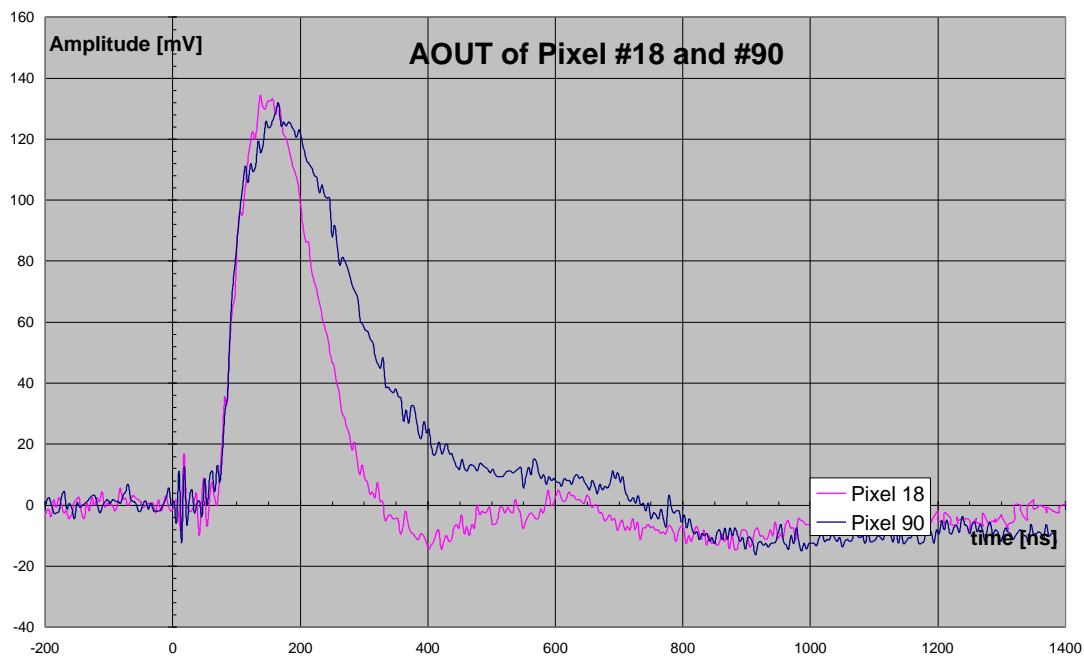


## SLS03: 2cm long column biased via periphery



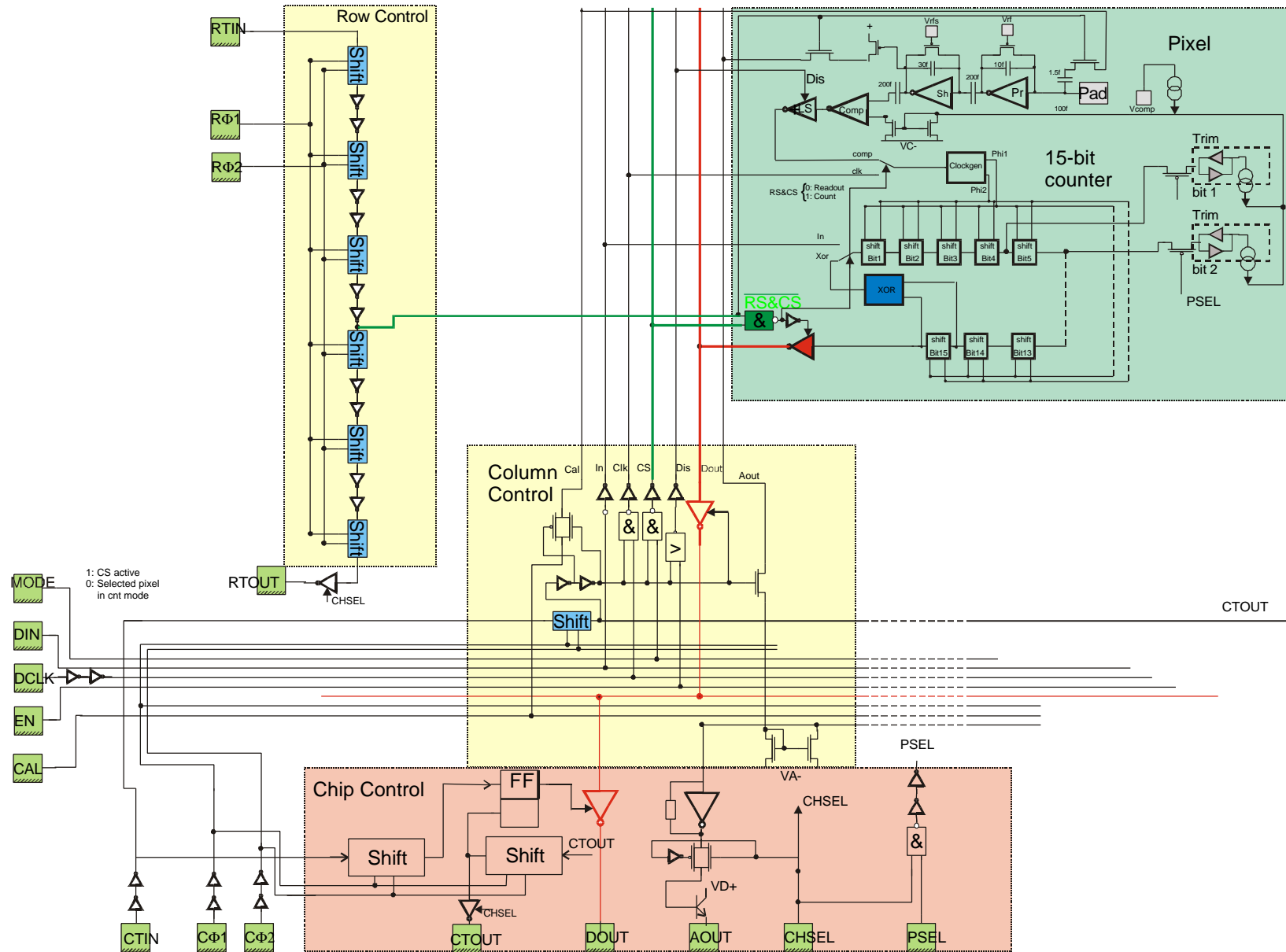
1.

supply	in [V]	out [V]	$\Delta$ [V]
VD+	5.025	4.81	-0.22
VD-	0.000	0.22	+0.22
VA+	5.024	4.93	-0.09
VA-	0.000	0.10	+0.10
VSF-	1.012	1.14	+0.13
VC-	2.983	3.06	+0.08
VGND	3.741	3.50	-0.24
Vsh	3.741	3.74	$\pm 0.00$
Vg+	5.024	4.92	-0.10
VC+	5.024	4.95	-0.07





# SLS05 Architecture



## Final Chip: Yield estimation

Yield measurements of SLS02 chip (22x30 pixels):

Defects due to dynamic logic (Semi-static SR in Pixels):

$3.8 \times 10^{-4}$  /bit ->  $5.8 \times 10^{-3}$ /pixel

(Yield for 85 pixel column: 60%)

Defects in analog part:

3/19=0.842/chip

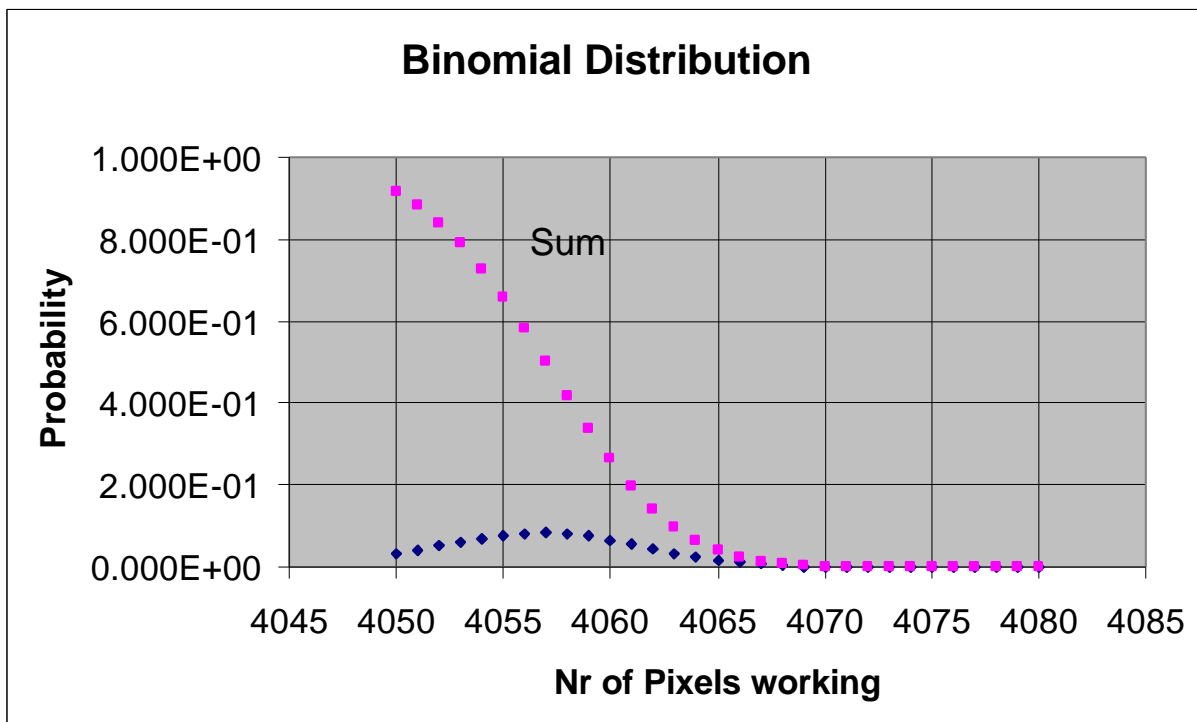
Yield estimation for 48 x 85 pixel chip

XY-Adressing, 133 SR-cells: 0.898

Analog part 0.346

30 bad pixels 0.916

**Expected overall yield 0.28**



## **Design of a large read-out chip for protein crystallography: Conclusions**

Prototype chips with 22x30 pixels are working

Simulated final chip with one 20mm long column-> working

Dynamic logic in DMILL is a yield killer

Design with yield tolerant architecture is a must