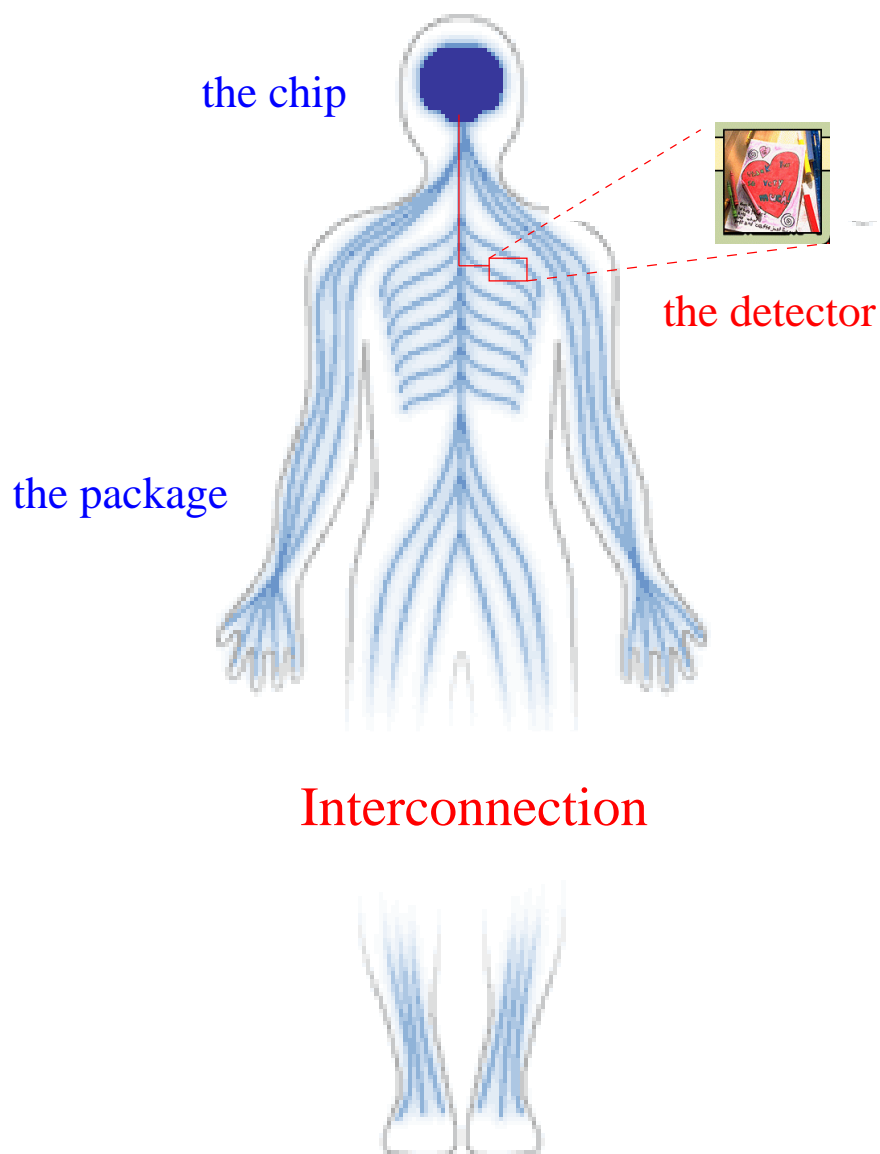


The challenge of hybridization

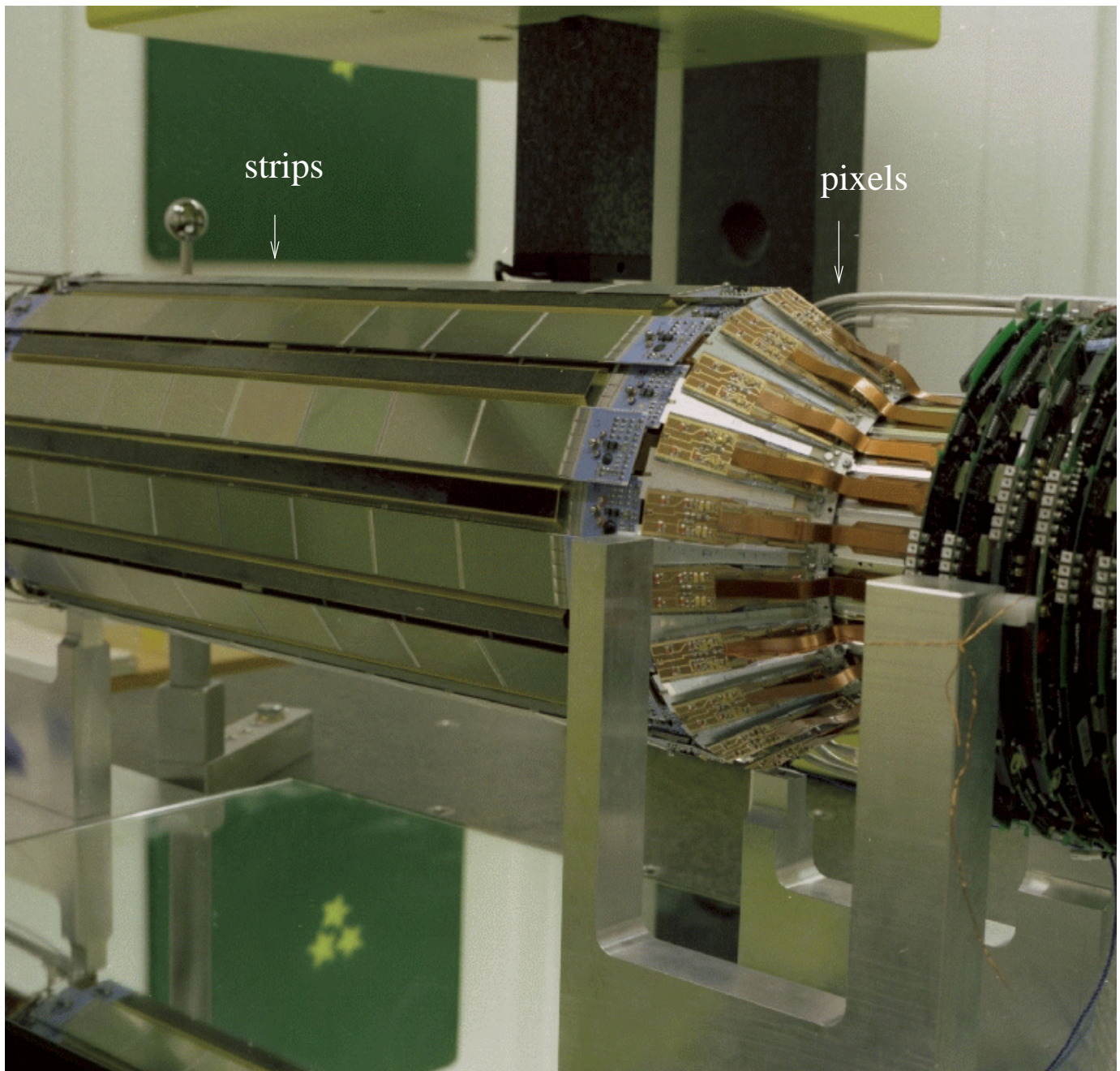
Massimo Caccia

Universita' dell'Insubria @ Como, Italy



Interconnection

a case study: the DELPHI pixel detector



- completed and installed in 1996
- running for 8 months/year without hw interventions since 1997

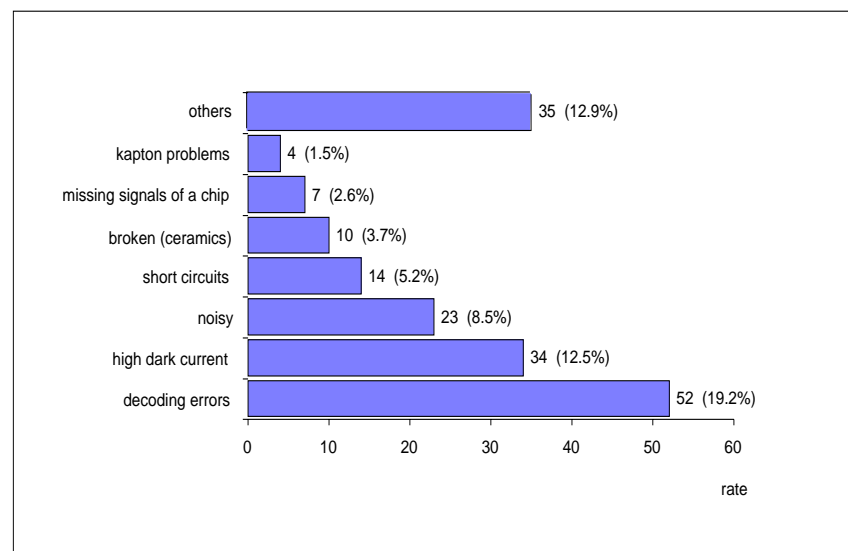
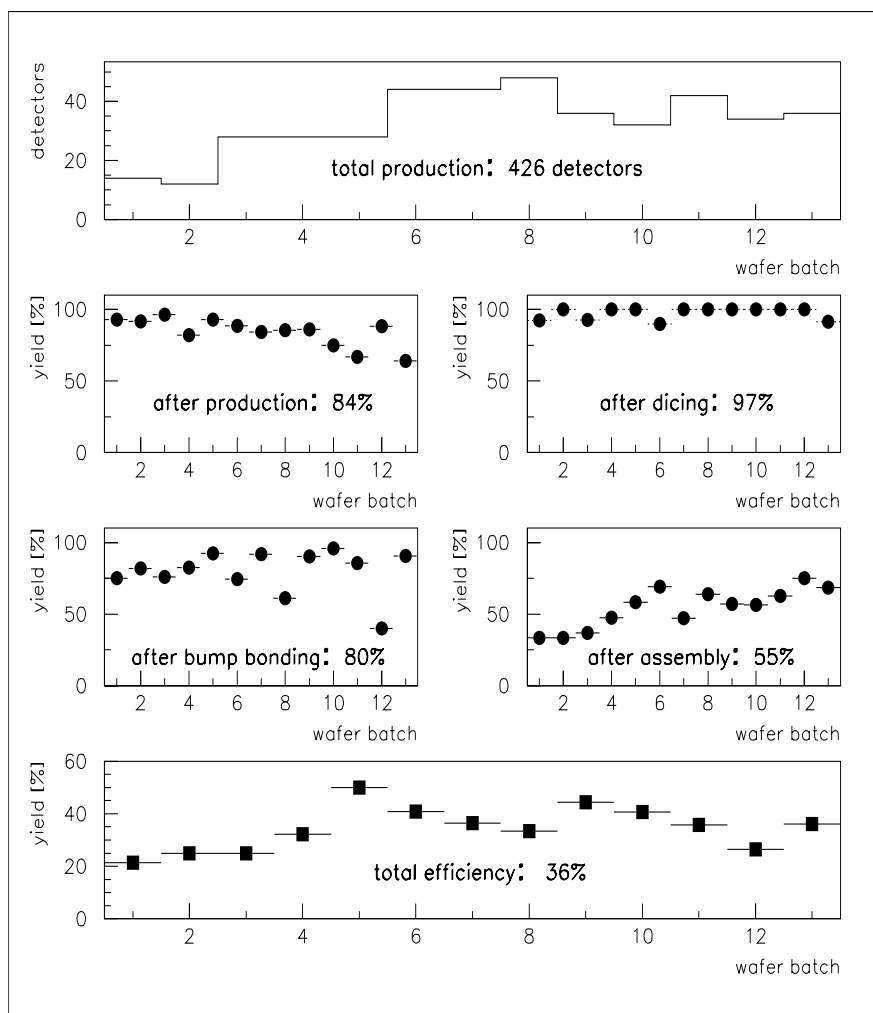


a "relaxed"
detector:

- "mass" production: 152 modules, for a total of 1.2 M pixels
- pixel cell size: 330 micron x 330 micron
- material budget: 300 + 300 micron (Si) + 300 micron (Kapton)
- temperature: - operating at room T
- 10 C gradient along the 7 cm long module acceptable
- radiation hardness: \ll Krad/year
- mechanical tolerances
- precision mounting/alignment
- readout speed: 5 MHz

nevertheless.....

Pixel detector production yield

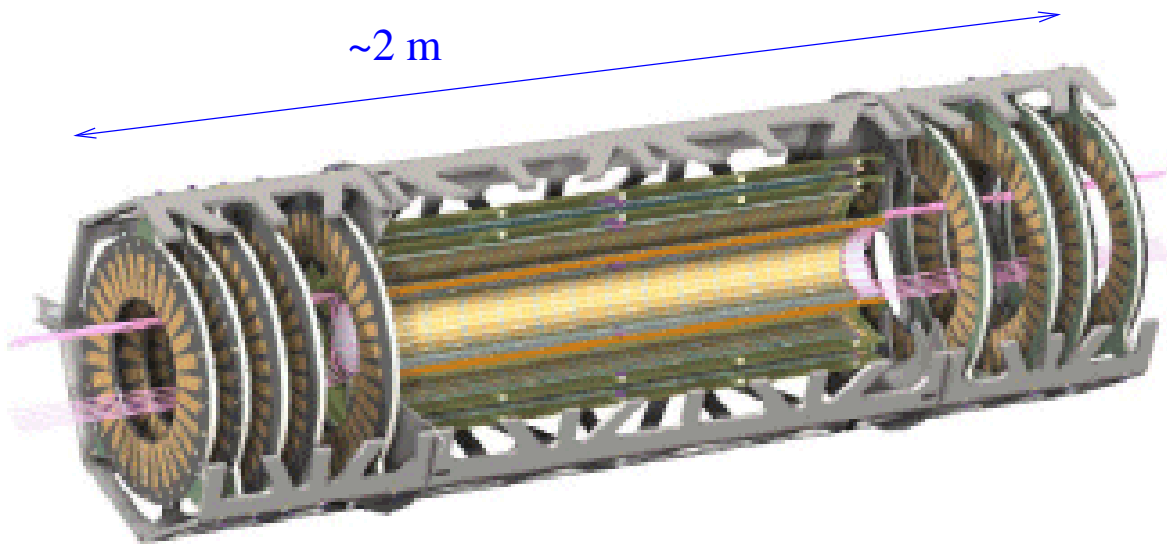


final test: breakdown of errors

module assembly most critical
"learning curve": ~30% --> ~60%

total production efficiency: 36%

the next generation: pixel detectors for the future hadron colliders



a sketch of the ATLAS pixel detector

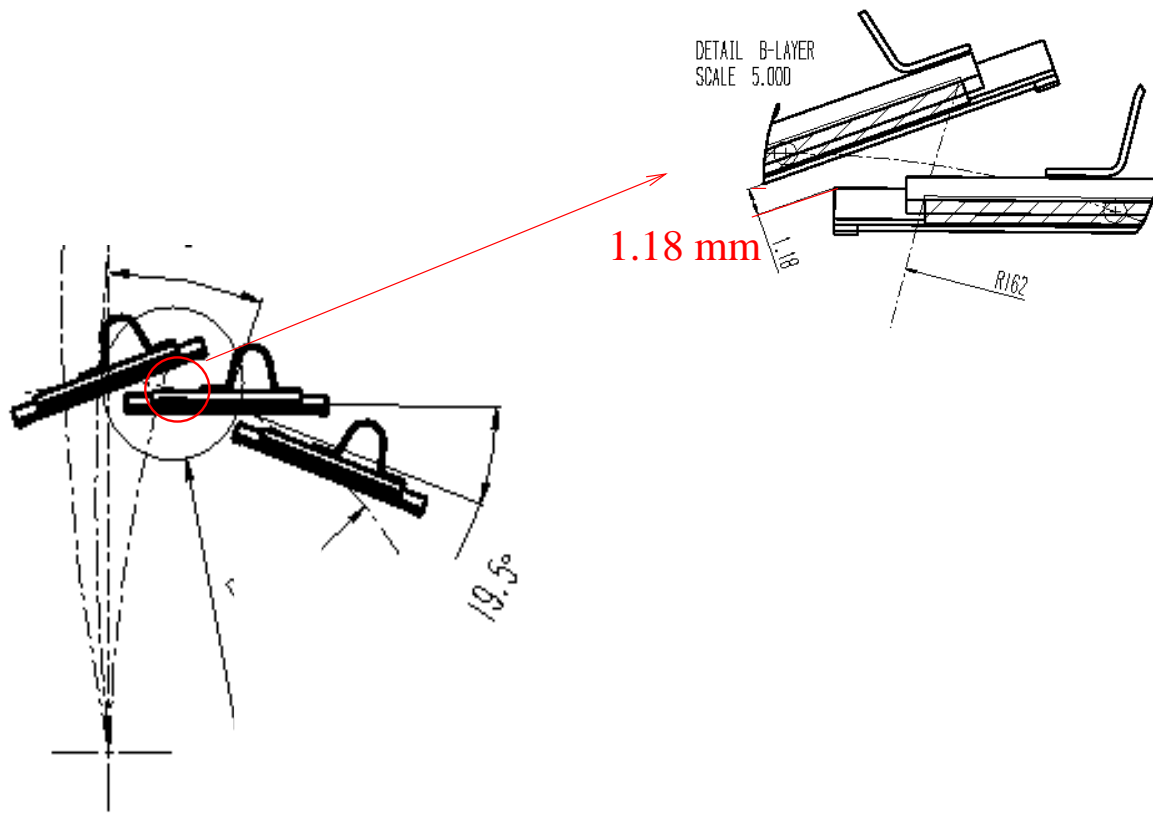
- real "mass" production: ~ 2200 modules (16 chips each),
~140 M pixels in total
- minimal pixel pitch: 50 micron
- material budget is an issue! ratio of the different contributions (in X_0)

sensor + VLSI : substrate for power bus, : mechanical support
data & control lines

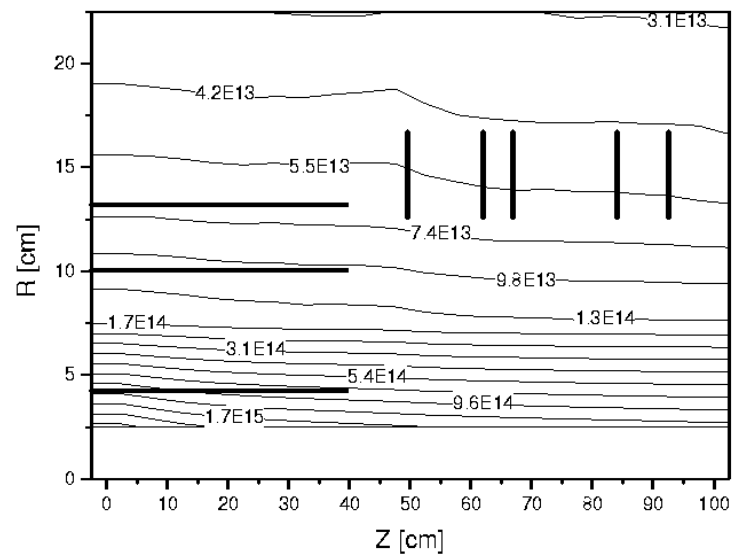
1 : 0.4 : 1.5

with possible gradients at the 2-3 C level

- very limited clearance : $O(1\text{ mm})$



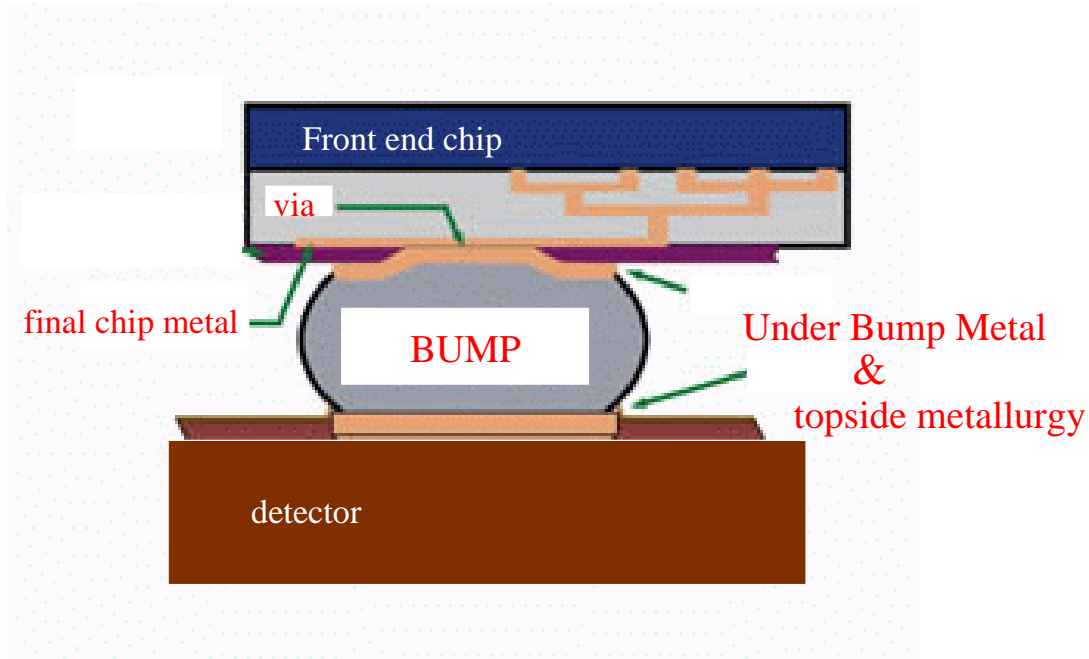
- radiation hard:



- clocked at 40 MHz

nevertheless, a global yield at the 70% level is the goal to be achieved to have the detector completed

Due to the bond density ($\sim 5000-10000 / \text{cm}^2$) and the pitch ($\sim 50 \mu\text{m}$) the only meaningful interconnection technique is BUMP BONDING of FLIPPED CHIPS:

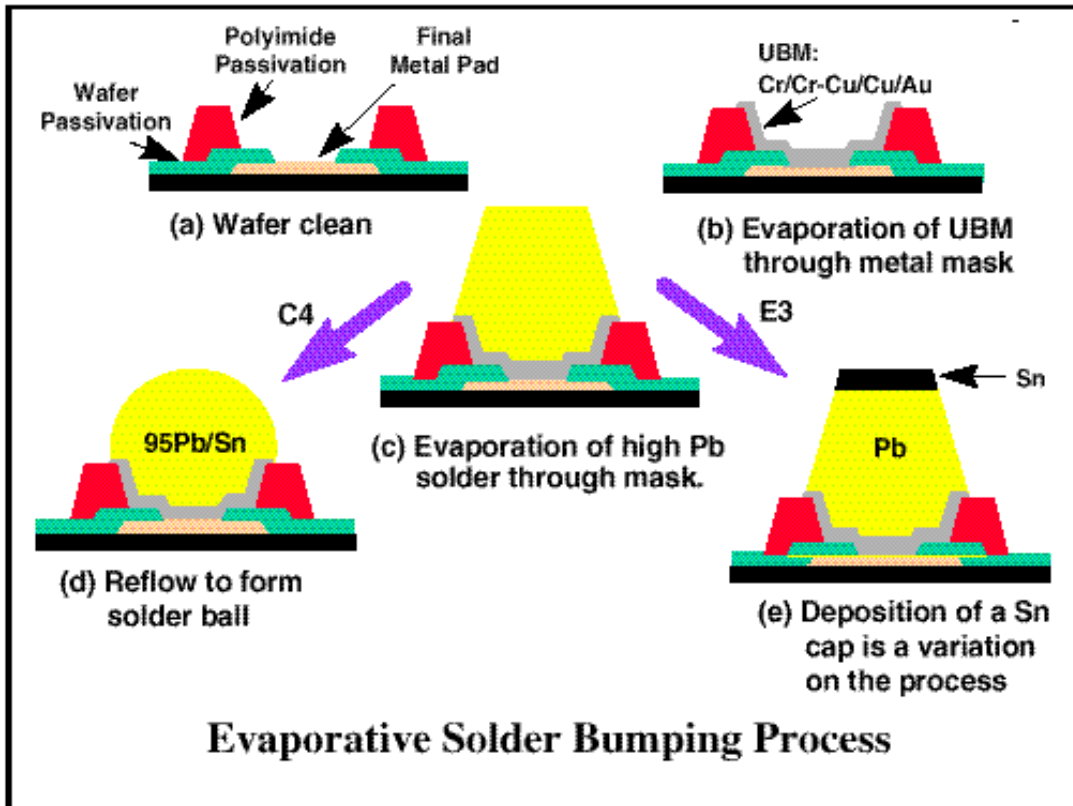


The choice of the bump metal determines the processing characteristics:

- under bump metallization
- bonding mechanism => - temperature
 - pressure
 - alignment precision
 - reflow
- aspect ratio => - pitch
 - single/double sided process
- mechanical properties => - tensile/shear strength
 - "reworkability"

Solder bumps

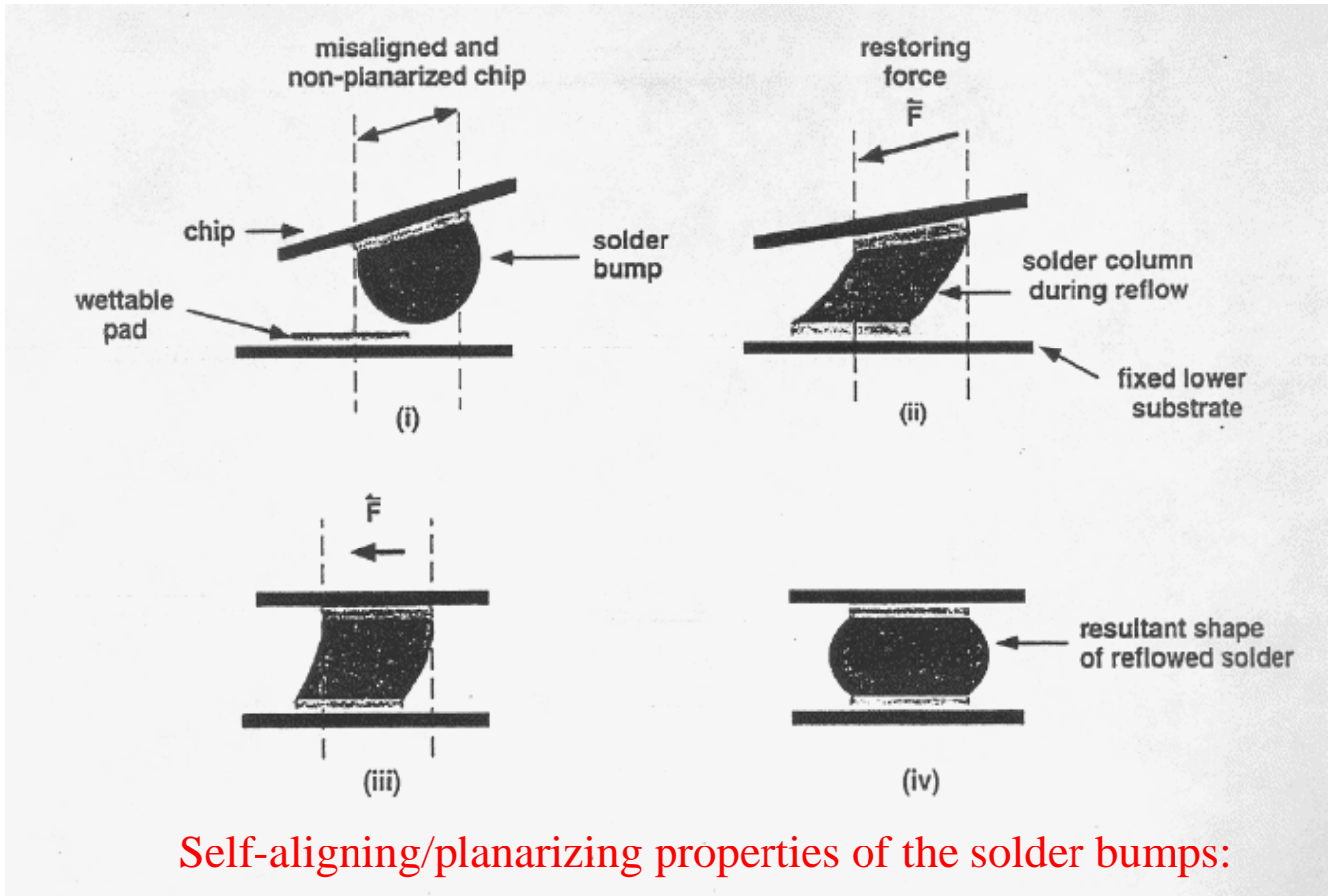
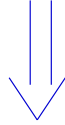
Solder bump bonding has been introduced ~ 30 year ago by IBM (C4 processing = Controlled Collapse Chip Connection) to overcome the limits of wire bonding



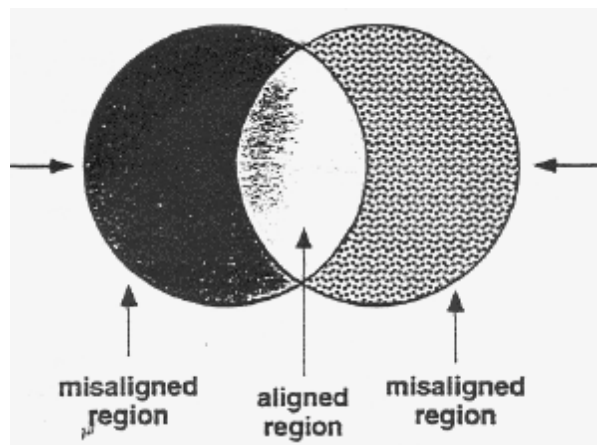
- UBM = Under Metal Bump:
 - adhesion layer (active metal) on top of the final metal pad (Cr or TiW)
 - barrier metal to prevent the solder dissolving the active metal (Cr-Cu or Cu)
 - Solder wettable metal (Cu)
 - Oxide prevention (Au)
- reflow occurs at different temperatures, depending on the solder mix and ranging between 230C (63SnPb) to 360 C (5SnPb).

Reflow may occur in presence of a suitable flux or in a fluxless process, possibly in a batch of organic compound

- apply a resin-based flux, for fixing the chip
- align the chip to the substrate and place it (~0 pressure)
- move the assembly to a furnace for reflowing (neutral atmosphere)



wettable
substrate pad



solder bump

remarks

strong points:

- uniformity & self-alignment => low % of missed contacts
- optimal height/pitch ratio (~20 micron/50 micron)
=> bump grown on one side only
- excellent electrical properties (contact resistance ~ mOhm)

critical points:

- complex UBM: a not perfect control of the metallurgy may result in poor adhesion
- "high" Temperature: it may harm rad-hard chips
- "reflow" chemistry: "leftover" might affect wire bondability;
Hydrogen entrapment may result in voiding
- pitch for detector applications at the edge of the industrial standards
(~150 micron, 70 micron footprint)
- thermal fatigue of bumps should not be neglected —————>

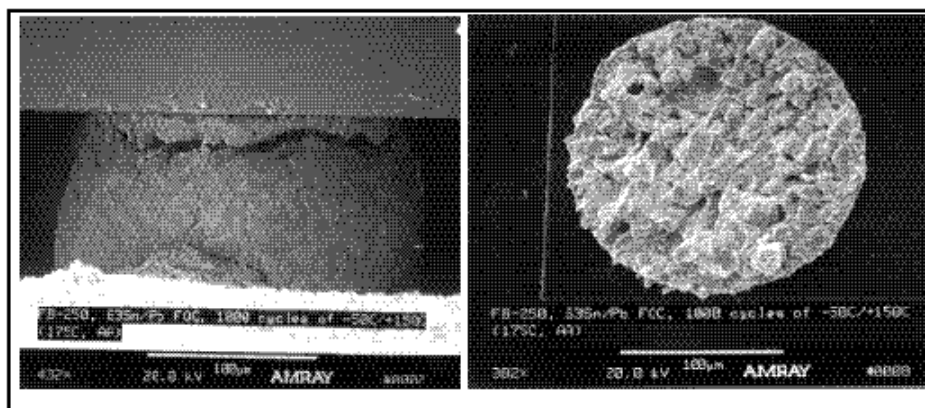
**Table III: Thermal Fatigue Life
Comparison of Bump Alloys
(normalized to 63Pb/Sn with no underfill)**

(number of cycles)

Solder Alloy Composition	Reflow Temperature (°C)	Fatigue Life without Underfill	Fatigue Life with Underfill
63Sn/Pb	230	1.0	15
5Sn/Pb	360	1.2	Not Tested
50In/Pb	260	2-3	>30
37In/Pb	290	2-3	>30
3.5Ag/Sn	260	0.5	11
5Sb/Sn	280	0.3	11
Sn/Pb/Cd/In	230	1.0	13
Sn/Ag/Cu/Sb	260	1.0	13

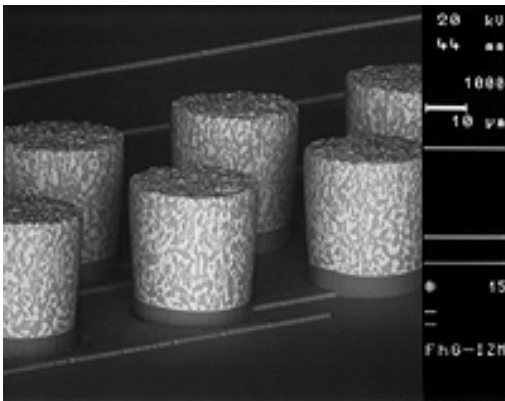
experimental conditions:

- bump diameter: 100 micron
- thermal cycle range: -50 C to 150 C
- substrate: Alumina, 0.5" x 0.5"

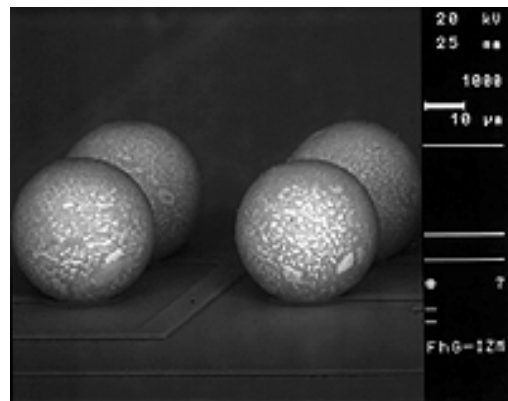


achievements

- WA97/RD19: 0.5 M pixels, 50 x 500 micron size, bump bonded by GEC-Marconi
- DELPHI: 1.2 M pixels, 330 x 330 micron size, bump bonded by IBM
- ATLAS: test structures & prototypes bonded by IZM, Berlin; 50 x 400 micron size



before

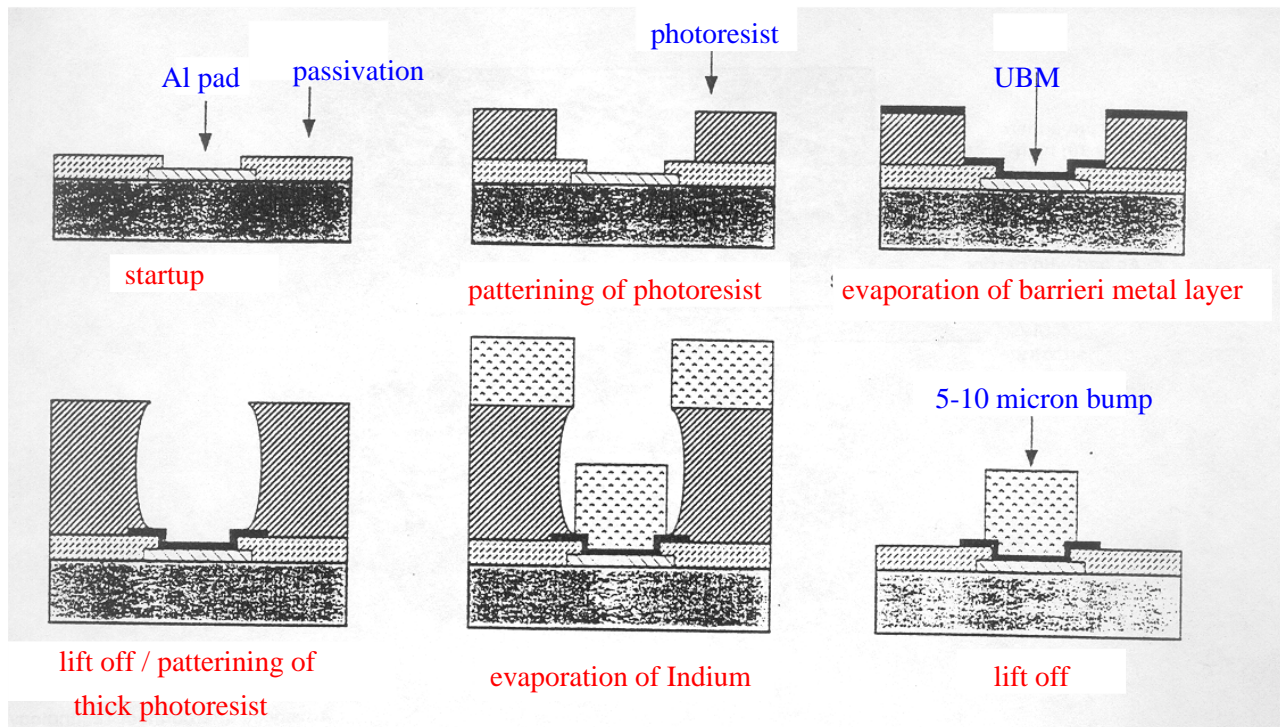


after reflow

fault rate ~ 10 ppm

Indium bumps

Indium bumping technology refined for IR sensors (Focal Plane Arrays), operating at liquid N temperature.



- because of In oxidation, "reflowing" In bumps is far from being "trivial"
- in order to avoid In to be smashed against the photoresist walls, chemical etching of the holes and evaporation have to be under good control and bumps have a small height/pitch ratio (5 micron/50 micron)
=> bump grown on both sides
- after electrical breakdown, the contact resistance is O(1 Ohm)

remarks

critical points:

- high yield attachment requires excellent planarity and bump uniformity
- "small" bumps require a "double sided process"

strong points:

- simple UBM: a Cr adhesion layer will do it
- bonding by solid state diffusion => it requires little pressure ($\sim 10^{-2}$ N/bump) at temperatures ranging between 20-100C
- pitch for detector applications well within industrial standards (~30 micron pitch)
- Indium plastic properties should help against thermal fatigue but intensive tests should be considered

achievements

- ALENIA (Italy), SOFRADIR (FRANCE) on ATLAS pixel modules
- PSI (Switzerland) on CMS modules

have gone far beyond a feasibility study; fault rates at the 10 ppm level have been achieved with a fair/good control of systematics:

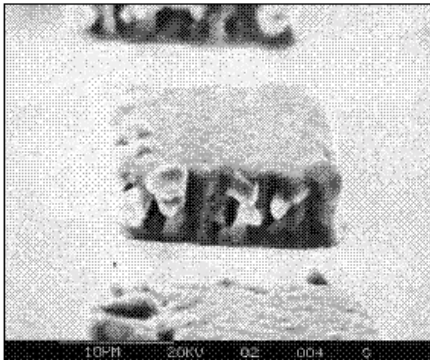
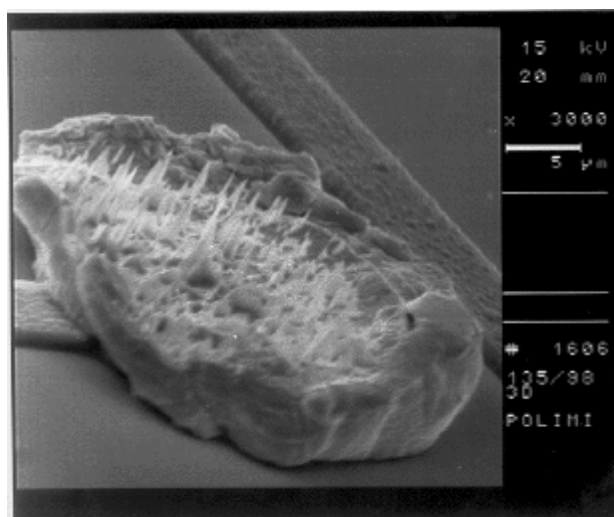


Figure 6-14 SEM image of the Indium bumps after the lift-off process (courtesy of ALENIA)

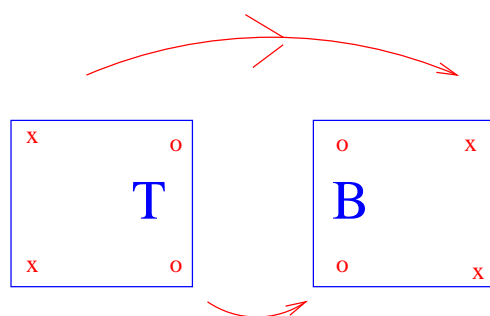
conclusions on the front-end to sensor interconnection

- both In and Solder bumps have proven to have an acceptable single bump failure
- the choice is defined by "side effects", process control and repeatability
- reworking is also an issue
- other interconnection techniques (ACF, stencil printing, stud bonding) are not an alternative by now

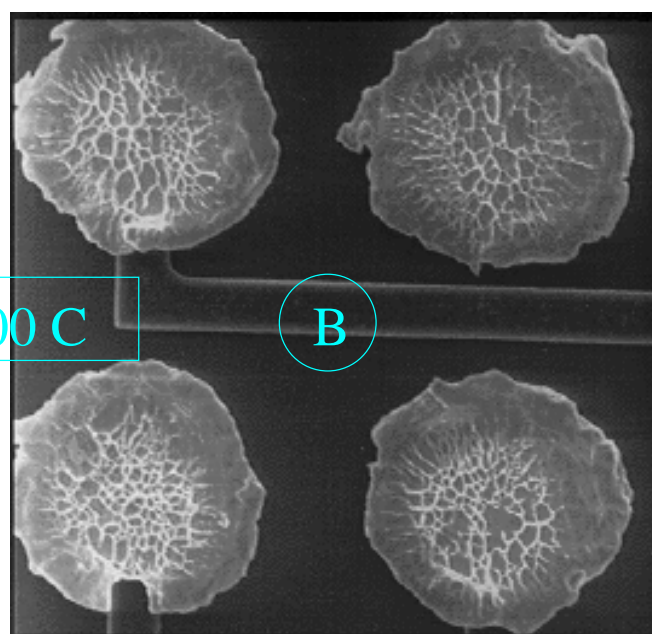
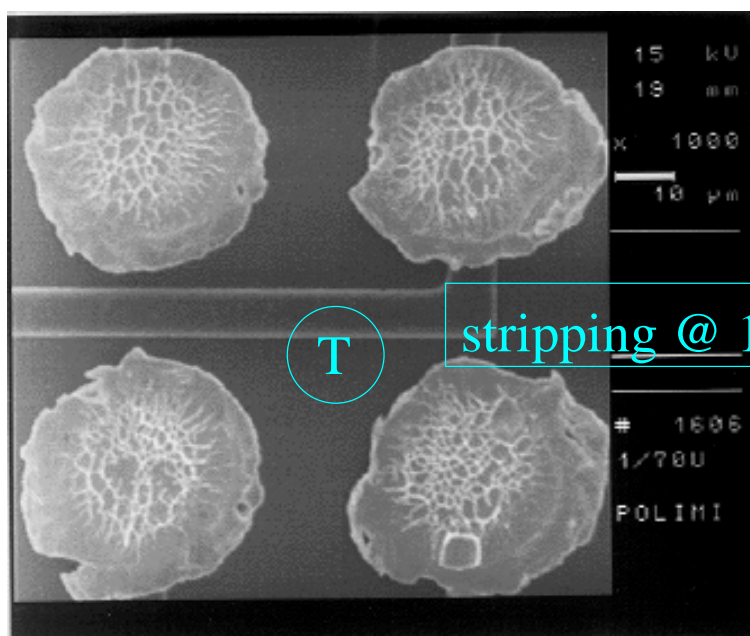
These is how the bumps appear after being stripped at 100 C:



a quite isotropical
detachment was
obtained



T is flipped
over B



IN BOTH CASES I_n IS LEFT ON BOTH SIDES

reworking

The possibility of re-working has been assessed by the analysis of test structures in terms of:

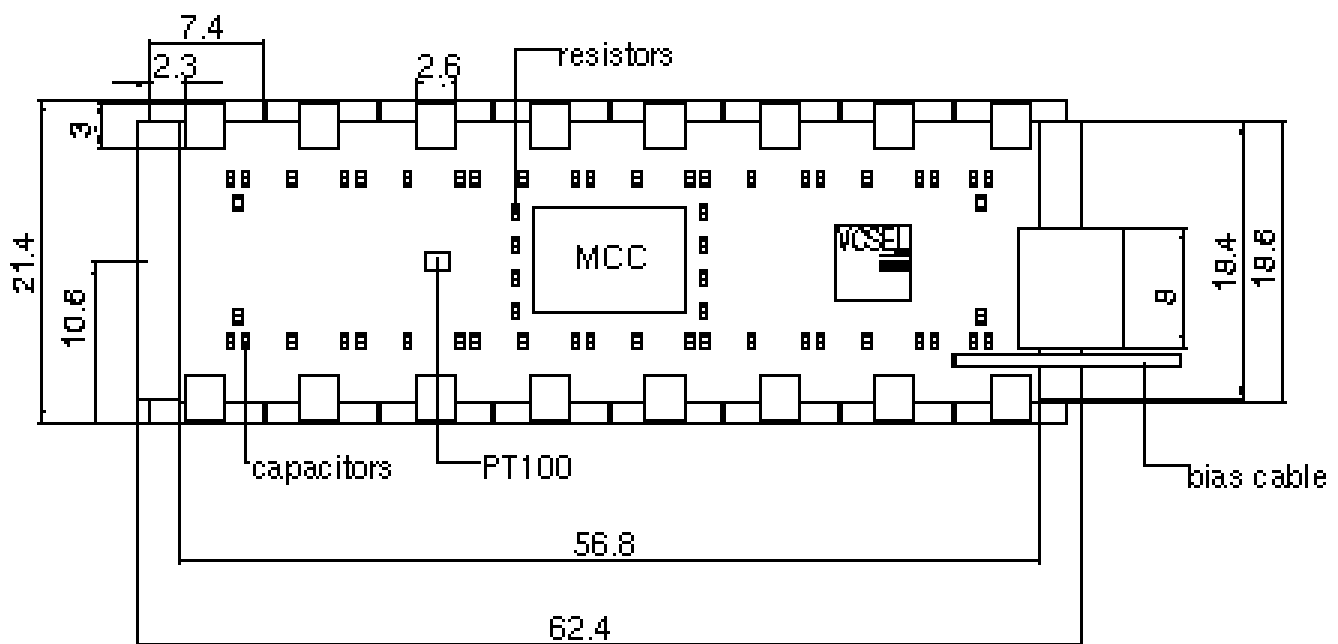
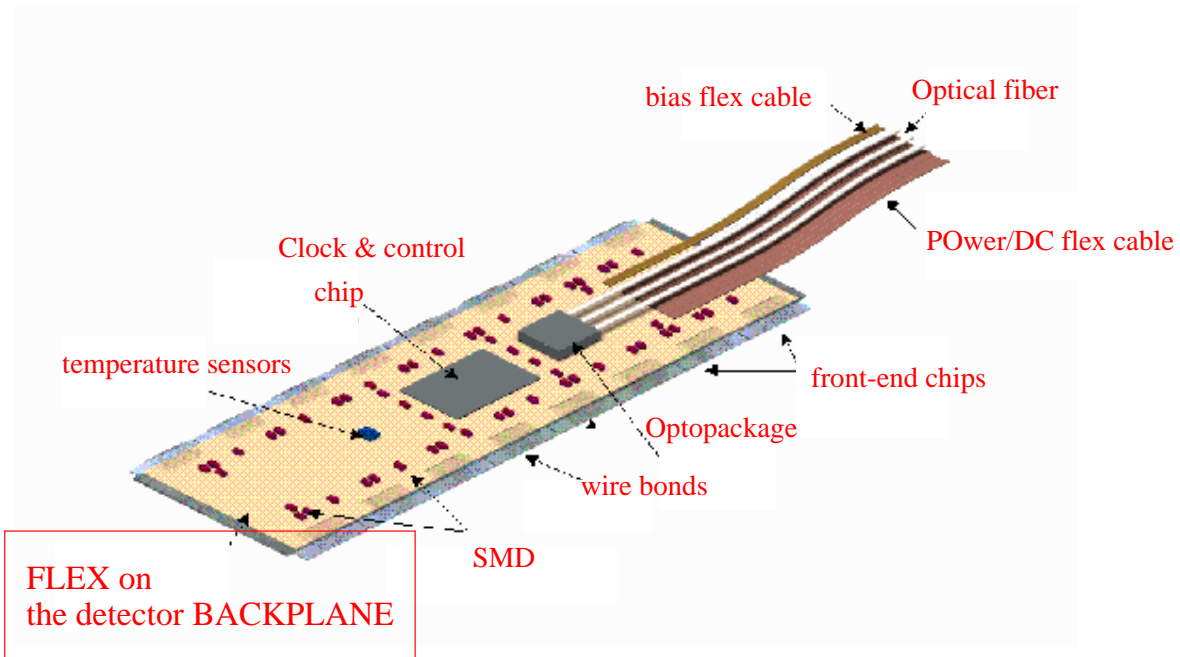
- tensile strength of the structure: decreased by 20%
- single bump electrical fault rate: 0/50 contacts missing on 3 structures
- characterization of a re-worked real detector: ~ 10% missing pixels on a "single chip" assembly

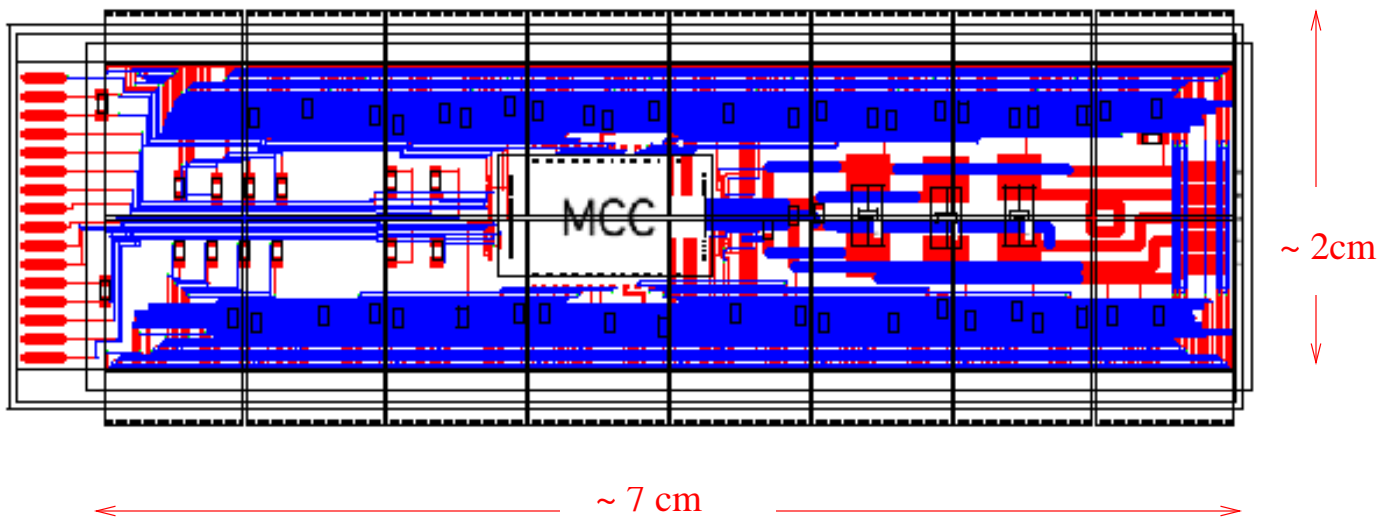
A dedicated "chip-stripping" machine has been designed and it's being built

Power lines and signal bus

Three approaches:

● "flex" hybrid:





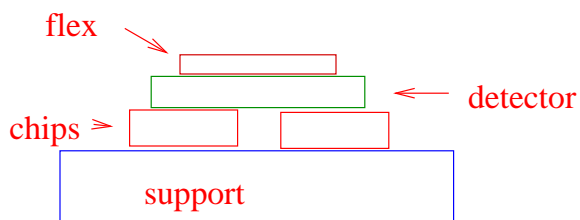
ATLAS specifications: - 2 metal layers

- stratigraphy:

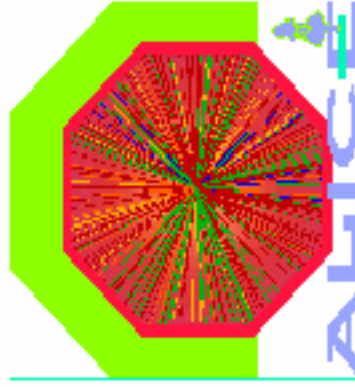
- * kapton substrate, metal traces on both faces (25 micron thick)
- * Copper traces: 7 μ m thick, 75 μ m minimal distance, 75 μ m minimal space
- * top/bottom cover layer: 12.5 μ m thick

critical issues:

- wire bonds
- stress induced on the bumps:

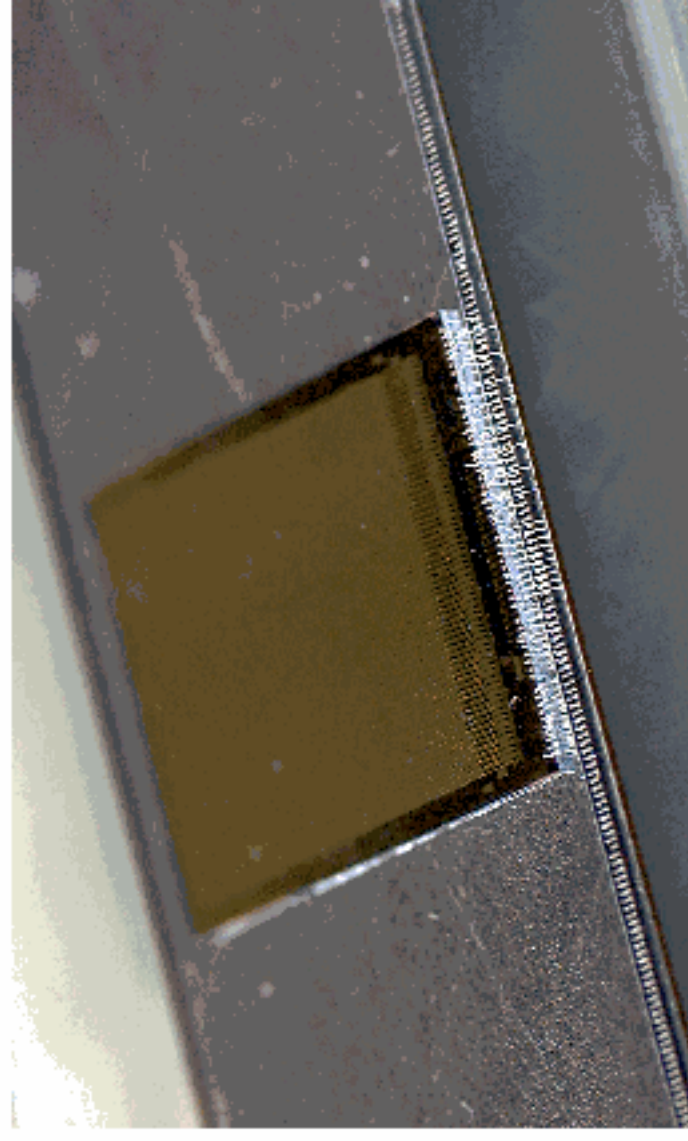
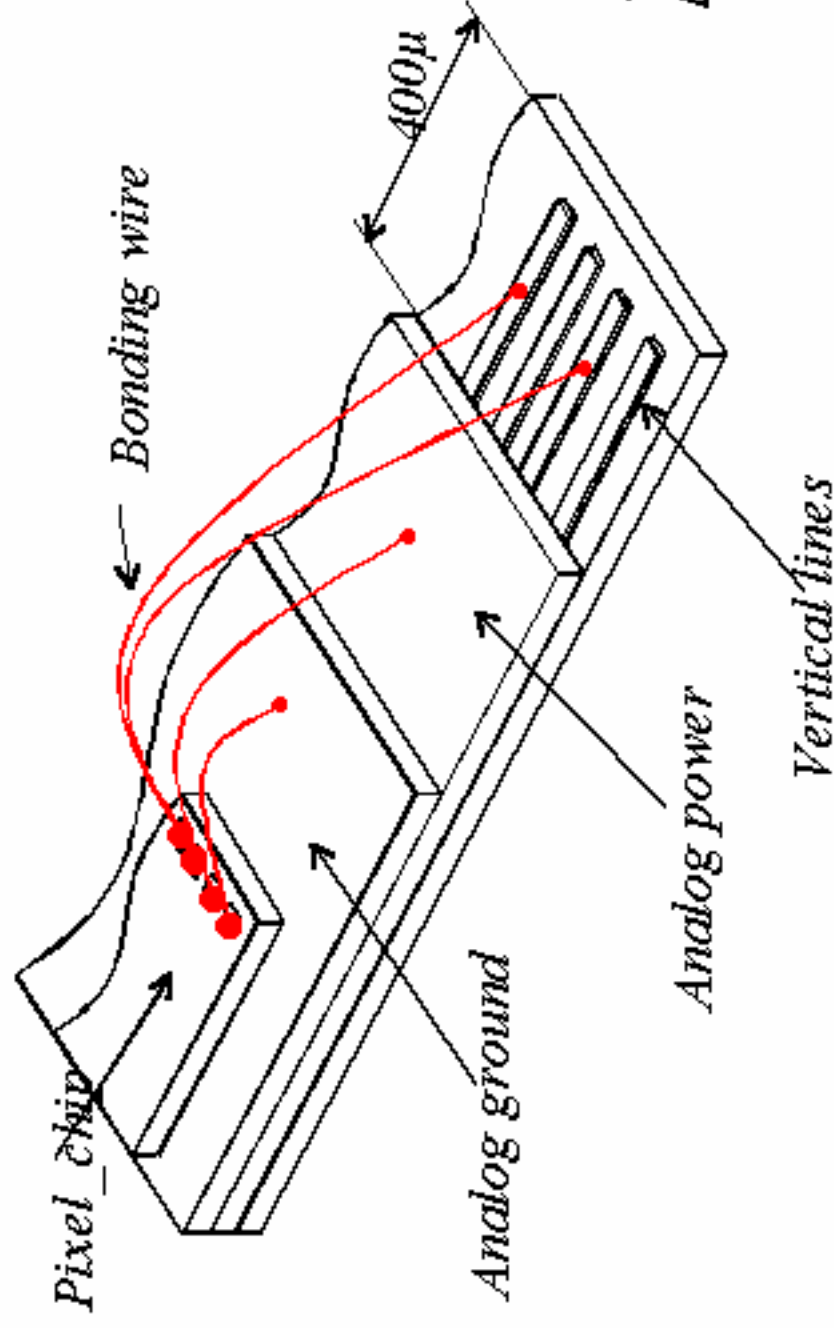


material	CTE ($\ast 10^{-6} \text{ C}^{-1}$)
CC (support)	-1 (in plane) 6 (transverse)
Silicon	2.5
flex	~ 45



ALICE SPD: MULTI LAYERS BONDING CONNECTIONS ISSUE

1-st essay



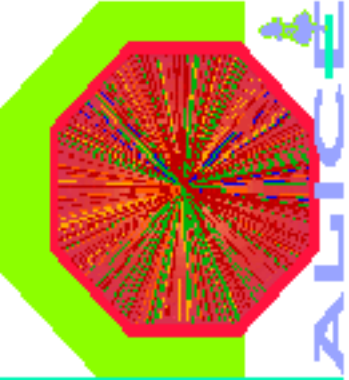
200mm x 17mm
4 aluminium layers
bus = 81 lines 100µ

Aluminium: 15µ
Kapton: 50µ
Glue: 10µ
Total thickness: 300µ

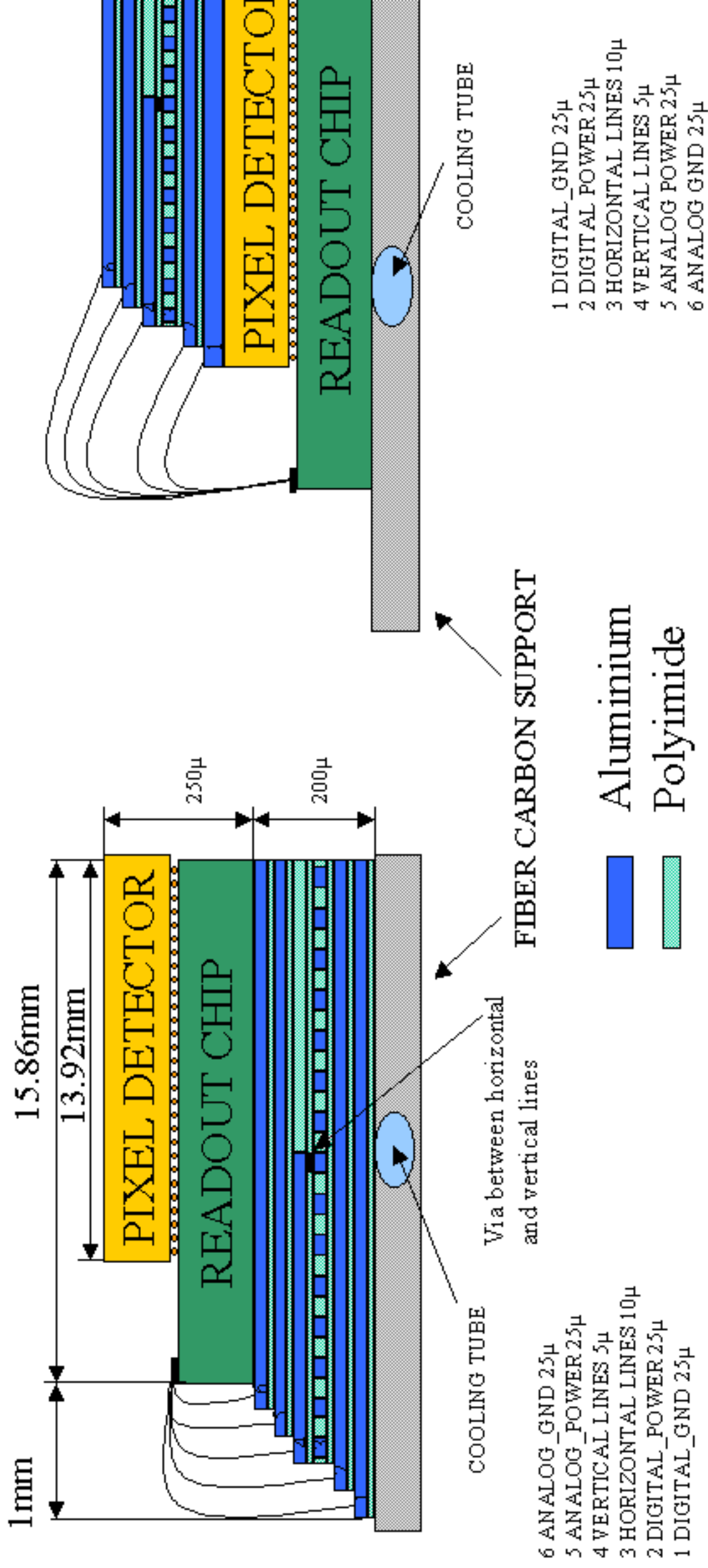
. . . mechanically it's feasible! →



Next step: 200µm & 6 Al layers



ALICE SPD: TWO PIXEL BUS HYPOTHESIS

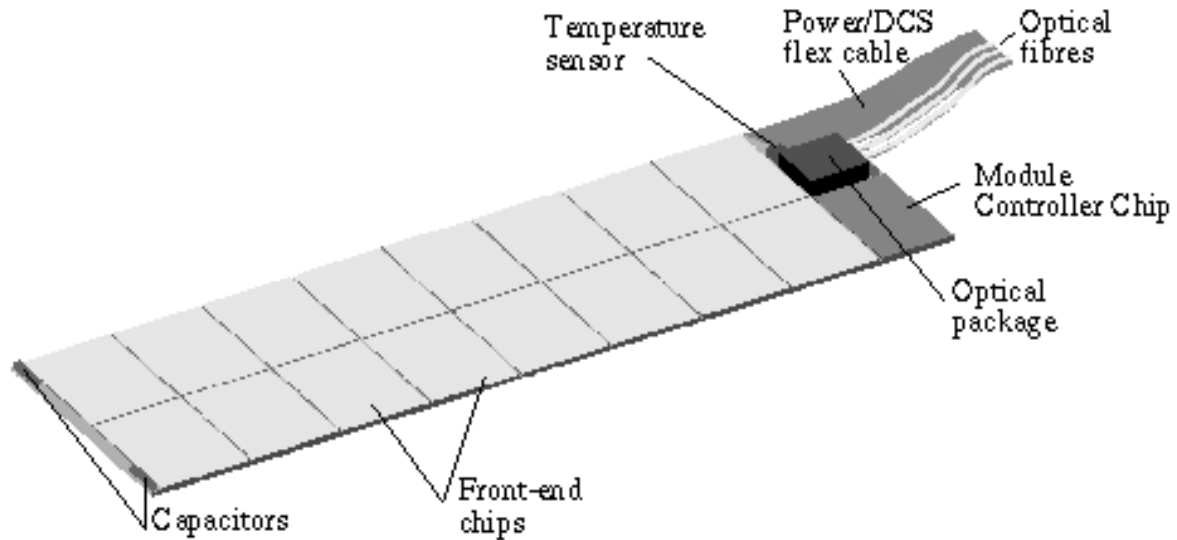


Solution A

Solution B

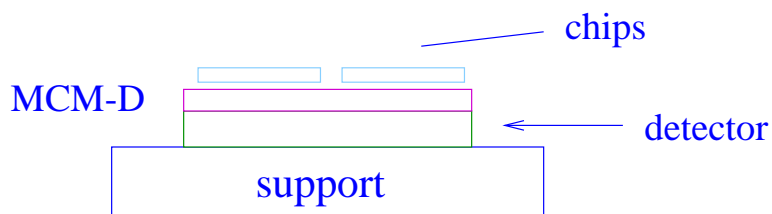
Each one has **pros** and **cons**: more studies are needed to decide

● "wireless" application: an MCM-D approach



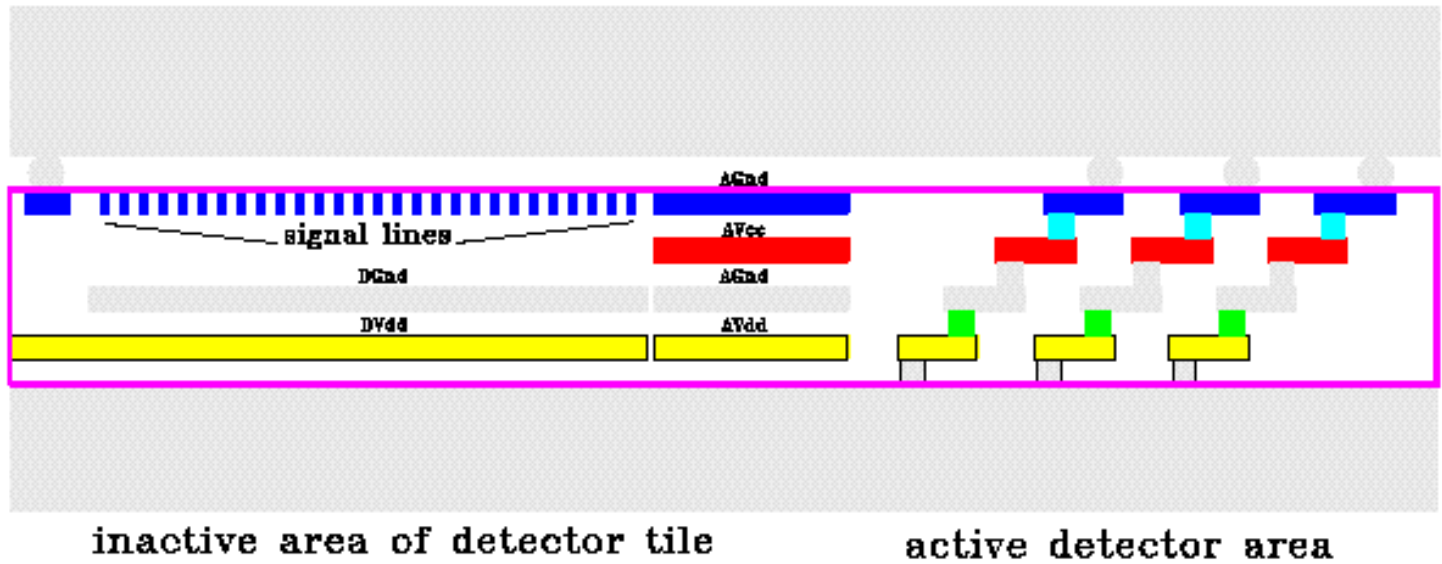
MCM-D = Multi Chip Module with Deposited Dielectric:

- thin film technology
- interconnections formed depositing dielectric material (BCB = benzocyclobutene, $\epsilon_r = 2.7$) and conductors on the junction side of the sensor:



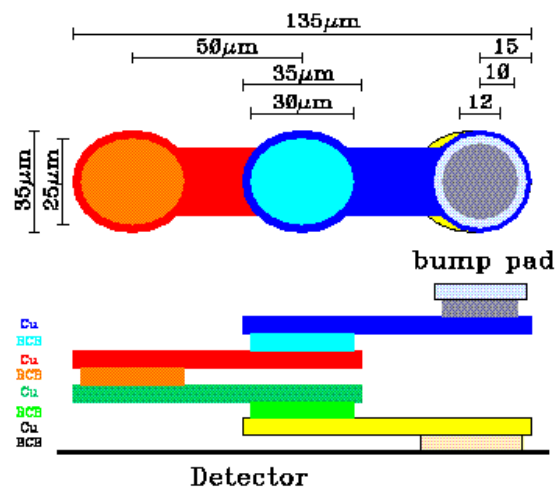
a study by the Wuppertal team + IZM, IMEC for the ATLAS pixels:

Readout Chip



main characteristics:

- 4 copper layers, for the signal & power bus at the chip edge (thickness: 4-10 micron/layer)
- traces: 20 micron width, 2 micron thick, 30 micron spacing
- interconnection of the pixels to the front-end cell through a "staircase":



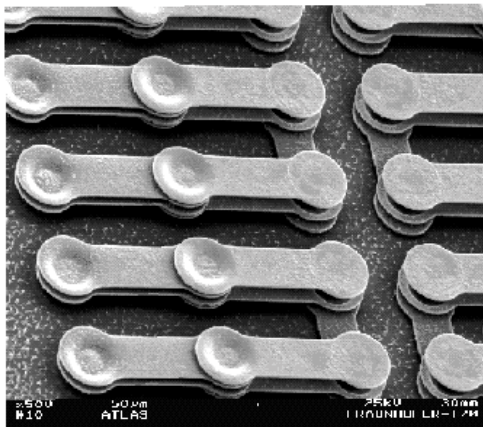
- no wire bonding: Front end I/O also connected by bump bonding

strong points:

- wireless, robust, "monolithic"
- "easy" to implement a mounting scheme limiting the stress induced by CTE mismatches on the bumps

critical issues:

- wireless, robust, "monolithic"
 - => the fault rate on the bump bonds HAS to be at the 10 ppm as the chips I/O are also bump bonded
 - => the staircase feed through connections from the pixel cells to the mating front end cell has to be quite reliable...

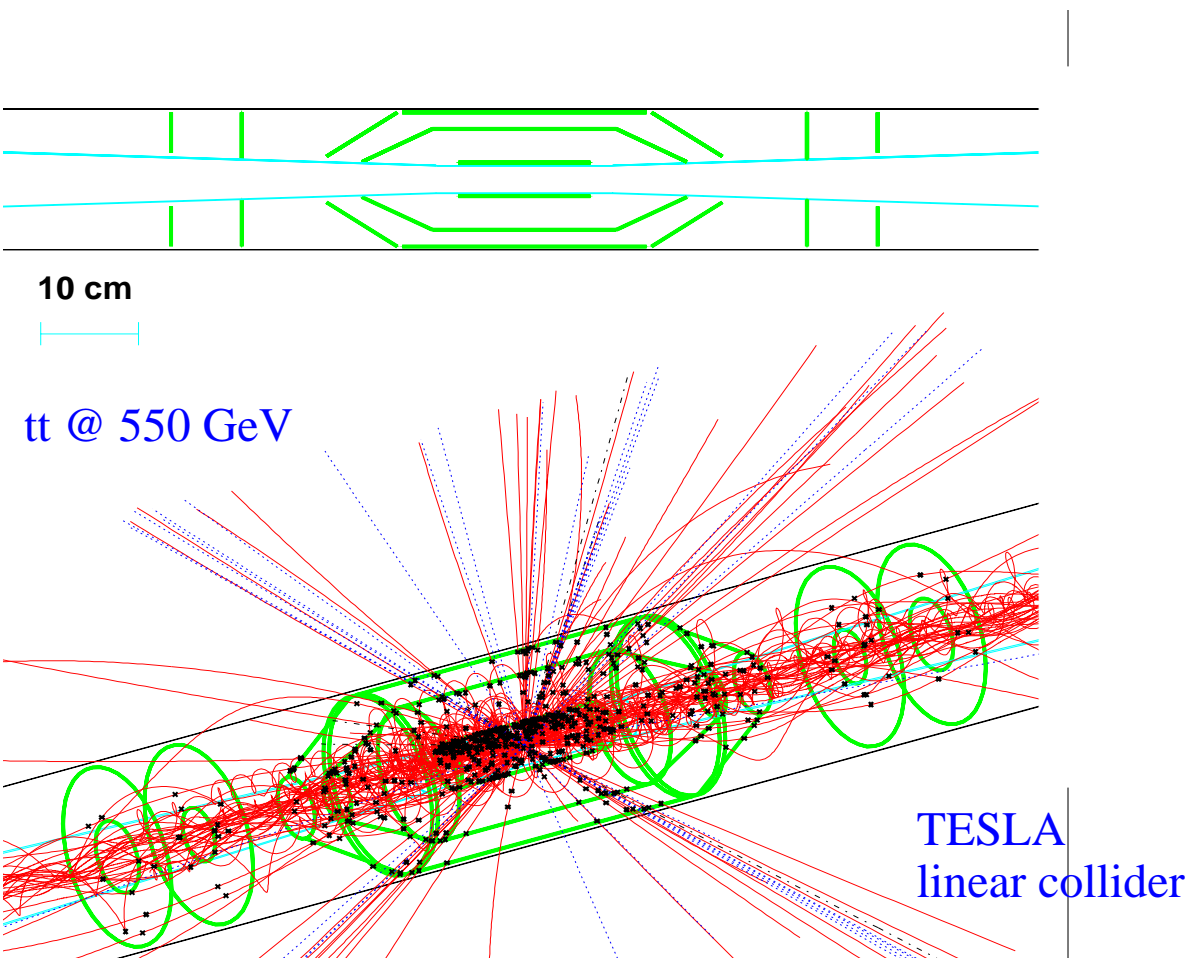


- 4 vias / cell
- ~ 250 000 vias/ module

=> the interconnection is necessarily tested after it has been grown on the detector substrate, so it has to be made sure the MCM-D process can be re-done on the same substrate

conclusions on power & signal bus

- The "flex" hybrid technology is "under control"; special care should be paid to mounting issues (stress on bumps and wire bonds)
- The "integrated" technologies are certainly appealing but processing optimization is still inder way



ext generation of Pixel detectors will require:

- higher resolution (~ 5 micron)
- (much) less material ($< 0.3 \% X_0$ / layer)

will be more compact....

following the trend in the consumer electronics for portable devices:

