PIXEL DETECTOR for X-Rays Experiments

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SUMMARY

A CRISTALLOGRAPHY EXPERIMENT

- Set-up
- Detectors in use and limitations

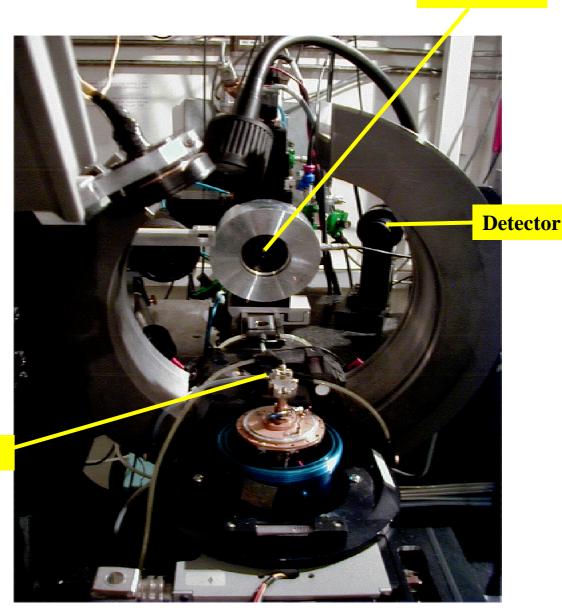
• THE D2AM/ESRF PIXEL PROJECT

- Main goals for a new detector
- The XPAD chip
- From prototype to final design
- Modules and staves
- Read-out scheme

• CONCLUSIONS

EXPERIMENTAL SET-UP

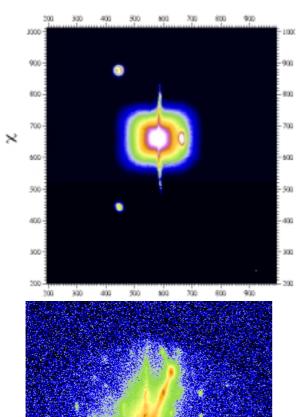
Beam out

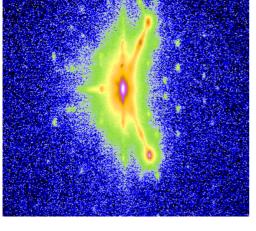


Sample

Courtesy of J.F. Berar/ESRF

CCD DETECTORS





100

Courtesy of J.F. Berar/ESRF

Detectors currently in use:

• Direct illumination CCD

- High number of charge for 1 X photon > Low dynamic range (100 ph/pixel)
- Small pixels (20μ) / to be compared to the source size $(200*200 \mu m)$

• Phosphor + optical demagnifier+CCD

• Low statistical accuracy (due to the 4 transformations)

$$vx \rightarrow vv \rightarrow OF \rightarrow charges$$

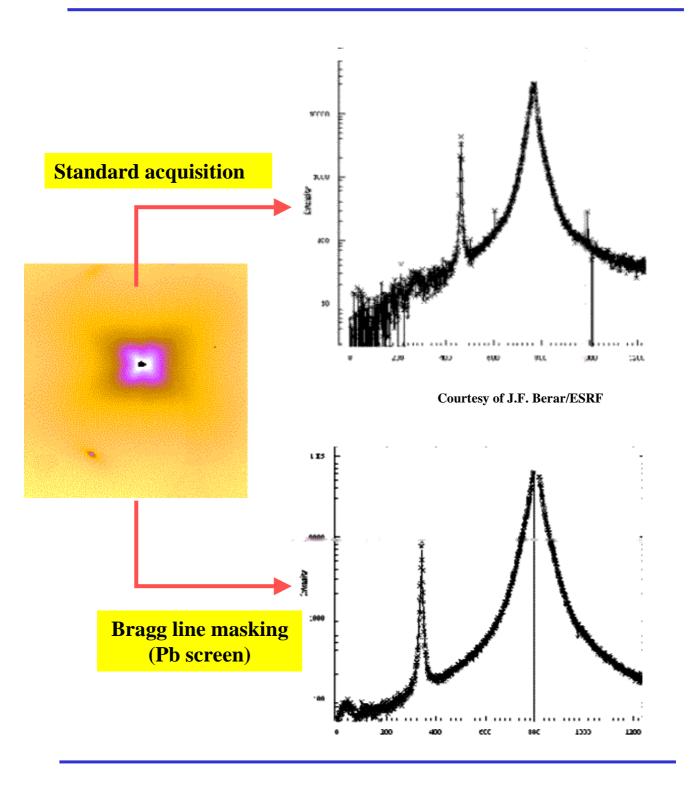
• In both cases:

- Dynamic range not sufficient (~14 bits / satellite peaks could be 1/1000 of peak intensity but well above background)
- Residual error on ZERO level (see next slide)

1000

10000

LIMITATIONS ...



The D2AM/ESRF project

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MAIN GOALS ..

MAIN GOALS OF A PIXEL DETECTOR FOR CRISTALLOGRAPHY

• X-RAY ENERGY: 5 to 25 keV

300 μ m thick silicon would be acceptable. ($100\% > \mathcal{E} > 13\%$)

Low threshold will be a challenge ($5 \text{ keV} \longrightarrow 1300 \text{ e}$ -)

- PIXEL SIZE: must agree with ESRF source image ~200 μm*200 μm
 330 μm*330 μm pixels for prototype
- COUNTING RATE:

As high as 10 7 photons/second/pixel

• SENSITIVITY / BACKGROUND :

In diffuse scattering, satellites peak counting could be less than 1 ph/s/pixel

- **REAL TIME STUDIES**: Chemical studies up to 1ms/frame with 100 frames capacity
- MECHANIC : Detector will be carried by a goniometer arm (<< 10kg)

THE XPAD CHIP

The XPAD (X-Ray Pixel with Adaptable Dynamics) chip:

- 25*24 (330µm2 pixels) matrix
- AMS 0.8 µ CMOS technology
- 2 stage differential amplifier with pz cancellation (next slide)
 - •1st stage with DC feedback

• Differential discriminator

- •4 bits tunable threshold
- •designed for positive charges but working also with negative pulses (*suitable for CdTe detectors*)

• 16 bits counter/pixel

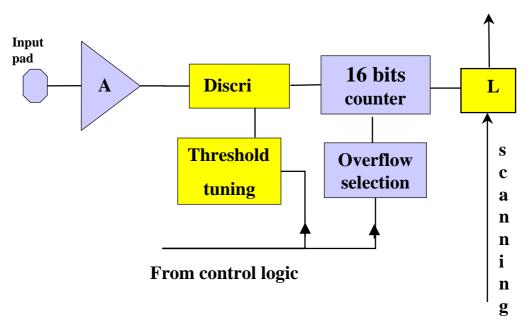
- •Selectable overflow
- •Read-out during data collection
- •40 MHz read-out possible (simulated at 100 MHz)

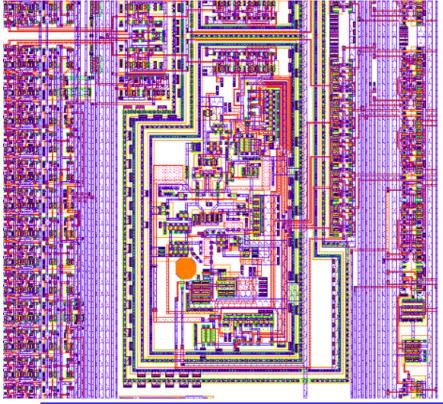
ATLAS F-Ends like Control Logic

• Power consumption

•80 μW/pixel

THE XPAD CHIP



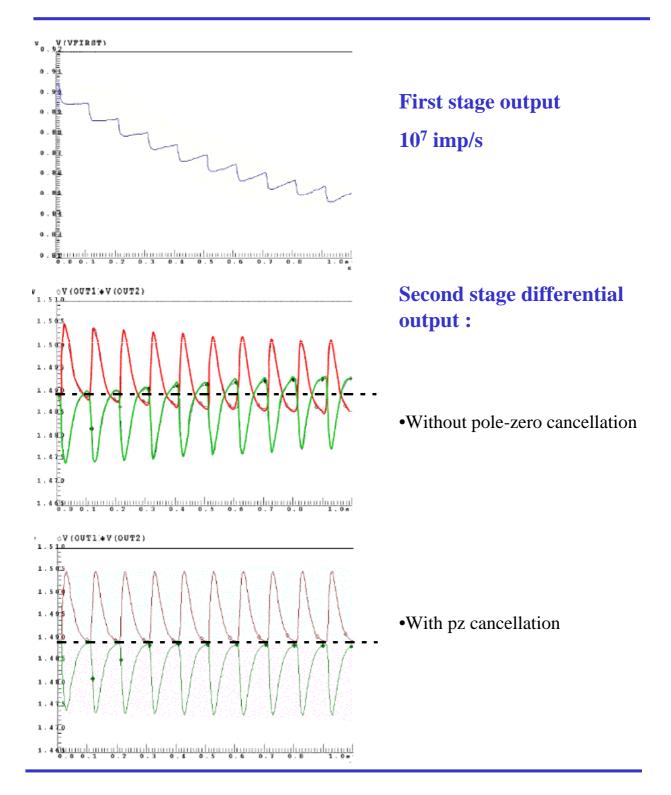


Foreseen scan clock 33 MHz

Overflow scan duration:

18 µs for 1 chip

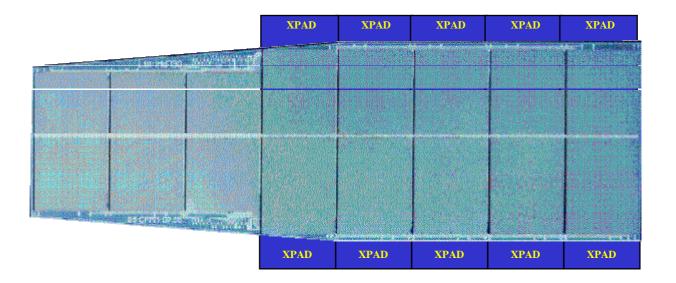
THE XPAD CHIP



DETECTOR PROTOYPES

FROM PROTOTYPES TO FINAL DETECTOR:

• Prototype using old DELPHI detectors:



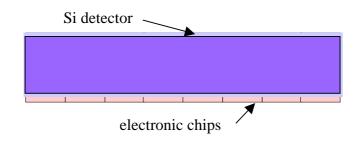
- 10 XPAD chips will be bump-bonded on 1 detector (TRONICS, 120 µm Pb/lead)
- Cost effective solution but pad input capacitance high
- Active area: 41*16 mm (small but to be compared with 50*50 mm CCD)
- •10 of this prototypes expected in Sept. 2000

DETECTOR DESIGN

MODULE:

=> 8 chips of 16 x 8 mm² active area (*Note the unusual size*) on one 64 x 16 mm² Si detector

Pixel size 250*250 μm
64*32 matrix
2048 pixels/chip

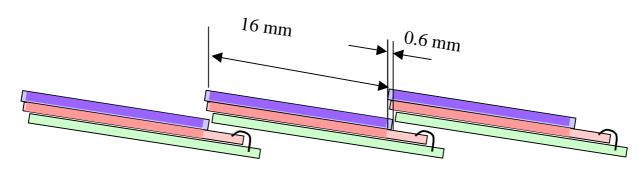


16kpixels

SUPPORT:

=> 4 modules on an ceramic

64kpixels

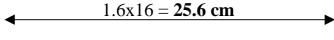


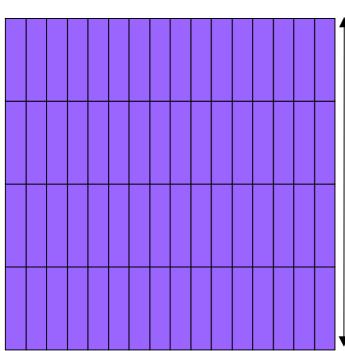
Support's arrangement

DETECTOR DESIGN

DETECTOR:

16 staves of 4 modules (512 chips)





Dead area problem:

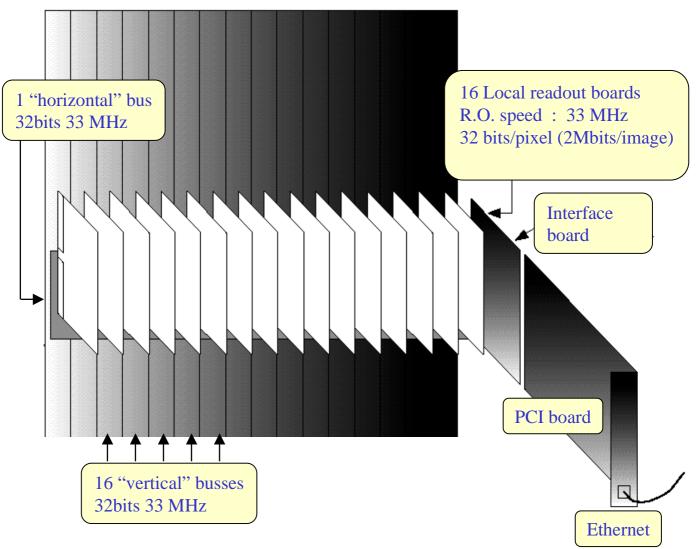
5 => Overlap along the small dimension of the model

 $\sim 0.6 \text{ mm} / 16 \text{ mm} = 3.8 \%$ dead area

=> Overlap along the long dimension of the module : $\sim 6 \text{ mm} / 256 \text{mm} = 2.3 \%$

No overlap in Z allows 4 modules in 1 ceramic **(32 chips)**

GLOBAL READ-OUT SCHEME



• Data scan every 5 ms (1 overflow every 6.4 ms at 10⁷ ph/s

1 ms < Scan duration + data handling < 4 ms)

- Complete image recording after exposure : 3ms
- Local memory storage: 128 images
- Expected read-out via Ethernet: 3 to 30 images/s

CONCLUSIONS

- First results of XPAD (without detector) in the next month
- Hybridations foreseen in August 2000

At this moment we will have an usable detector for cristallograhy experiments

• Studies of this prototype in real conditions :

Threshold, counting rate, radiation problems? ...

• Few chips to be hybridized with CdTe detectors (and AsGa)

Efficiency improvement (at 30 keV, 100 µm CdTe = 3 mm Si)

• Electronic final design during next year