

ATLAS
BUMP BONDING PROCESS

BUMP BONDING PROCESS

Bumping

Requirements:

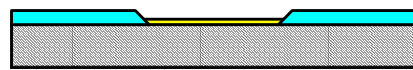
- Pitch: **50 μm**
- Density : **≈ 5000 contacts/cm²**

Bump Material: **INDIUM + Under Bump Metal**

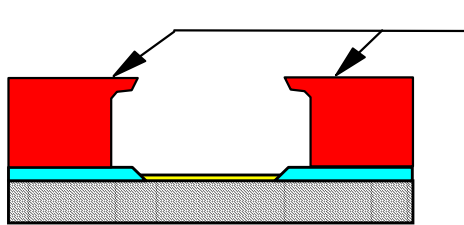
Process: **LIFT OFF**

Deposition technique: **e-BEAM
EVAPORATION**

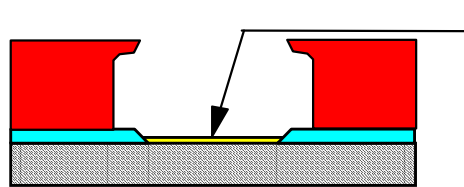
BUMP BONDING PROCESS



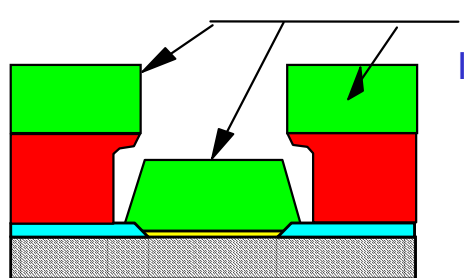
Wafer Cleaning



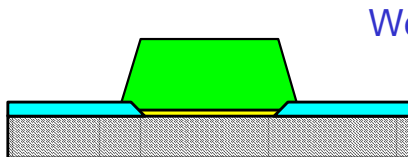
Photolithography



Plasma activation



Evaporated Indium



Wet Lift off process

Process parameters:

- **Resist Thickness: 15 μm**
- **Pre-bake: 30min@80 °C**
- **Deposition rate: 0.5 $\mu\text{m}/\text{min}$**
- **Dep. Pressure: 9×10^{-7} Torr**
- **T during Dep.: < 50 °C**

BUMP BONDING PROCESS

BUMPING RESULTS

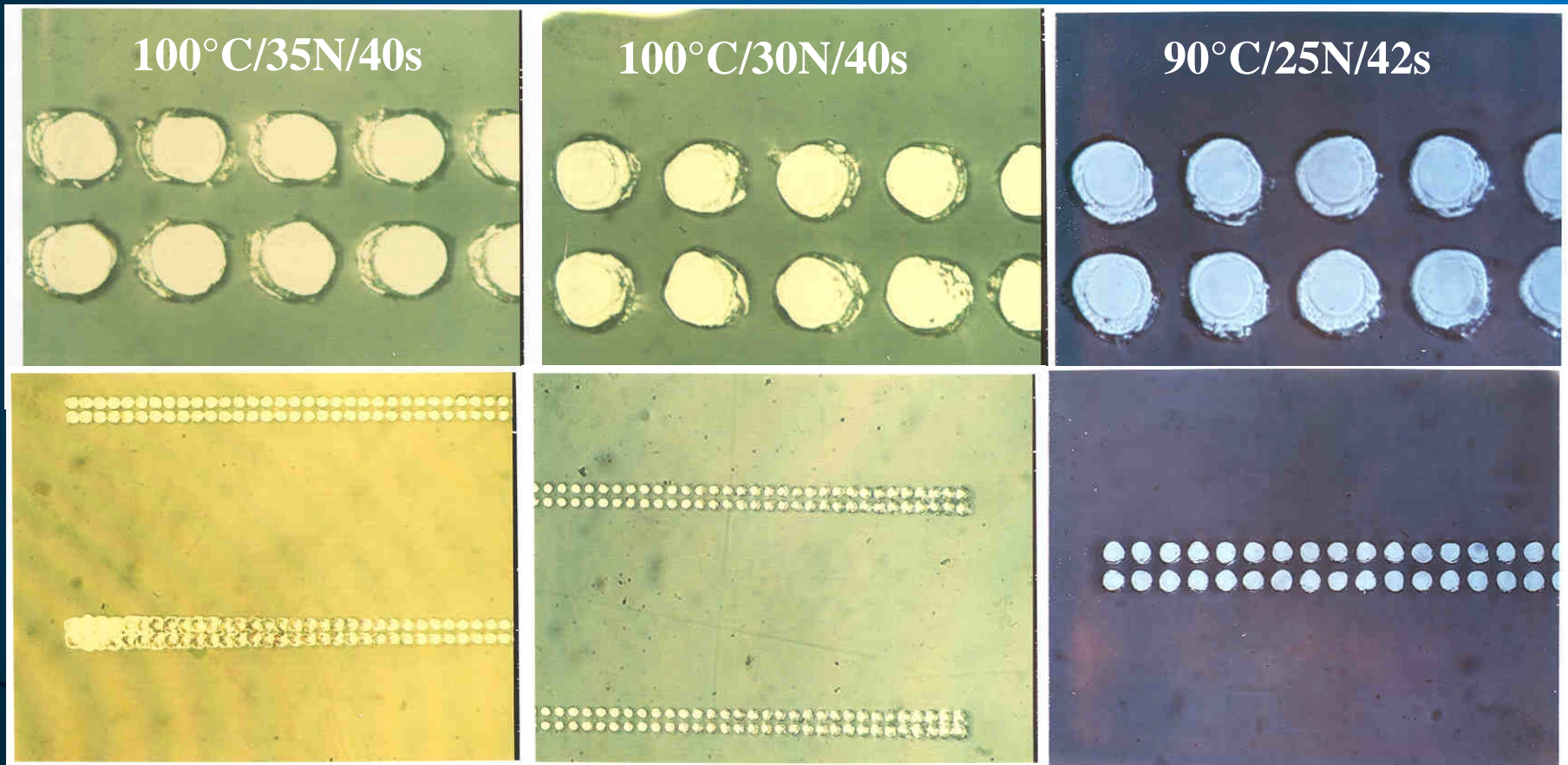
- Final Bump Thickness: $6.8 \pm 0.2 \mu\text{m}$
 - Thickness uniformity: $\pm 3000 \text{ \AA}$ (on 6" wafer)
 - Fault Rate: $2 \times 10^{-5} \pm 0.6 \times 10^{-5}$

BUMP BONDING PROCESS

Bonding

Equipment: FC 6 KARL SUSS BONDER

Parameters:



BUMP BONDING PROCESS

Bonding

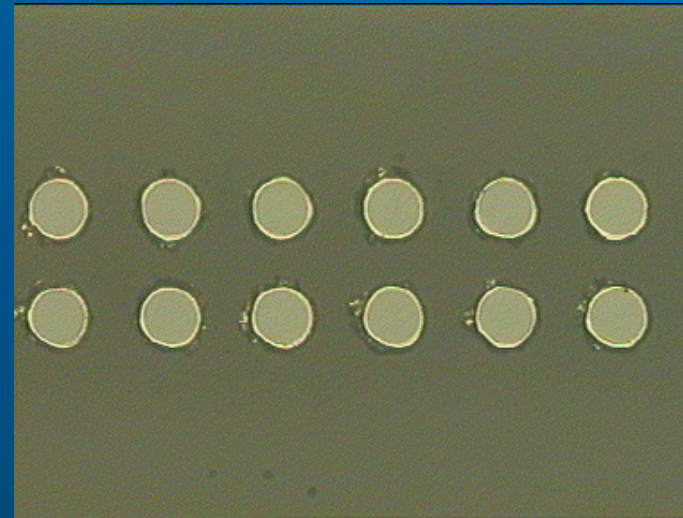
Selected parameters:

Force: 25 N (on 3800 bumps)

Substrate Temperature: 90 °C

Chip Temperature: 90 °C

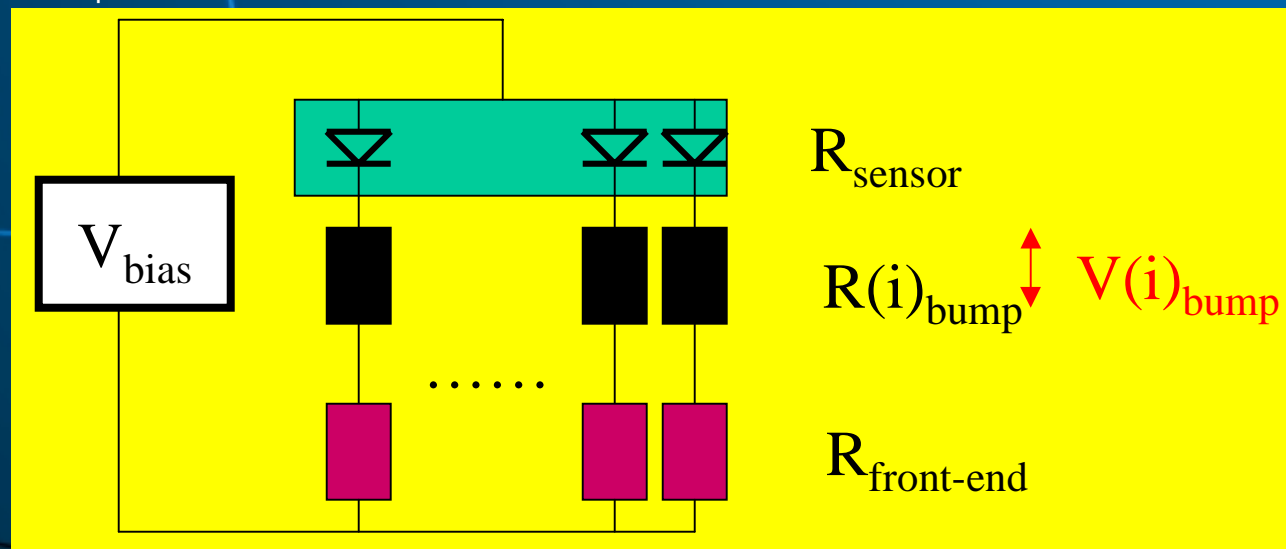
Time: 42 sec



BUMP BONDING TESTING

Electrical measurements

- Measure of bump connection resistance, which must be small ($< (100\Omega)$) not to significantly contribute to the front-end noise.
- It is well known that In develops an oxide layer once taken out of the vacuum tank where the bump deposition is done. In_2O_3 , is an insulator.
- It is desirable the oxide layer is automatically broken when the bias is applied to the sensor.
- For this to happen the resistance of the oxide must be high enough in order to develop a $V(i)_{\text{bump}}$ across it such as to break the insulating layer.

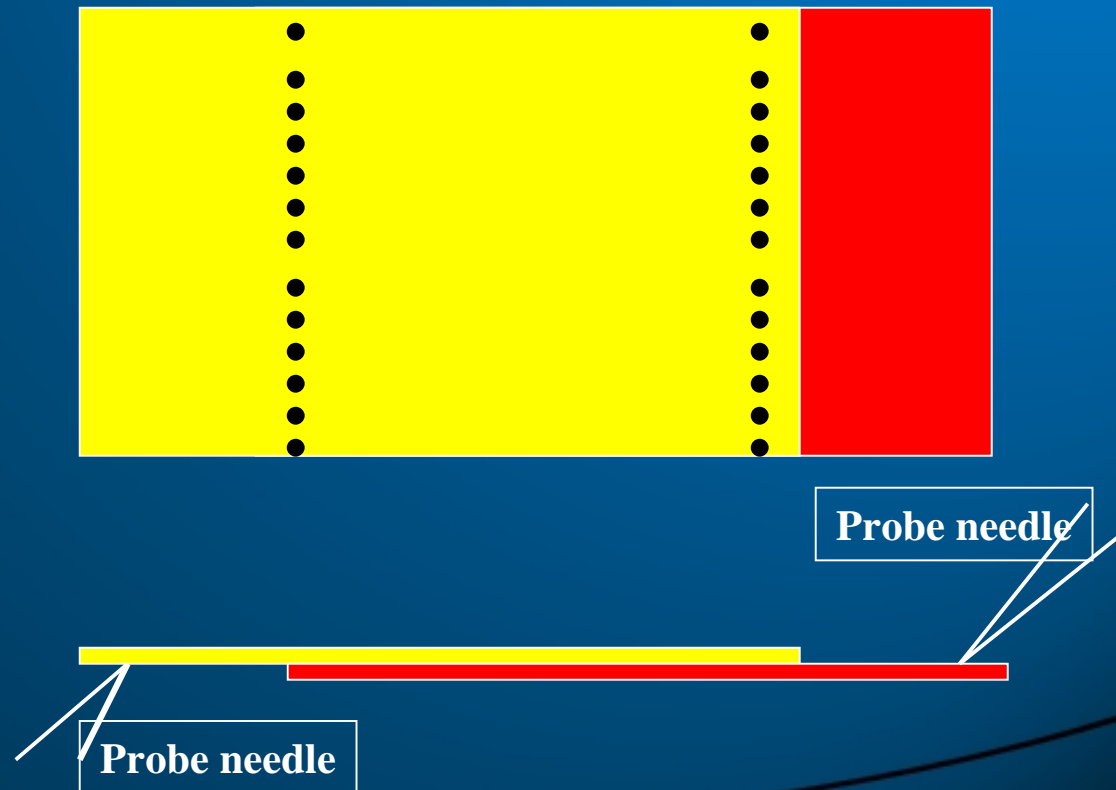


BUMP BONDING TESTING

Electrical measurements

- “electronics dummy chips” have been used but - instead of mating them to “sensor dummy chips” to build long chains, we flipped them on “electronics dummy chip” too. This allows to measure 18+18 individual bumps (through ~55 Ohm paths) along the periphery of the chips (the most critical region for our flipping process).

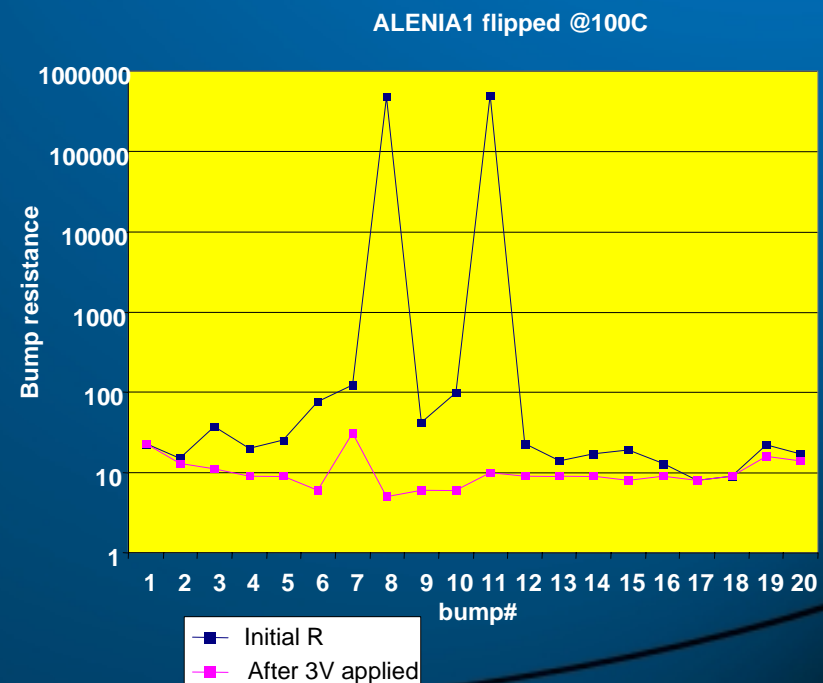
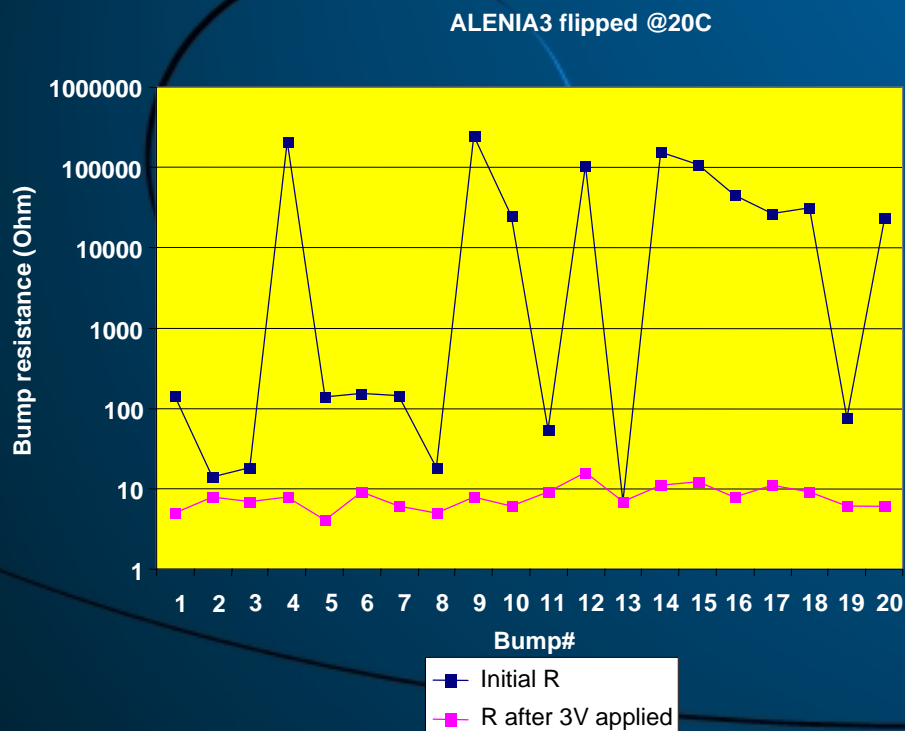
- INFN has measured the individual resistance and the breakdown voltage



ATLAS-Pixel Project: *Bump Bonding*

Electrical measurements

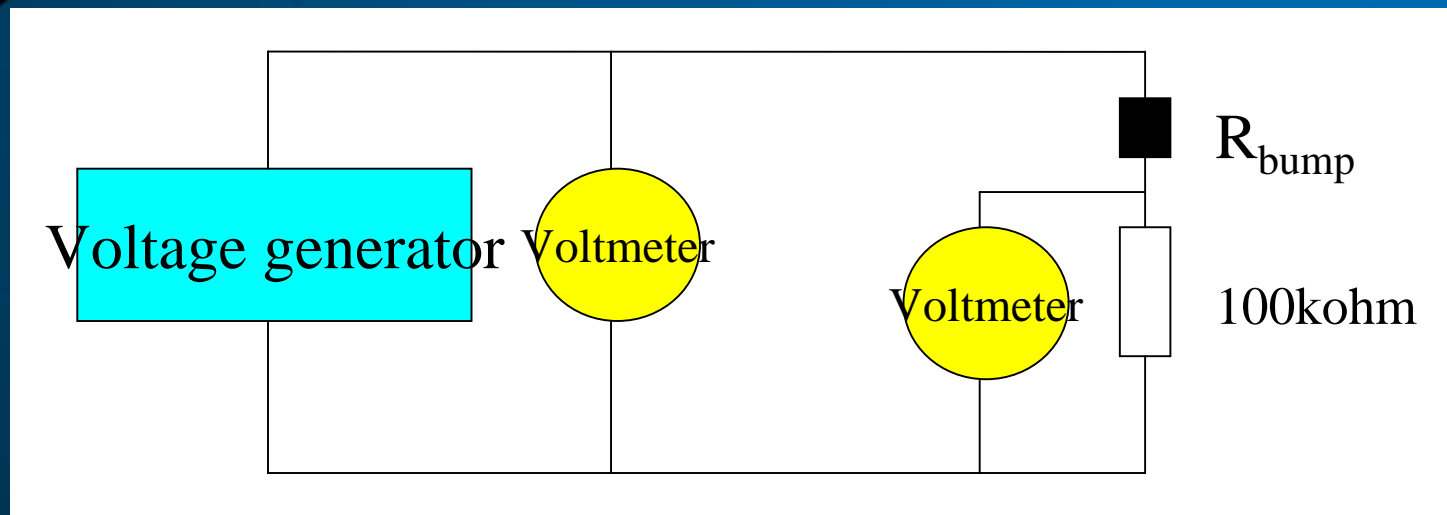
- Samples at 20C and 100C have been bonded
- First the resistance of the bumps as measured with a digital ohmmeter for 10+10 bumps, before and after applying 3V through an ordinary battery.
- It can be observed that:
 - @20C half of the bumps have initially an oxide layer while at 100C this happens in only 10% of the cases;
 - once the oxide is broken the bump resistance is uniformly low (~10 Ohm);



BUMP BONDING TESTING

Electrical measurements

- Measuring resistance with a digital meter we apply a voltage across the bump. The value of this voltage depends on the resistance to be measured (few mV @60 Ohms, 200mV @100kohm, 600mV @2Mohm)
- In order to explore the region below 200mV and to understand where the oxide breaks in case a constant voltage is applied the following set-up has been used



- It is possible to apply a known voltage across the bump and measure the resistance at the same time.

BUMP BONDING TESTING

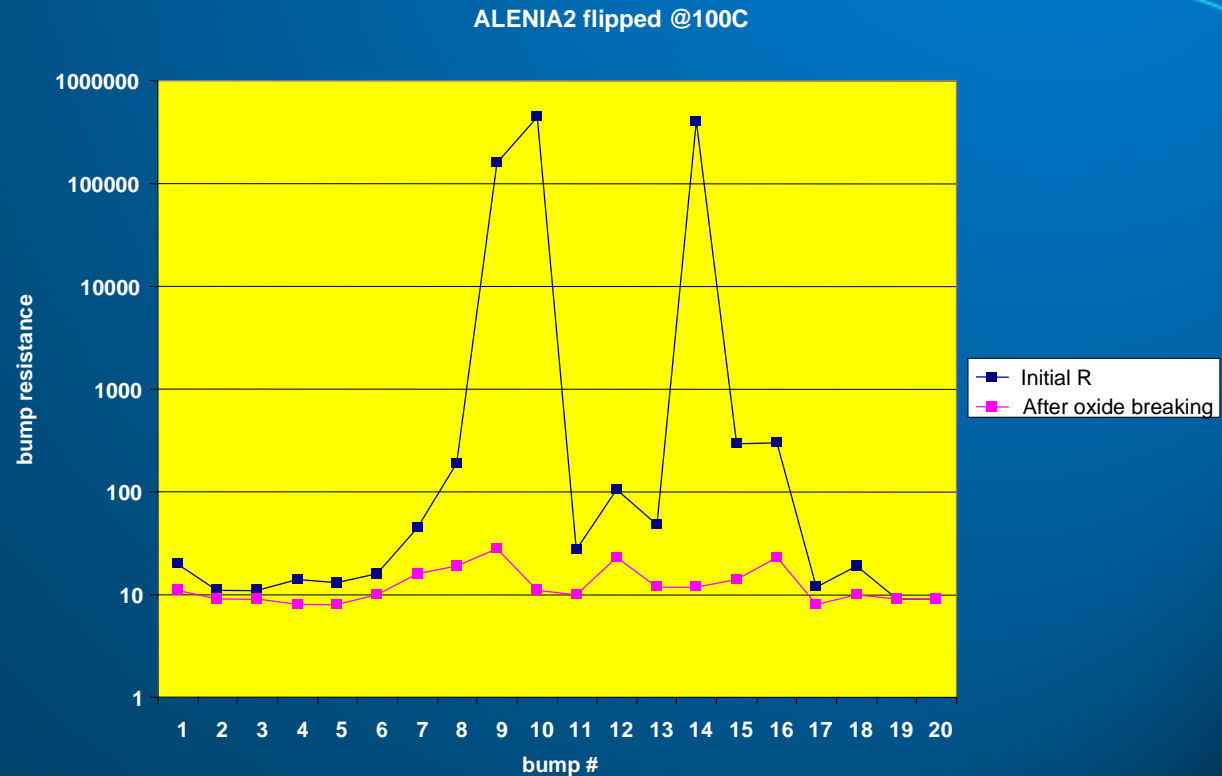
- Ramping the voltage tell us where the oxide breaks

Breaking happens at ~0.5V if flipping @20C and @4.3V for the unique case @100C, indicating a thicker oxide.

- With the same set-up it has also been studied how long the oxide survives if the voltage generator is set to 20mV (voltage on bump and current through it will depend on the bump resistance, but are <20mV and <200 nA)
 - Using a new set flipped @20C and looked at 20 bumps, 6 of them had large initial resistance (i.e. similar pattern as previous sample)
 - Waiting up to 30' and all oxide layers broke.

BUMP BONDING TESTING

- Then it was studied if a pulse is as effective as a constant voltage in breaking the oxide layer
- Pulses :
 - duration=10 μ sec
 - period=500 μ sec



- The bump oxide layers have been broken using pulses, instead of constant voltage

BUMP BONDING TESTING

Conclusions on Oxide Resistance

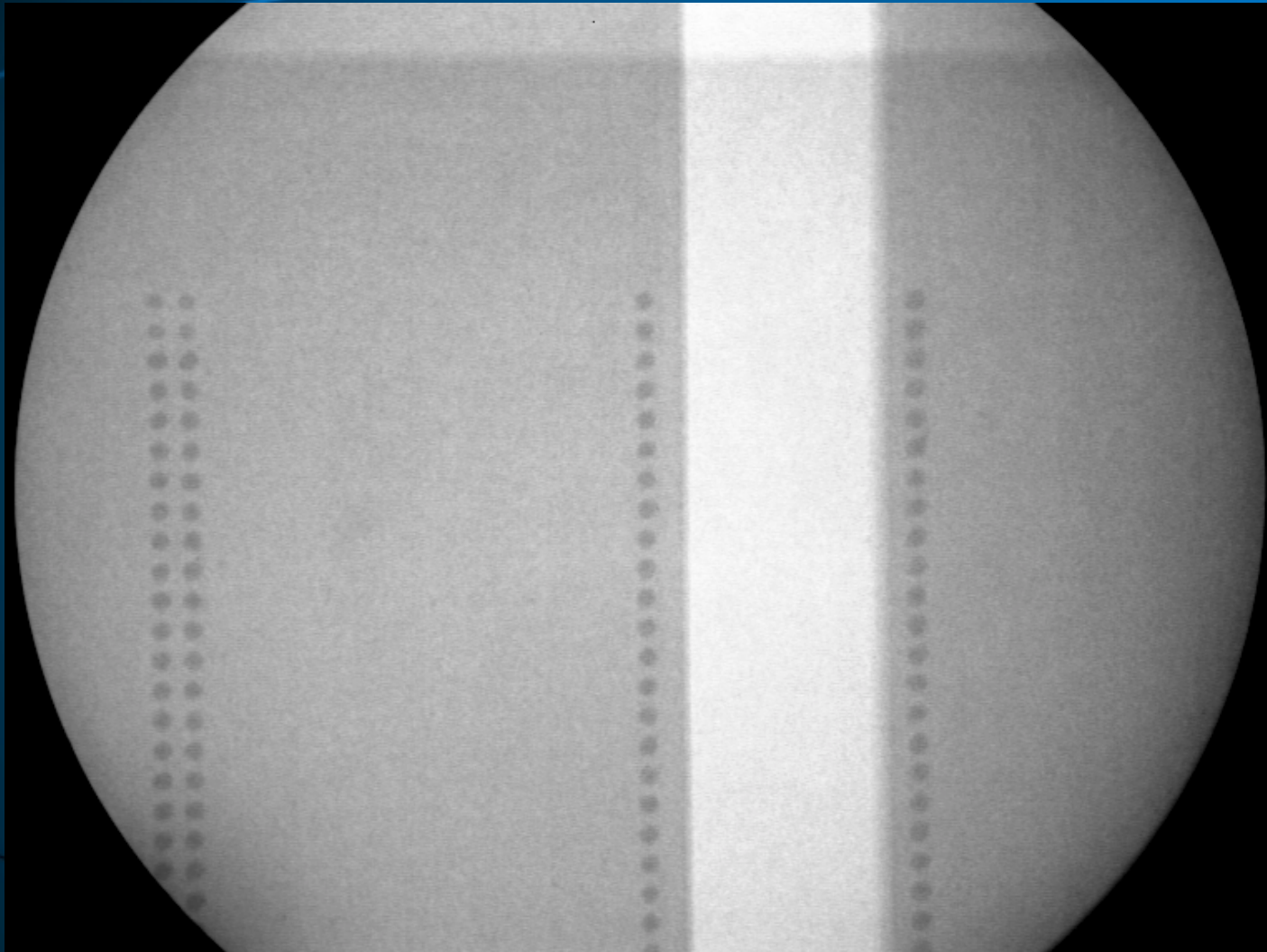
- AMS In oxide is thin (low resistance (100k)) and already broken in 50% to 90% of the cases (depends on flipping parameters). Breaking the residual oxide requires low voltages ((50mV) for minutes) either constant or pulsed and low currents ((100nA))
- The bump resistance after oxide breaking is low enough ((10 Ω)) to allow proper operation of the front-end electronics and it is stable in time
- Flipping at 100C is beneficial both for bump adhesion and for oxide breaking.

BUMP BONDING TESTING

Activity Until now :

- **12 Single chip assembling and 4 full module (1 Tile with 16 Front End Chips) have been completed and tested**
 - X-Ray radiograph
 - test in laboratory
 - test over radiation beam
- **Several “dummy chip” assembling to set parameters, mechanics, reworking, etc**

BUMP BONDING TESTING



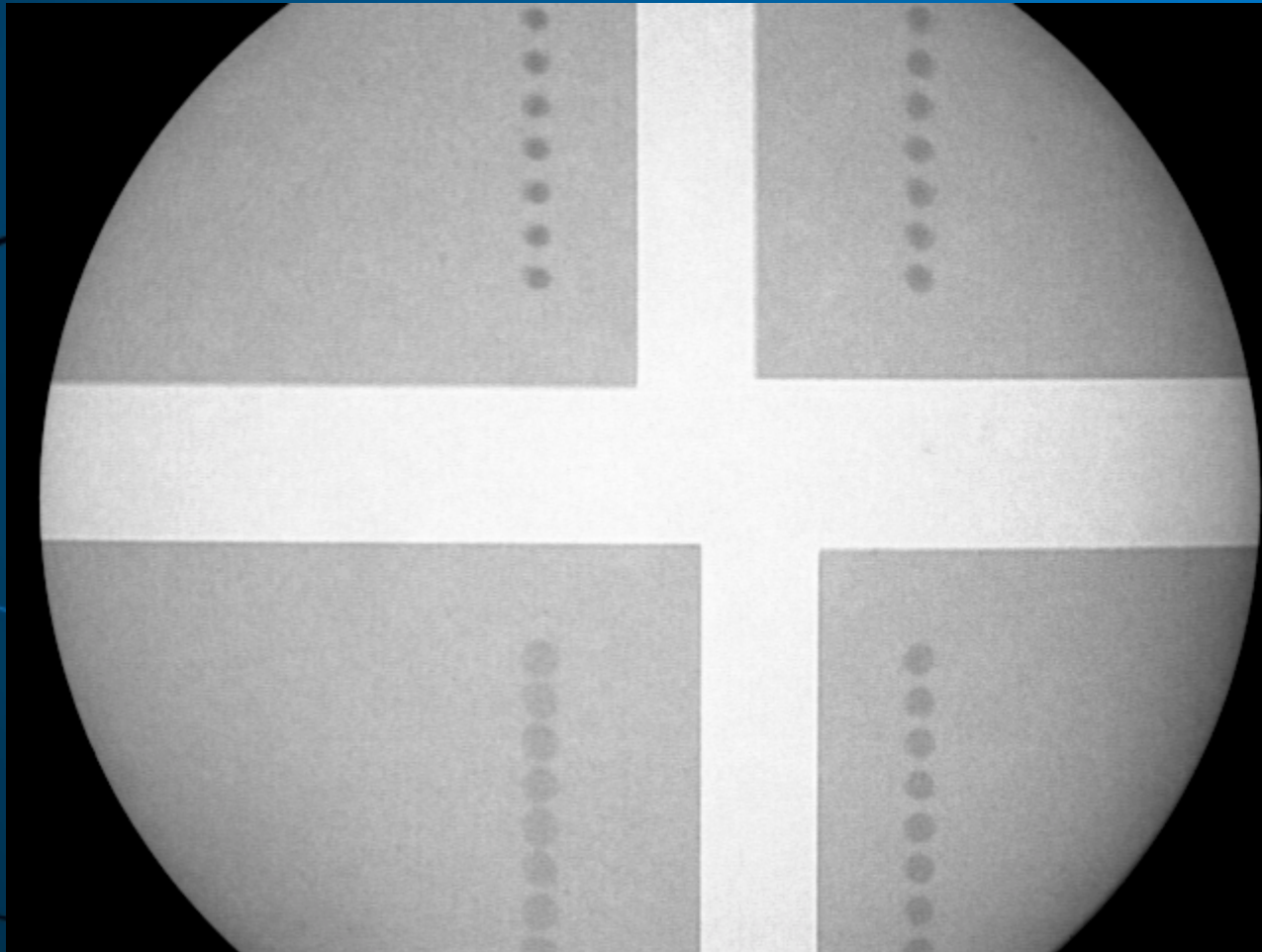
*X-ray on a full
module:*

*border between
two front end*

Good alignment

BUMP BONDING TESTING

- ~10 shorts on 50000 bumps

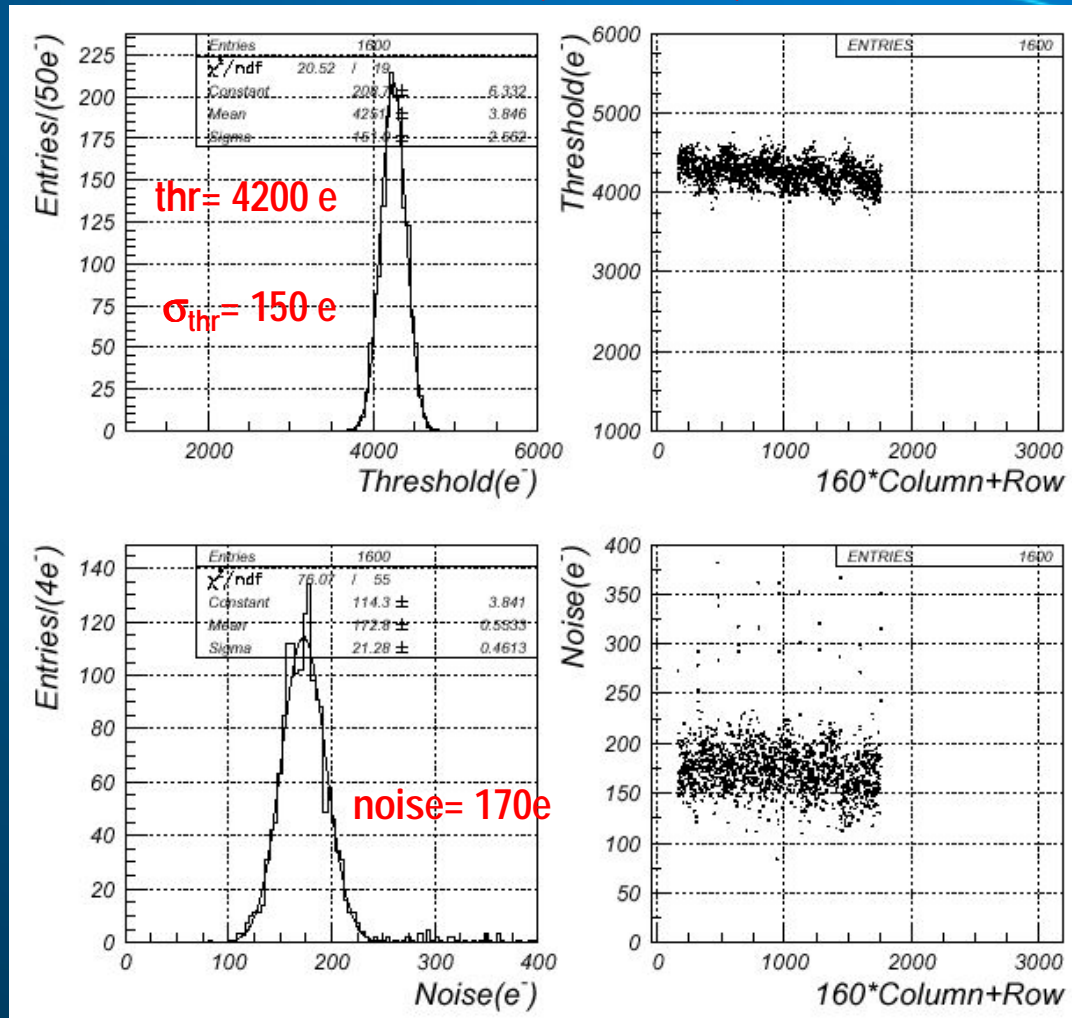


BUMP BONDING TESTING

FE_B (full-CMOS)

Lab test:

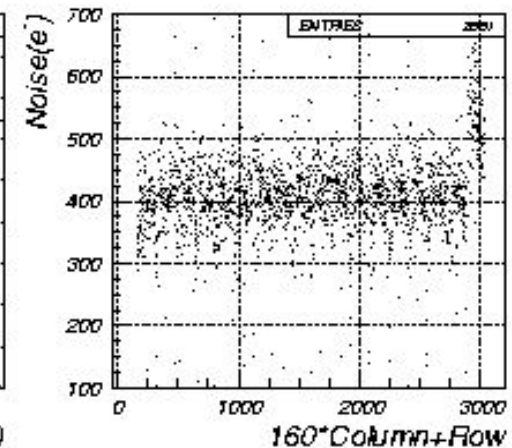
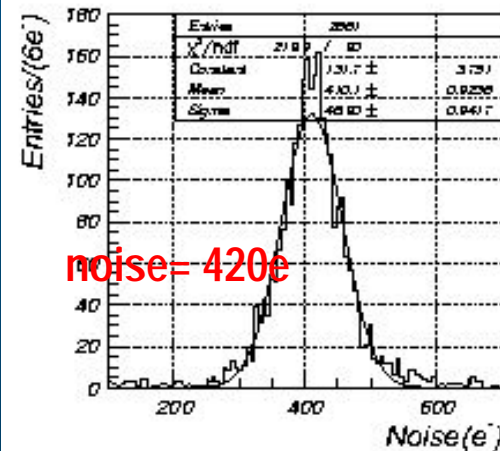
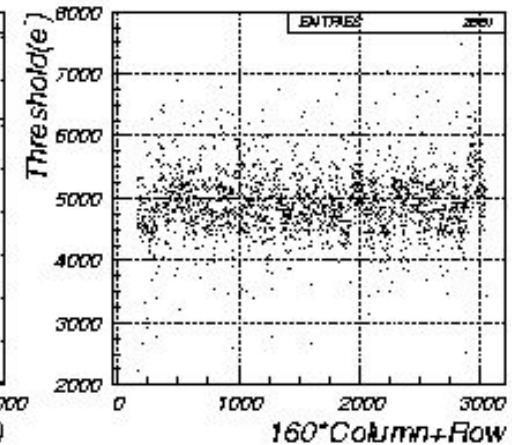
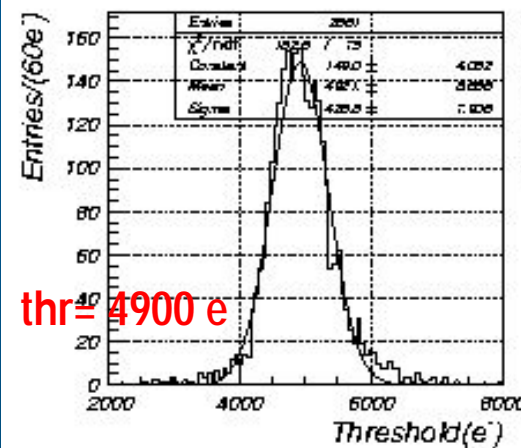
Noise and threshold dispersion



BUMP BONDING TESTING

Threshold dispersion
and noise of irradiated
Pixel Sensors

10^{15} mips/cm² ge_c_4\scan_1200

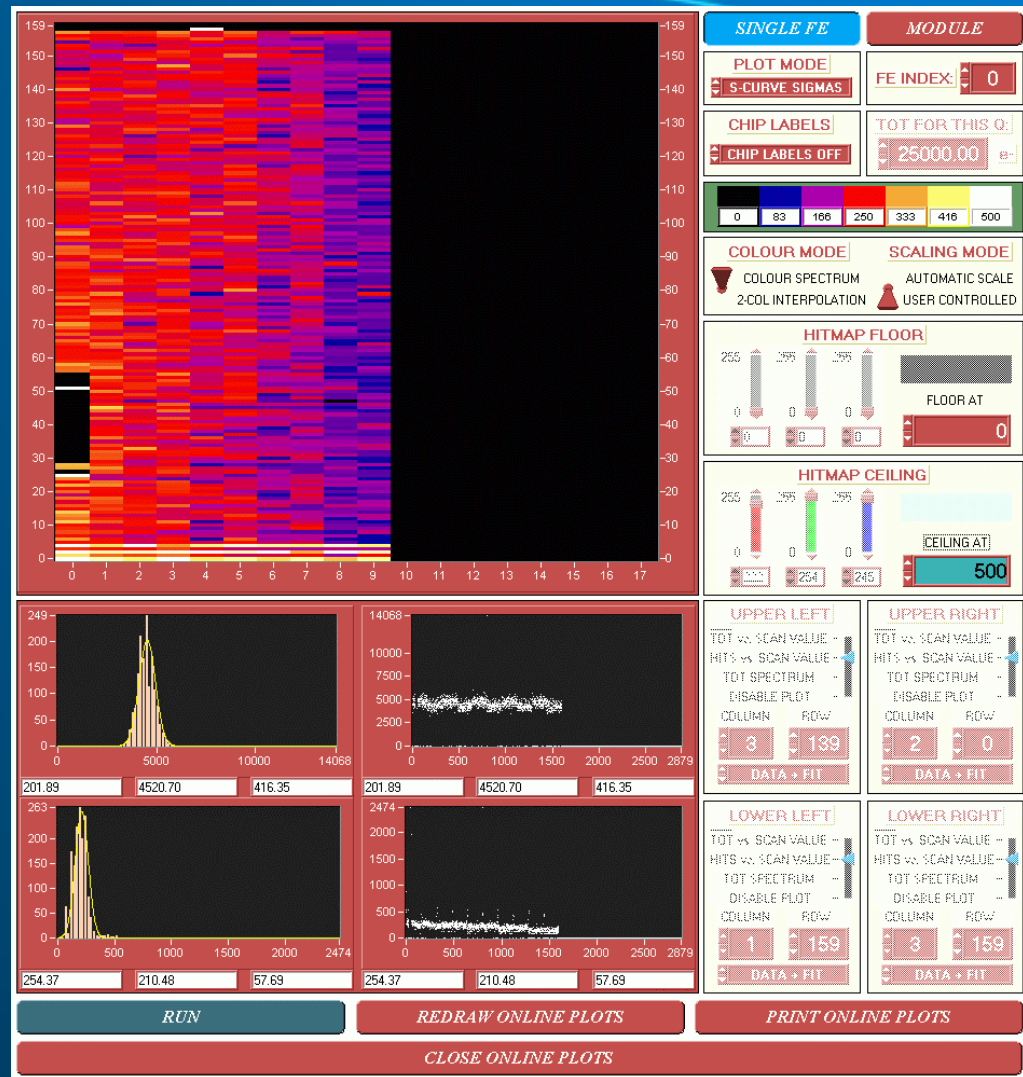


BUMP BONDING TESTING

Thresholds (4500e) and noises of a sensor assembled with a thinned (150 μm) electronics

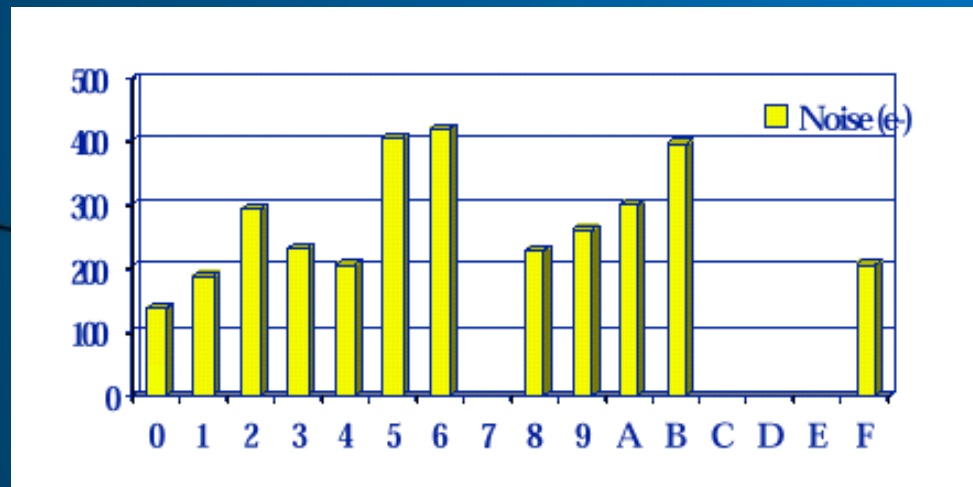
The pressure applied to bond In-bumps allow to level the warped thinned chip

Until now the thinned electronics has been assembled only by In-bumps



BUMP BONDING TESTING

Bare Module



Three chips (E, D, C) do not respond to the digital injection

One (7) is unstable and induce noise in the other:

chip 6 from 380 to 520 e-

chip 1 from 180 to 500 e-

chip 3 from 190 to 380 e-