



Pixel electronics for ATLAS

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for the ATLAS pixel collaboration

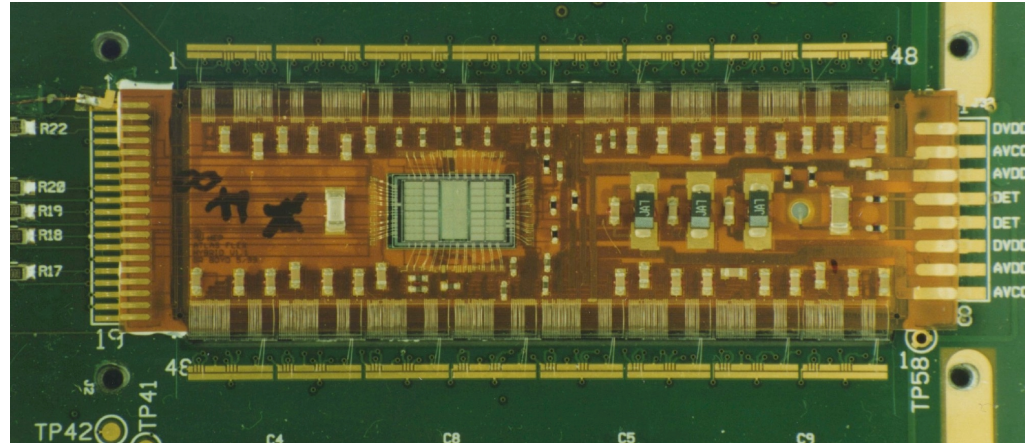
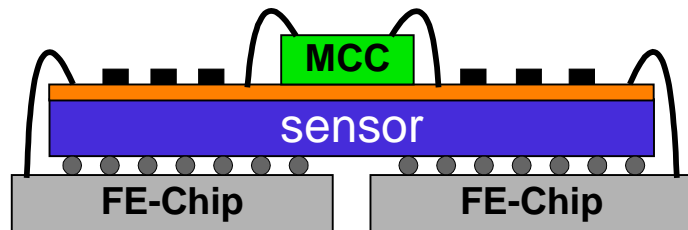
Outline

- Overview of electronic components
- On-chip electronics:
 - DORIC and VDC: chips for the optical link
 - MCC: module controller chip
 - FE-Chips: charge amplifier and readout
single chip & module performance
- Status and Outlook

The ATLAS pixel modules

Flex Capton (barrel 1 & 2, disks)

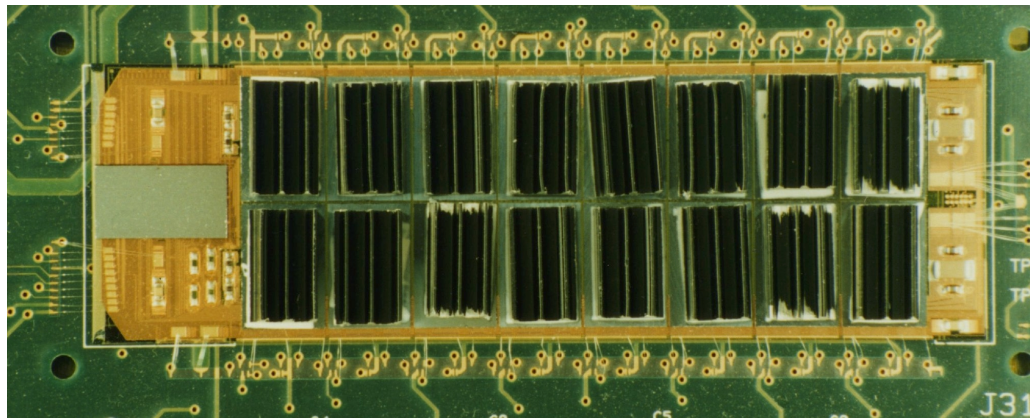
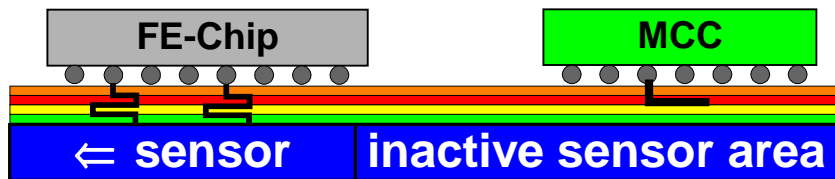
- Capton with routing glued to sensor
- Chips connected with wire bonds



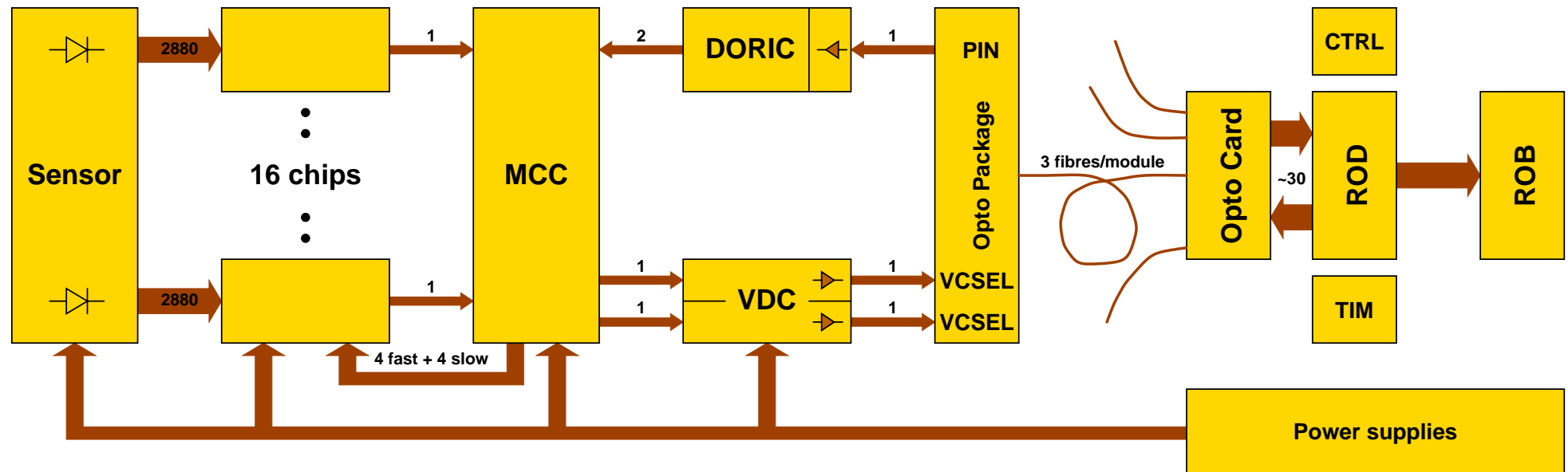
sensor: 47104 pixels, $16.4 \times 60.8 \text{ mm}^2$

MCMD (B-layer)

- Multi-layer structure (busses) on sensor
- All chips connected with bumps



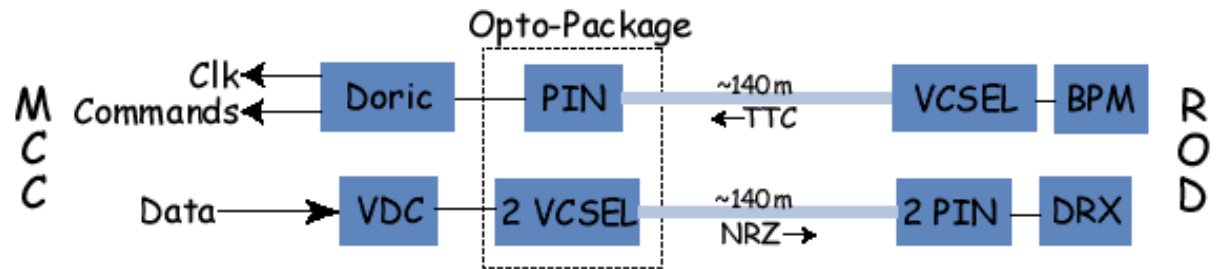
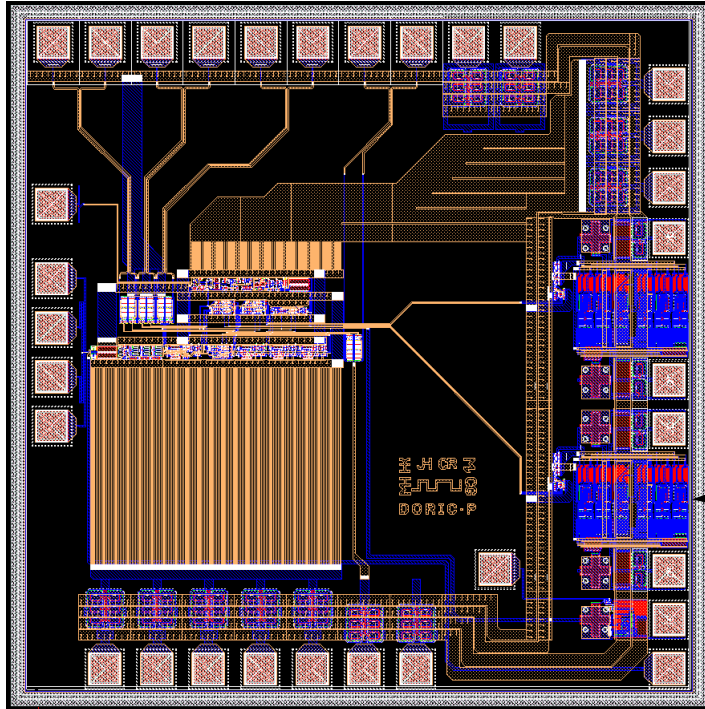
Electronic components of the pixel system



- | | | |
|----|------------------------|---------|
| 1 | Sensor | |
| 16 | front end chips | (FE) |
| 1 | module controller chip | (MCC) |
| 2 | VCSEL driver chips | (VDC) |
| 1 | PIN diode receiver | (DORIC) |

- | |
|------------------------|
| Opto Receivers |
| Readout Drivers (ROD) |
| Readout Buffers (ROB) |
| Timing Control (TIM) |
| Slow Control, Supplies |

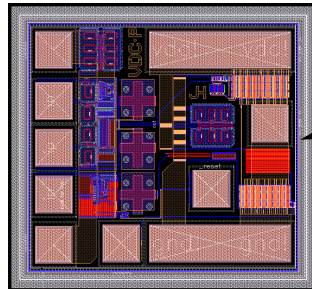
Data transmission: VDC and DORIC



DORIC:

- amplify PIN diode signal
- regenerate 40 MHz clock and data/cmd signal
- **status:** - still some problems...

DMILL
prototype chips
(Siegen, OSU,
Wuppertal)



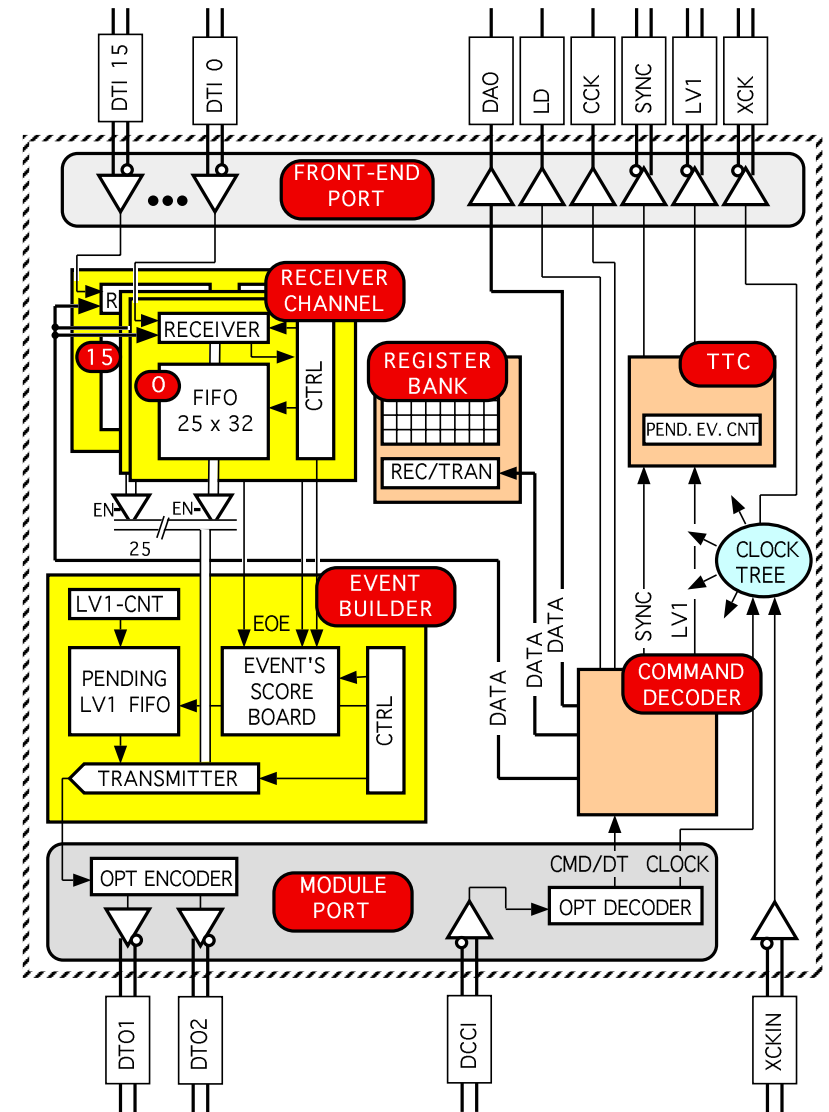
VDC:

- drive VCSEL laser (digital signals @ 80 Mbit/s)
- readjust current after irradiation
- **status:** - chip works, still under test

The MCC: Event building & Control

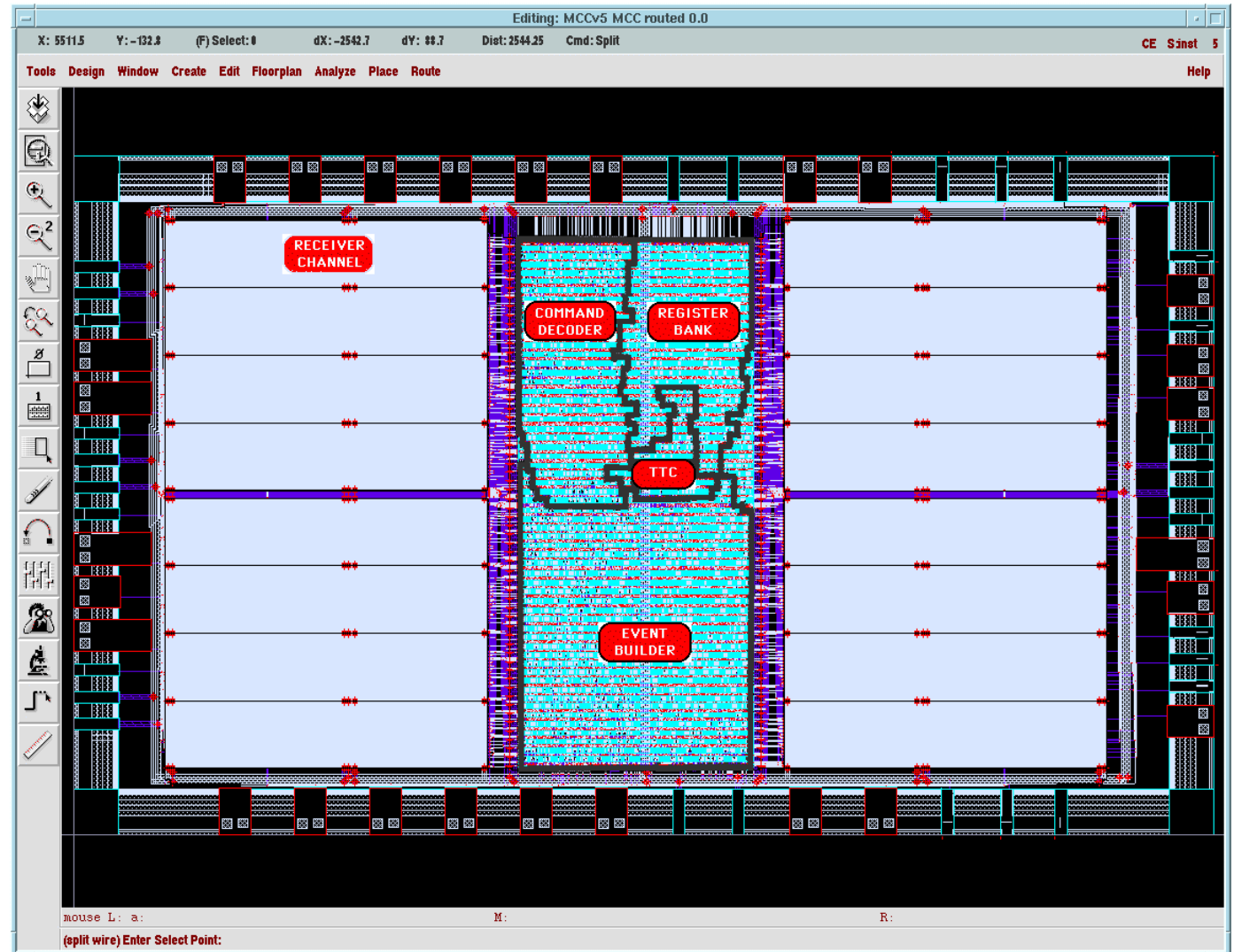
Tasks of MCC:

- Decode data/cmd signal (from DORIC) configuration data
,slow' commands
,fast' commands (trigger, SYNC, ...)
- Generate control signals for FE chips
- Receive serial data from 16 FE chips, accumulate data in FIFOs
- Check consistency of event (,score board')
- Build complete module event
- Send event to DAQ (via VDC)
- Error handling, fault conditions (disable defective FE chips, ...)



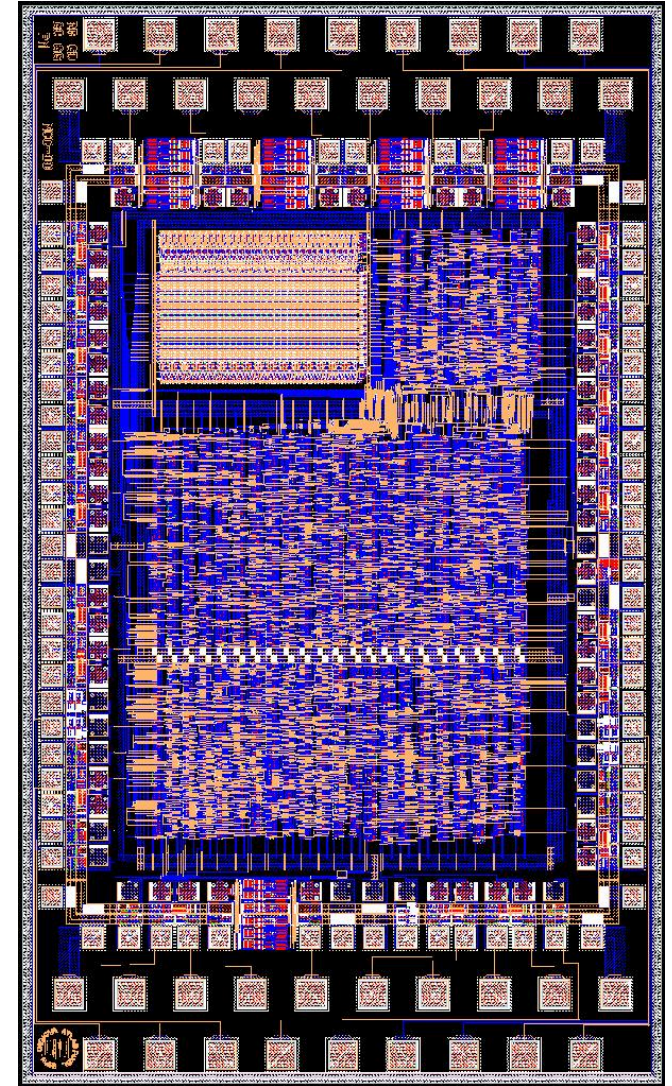
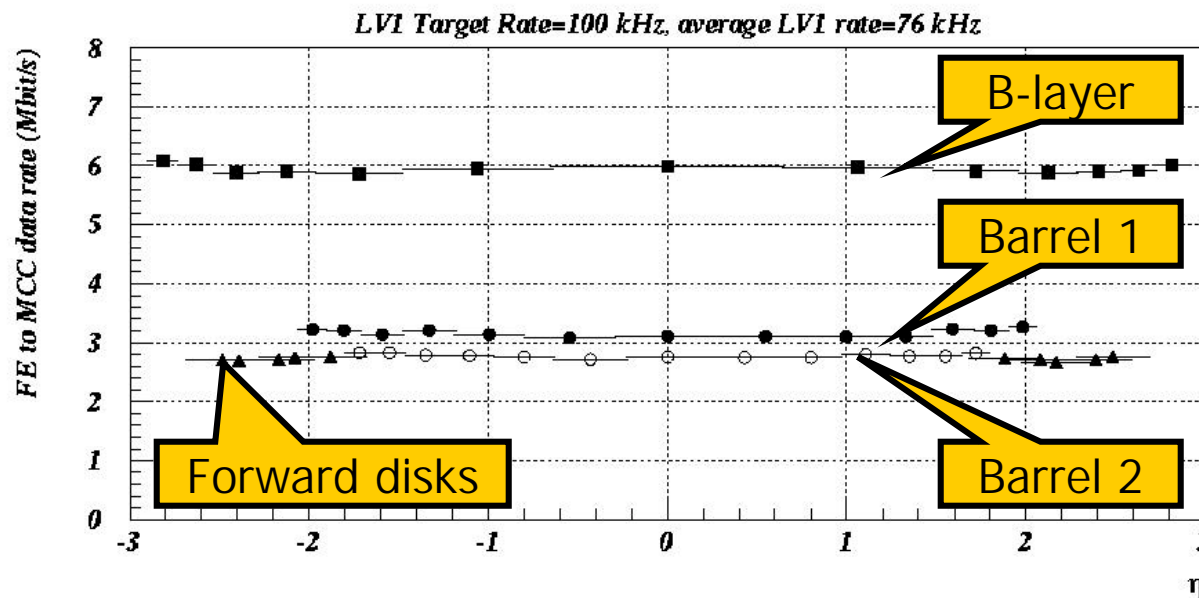
MCC: full prototype in AMS 0.8μm

- Chip is fully operational
- Has been used successfully on many modules
- Meets basically all our specifications
- Size: 6.3 x 10.6 mm²
- Uses synthesized standard cells and full custom blocks (FIFO, IO)
- Design in Genova



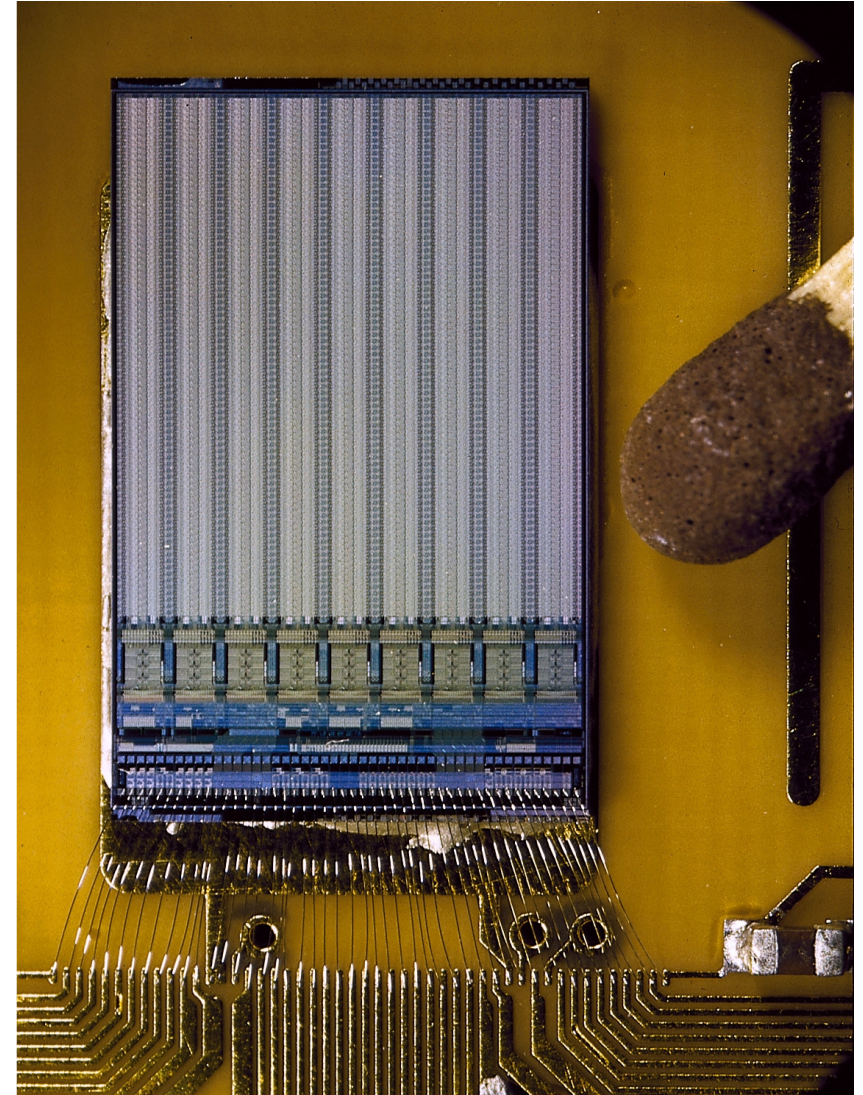
MCC-D0 prototype in DMILL

- DMILL Prototype with one input channel exists
- works @ 100 MHz
- Detailed simulations (Marseille) were done to
 - check data rates, hit losses
 - simulate error conditions
 - fix FIFO size.
- Example: data rate FE MCC per link:



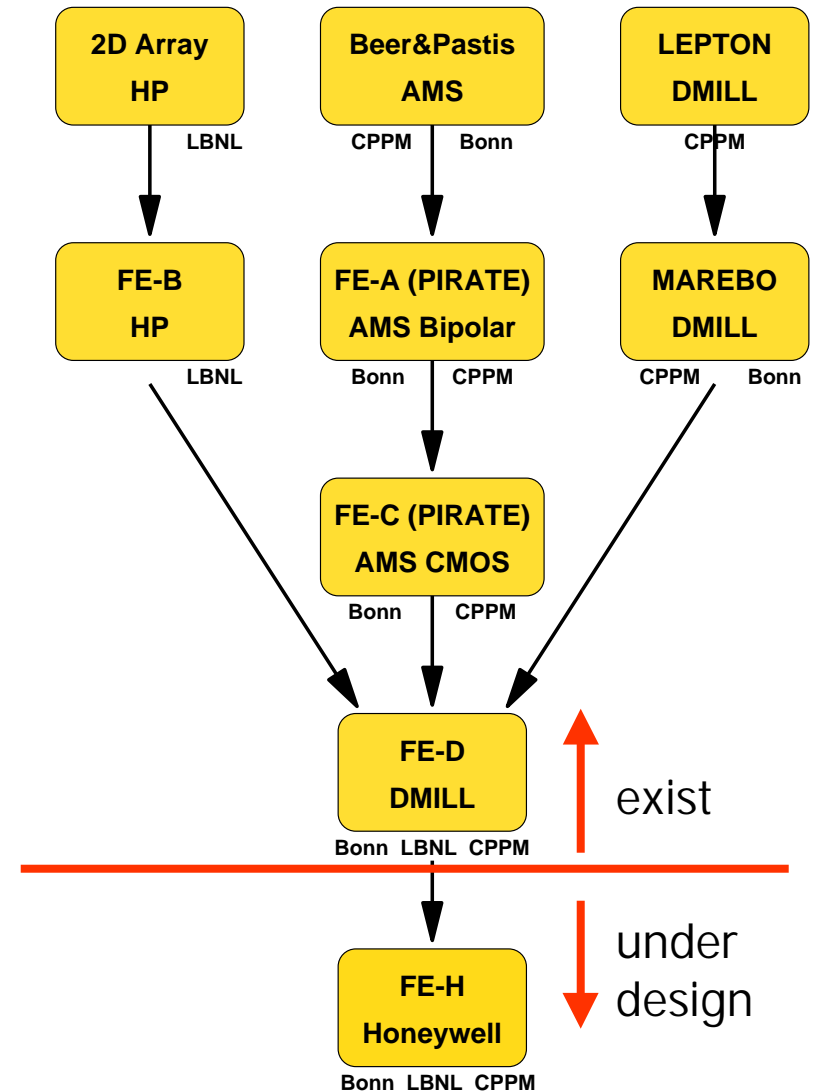
The front end chips

- Chip size: $7.4\text{mm} \times 11\text{mm}$
- Pixel size: $50\text{ }\mu\text{m} \times 400\text{ }\mu\text{m}$
- # pixels: $18\text{ columns} \times 160\text{ rows} = 2880$
- ~ 700.000 transistors
- Mirrored cells in odd/even columns
- 40 MHz readout operation
- On-chip data buffering until trigger arrives
- Serial protocol for command in and data out, compatible to MCC
- Coarse hit amplitude information by reading Time over Threshold (ToT)
- Latest chips use time stamp readout
- Fast IO signals are differential low voltage swings

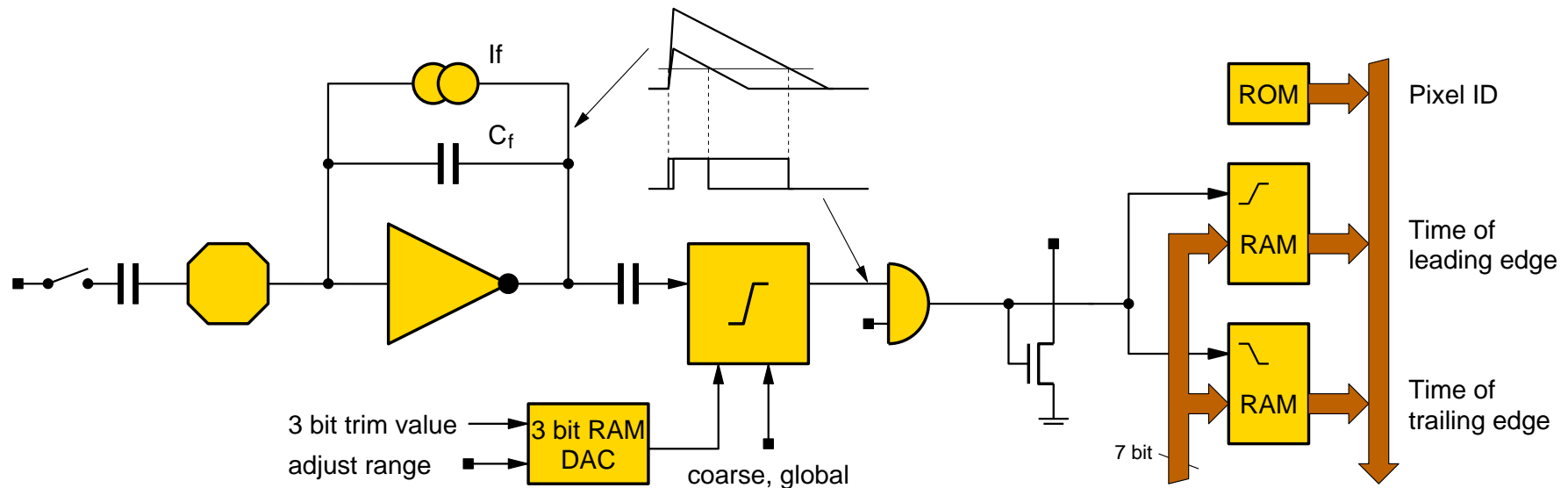


FE Chips: history

- Different chip developments in LBNL, CPPM / Bonn
- Final chips are a common design of the three teams with
 - analog part of FE-A/C
 - time stamp readout of FE-B
- Analog part has been prototyped in 'MAREBO' chip in DMILL
- **Successful test beams** have been done with **full modules** with **FEB** and **FEC** chips
- Latest chip is (radhard) DMILL chip '**FED**' it is presently being evaluated
- Honeywell chip '**FEH**' is in preparation
- we work with two rad hard vendors



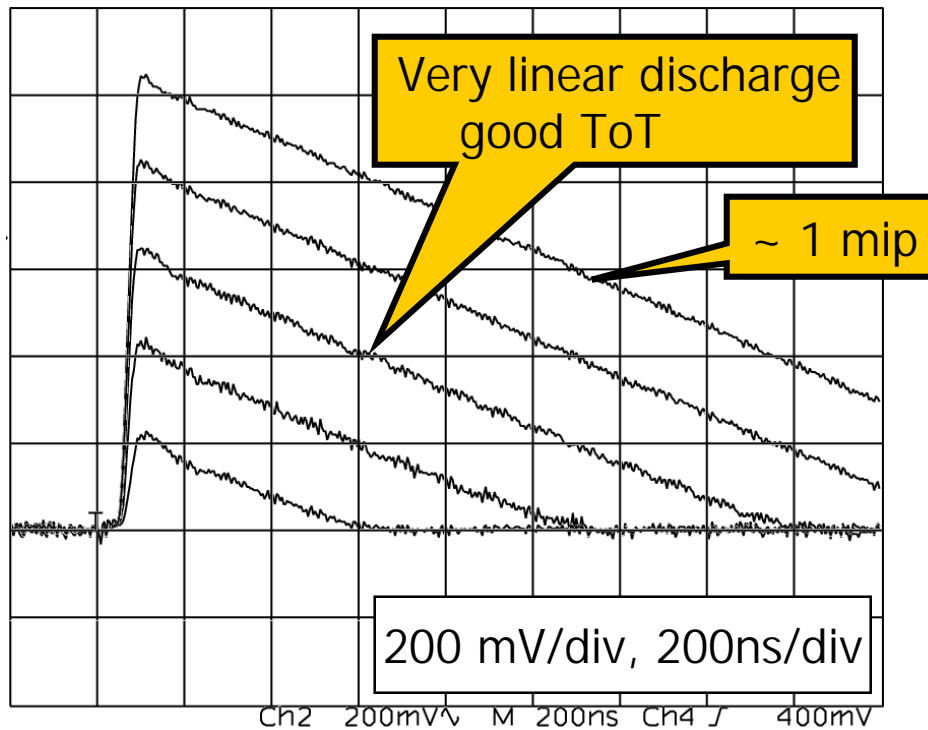
Analog part



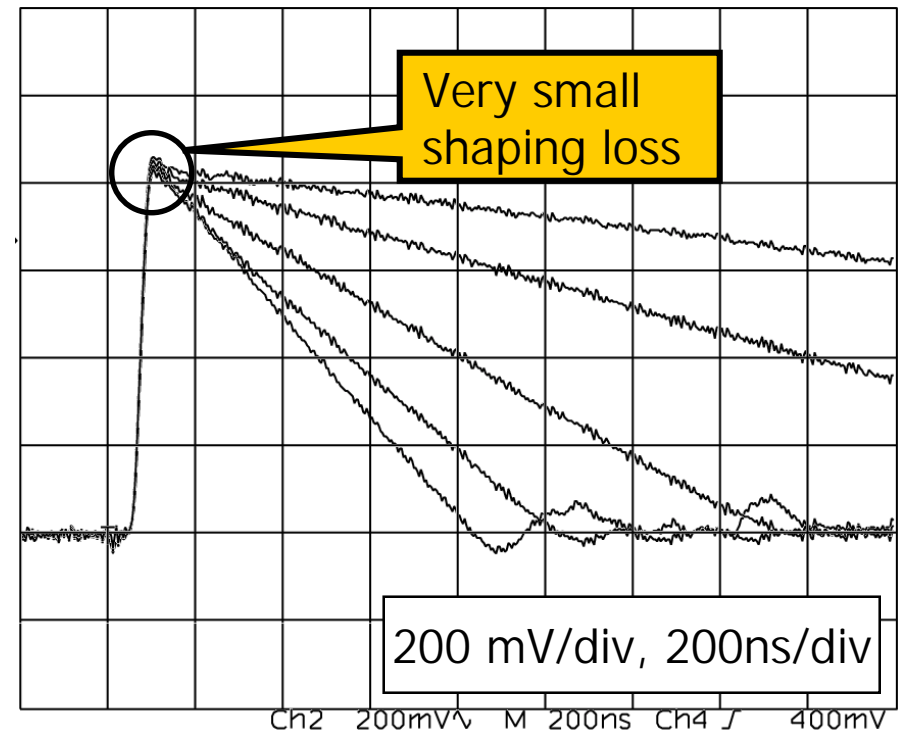
Inject Bump Pad Preamplifier Trim Discriminator Mask Hit-OR Time Stamp Hit Data

- Fast charge sensitive preamplifier with dc current feedback
- Discriminator with individual threshold adjust (3 bit DAC with adjustable range)
- Measurement of the pulseheight by Time-over-Threshold (ToT)
- Mask and test injection in every pixel
- Discriminator hit signal is sent to fast OR (hitbus')
- Power consumption is $\sim 40 \mu\text{W}$ per pixel, $V_{\text{DDA}} = 3 \text{ V}$, $V_{\text{CCA}} = 1.5 \text{ V}$

FED: preamplifier pulse shapes



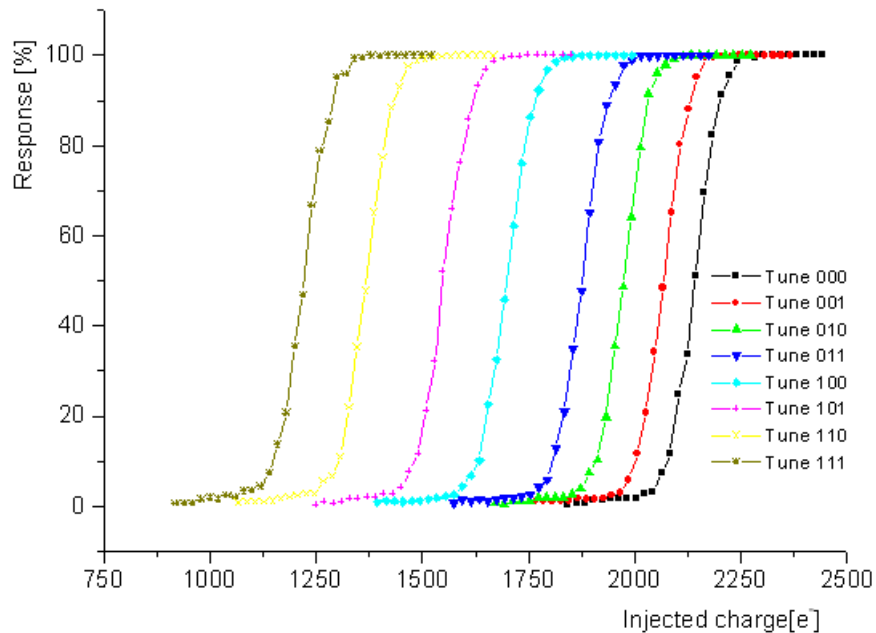
Different injected charges



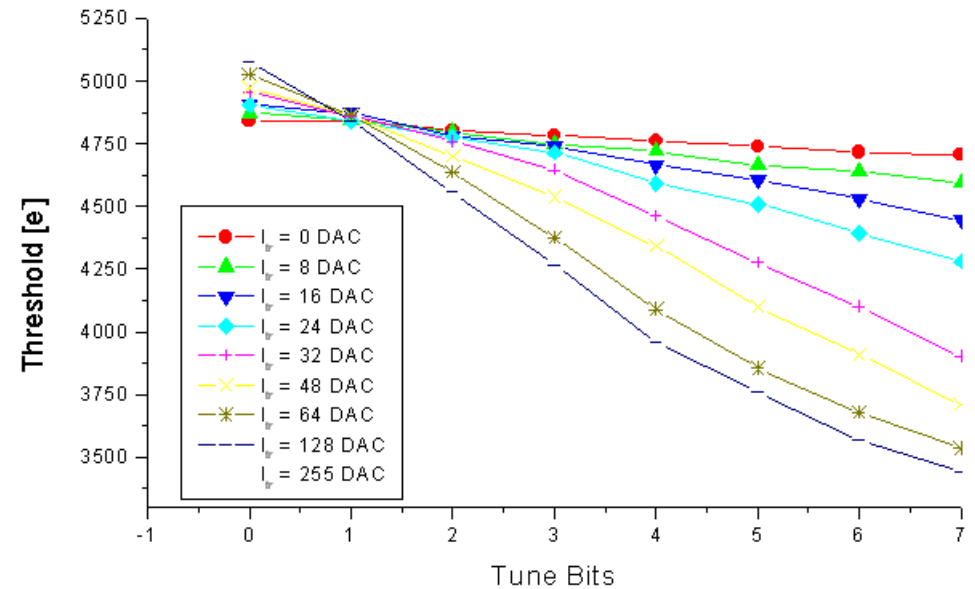
Different feedback currents

(Measured on testchip with internal chopper, no sensor)

Threshold adjustment (3 bit DAC)



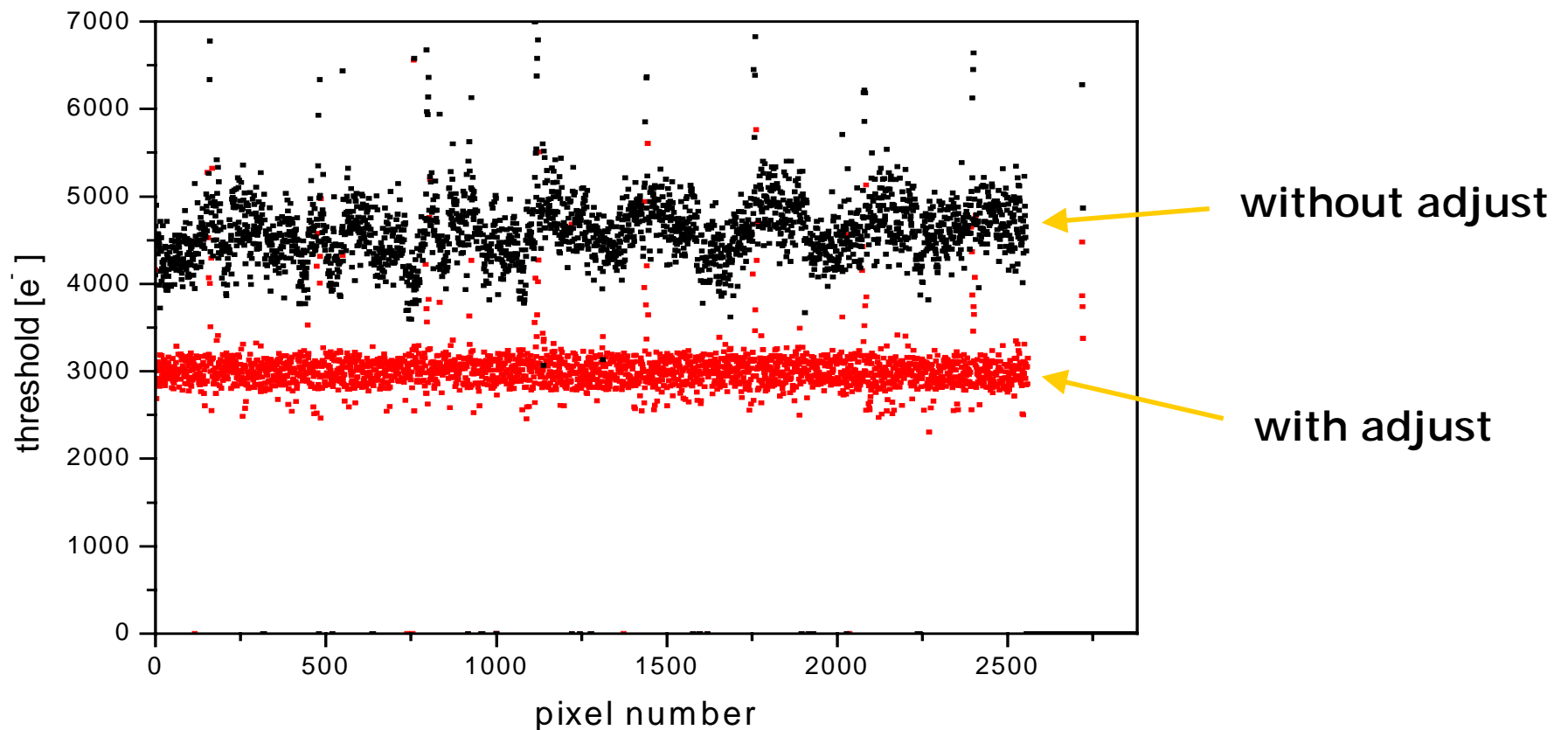
- threshold scans for the same global threshold setting, but 8 different DAC values



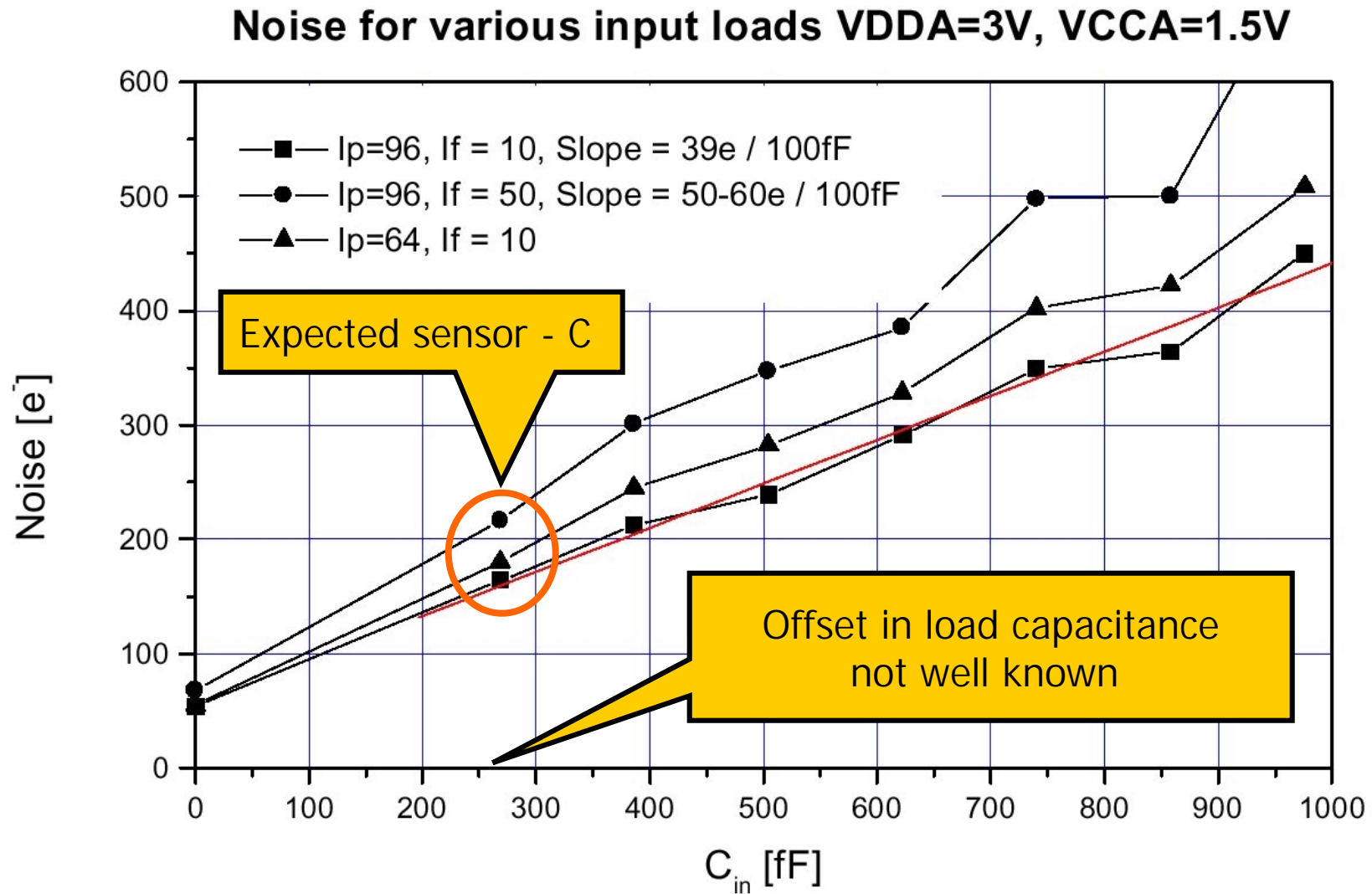
- Threshold change for 8 trims for various range settings
- 10 - 250 e^- / bit threshold trim

Adjusted thresholds

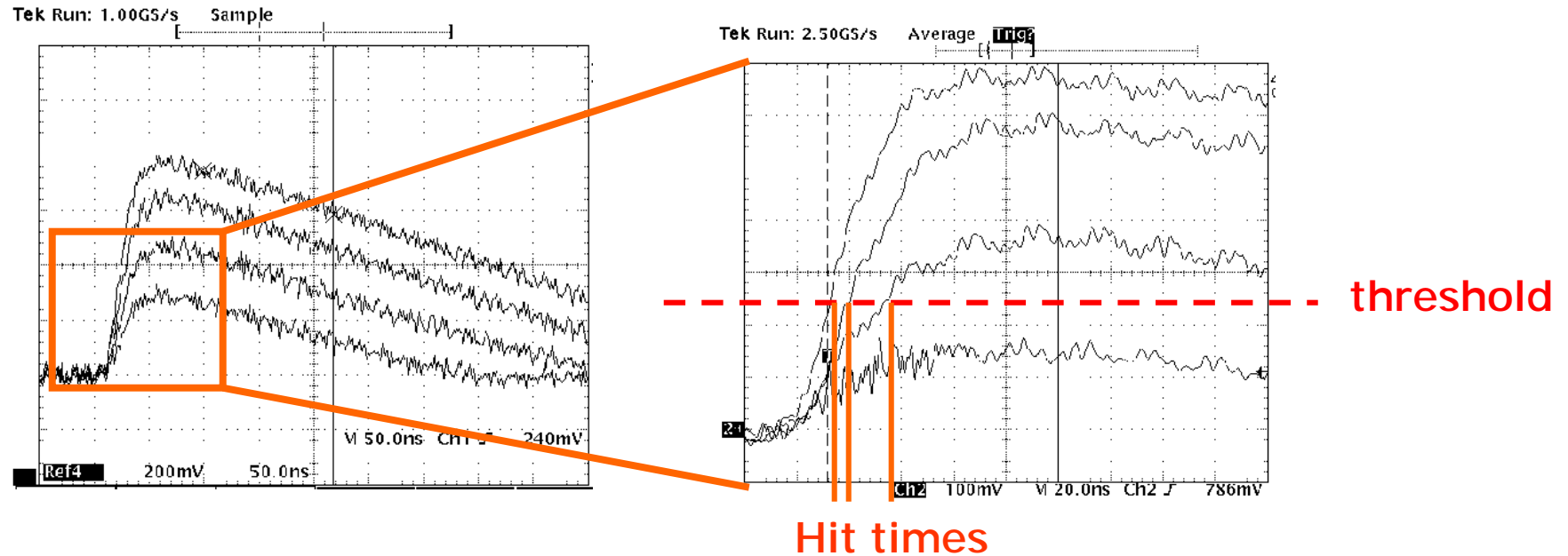
- Reduction of threshold dispersion (chip with sensor)
from $\sigma_{\text{thr}} = 323 \text{ e}^-$ to $\sigma_{\text{thr}} = 144 \text{ e}^-$



FED: Noise

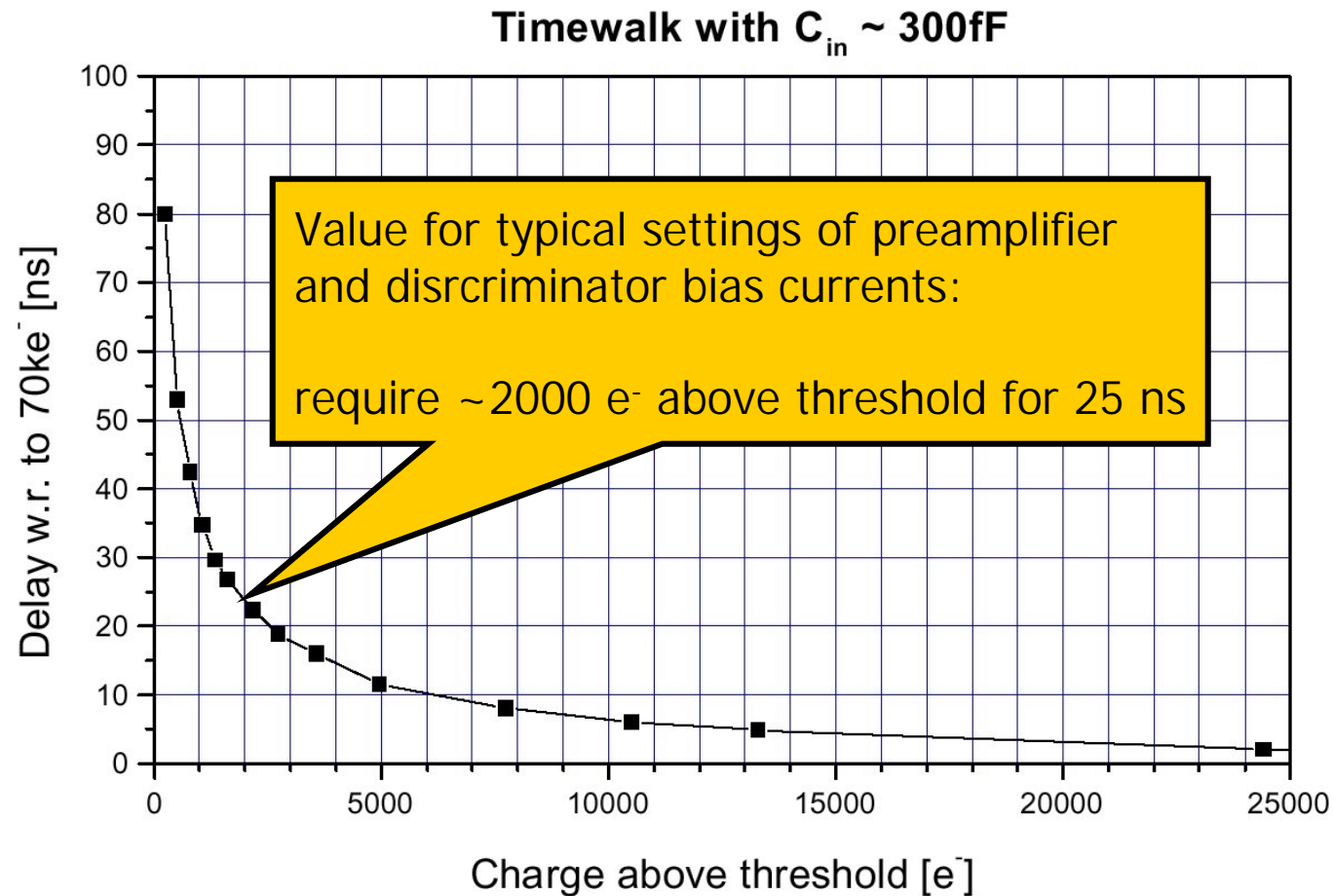


Time walk



- For correct hit association the time resolution has to be < 25 ns
- Problem: higher charge \rightarrow faster discriminator response
- Measure response time with respect to a 'high' reference charge (e.g. 50 ke)
- Timewalk is the **limiting factor for low thresholds** !
- Might be recovered if 2 crossings are read out

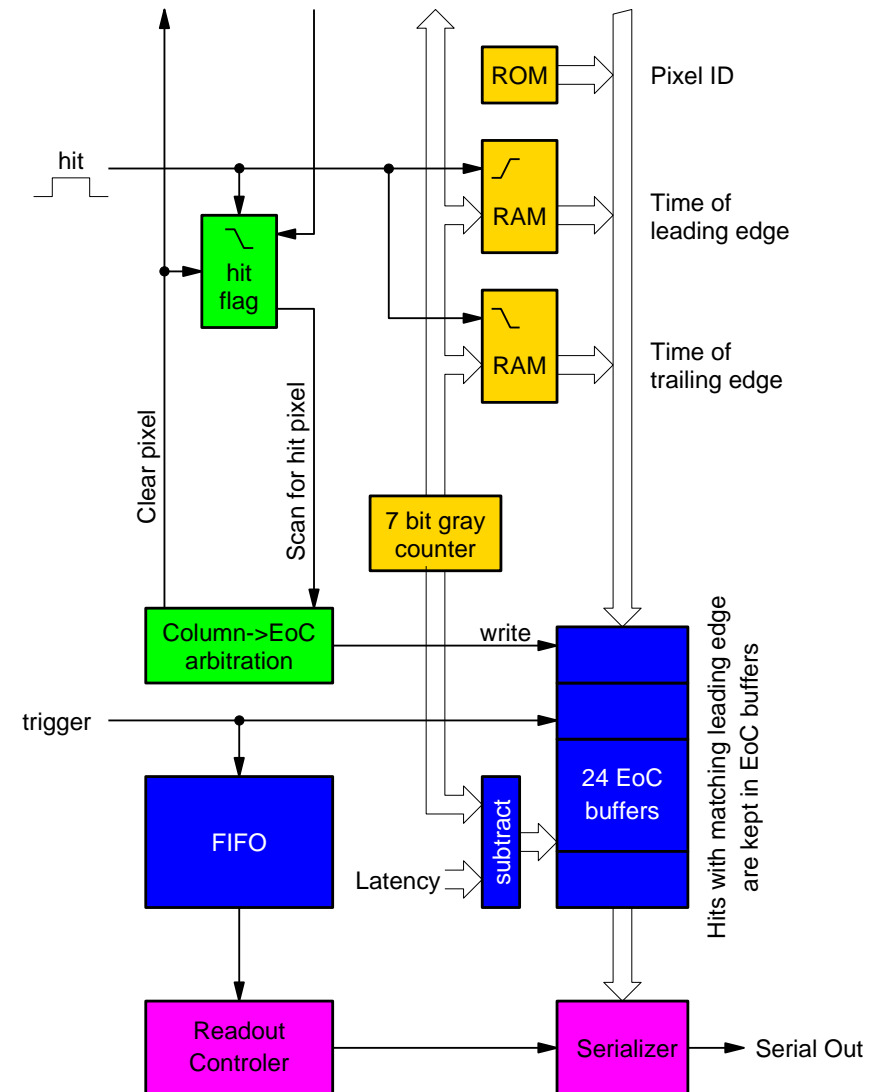
FED: Timewalk



(Measured on FED analog testchip, internal chopper)

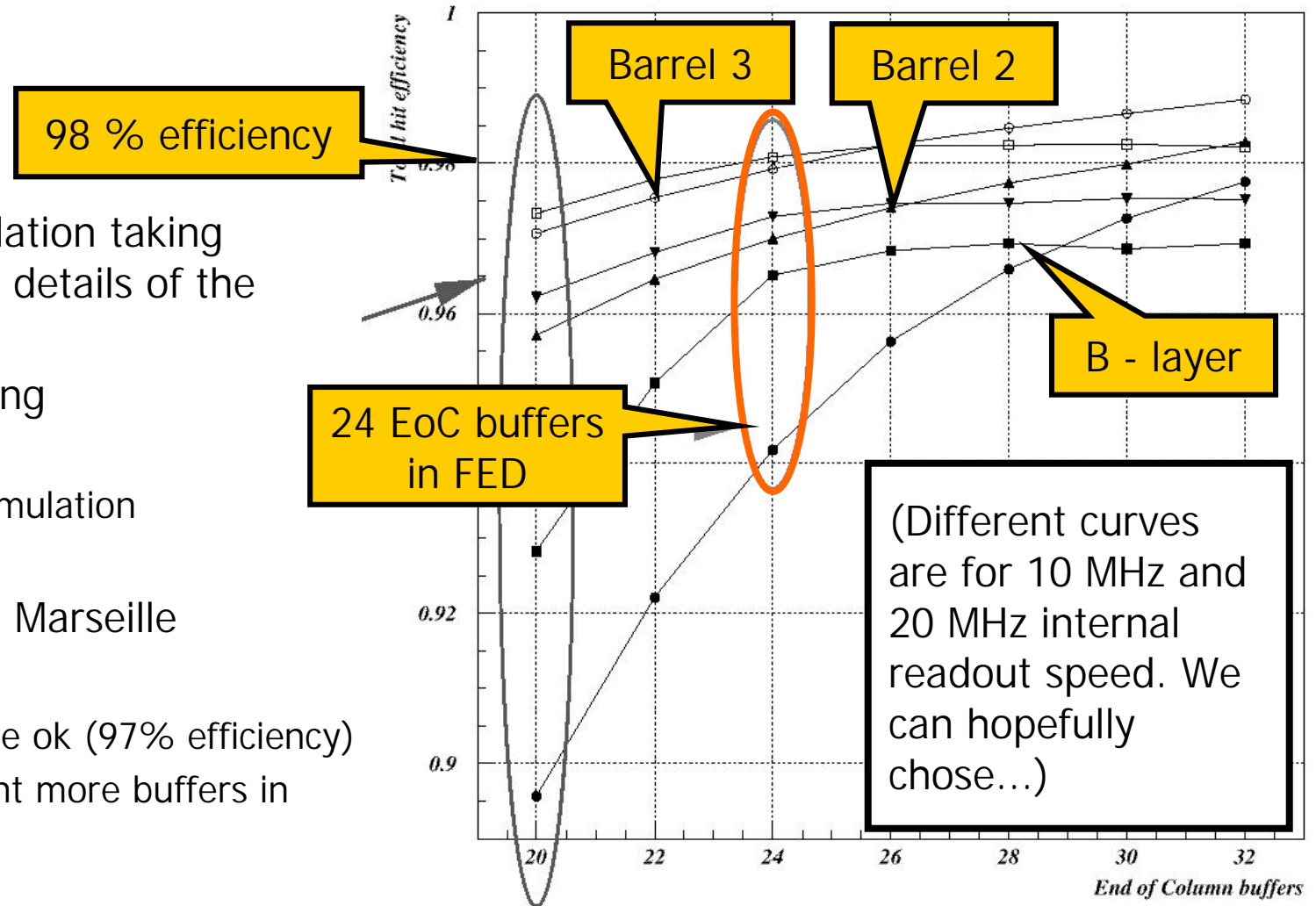
Time stamp readout

- A 7 bit **time stamp** is distributed to all pixels in the column
- After a hit the time stamps for leading and falling edge of the discriminator are **stored**
- The **hit is signaled** to the end of column logic with a fast ripple scan
- Hit pixels are **read out** and the hit **data is stored** in EoC buffers.
- The hit pixel is **cleared**
- After the trigger latency, the data is cleared from the EoC buffers or **sent to the MCC** when a trigger occurred
- 24 EoC buffers are used on FED

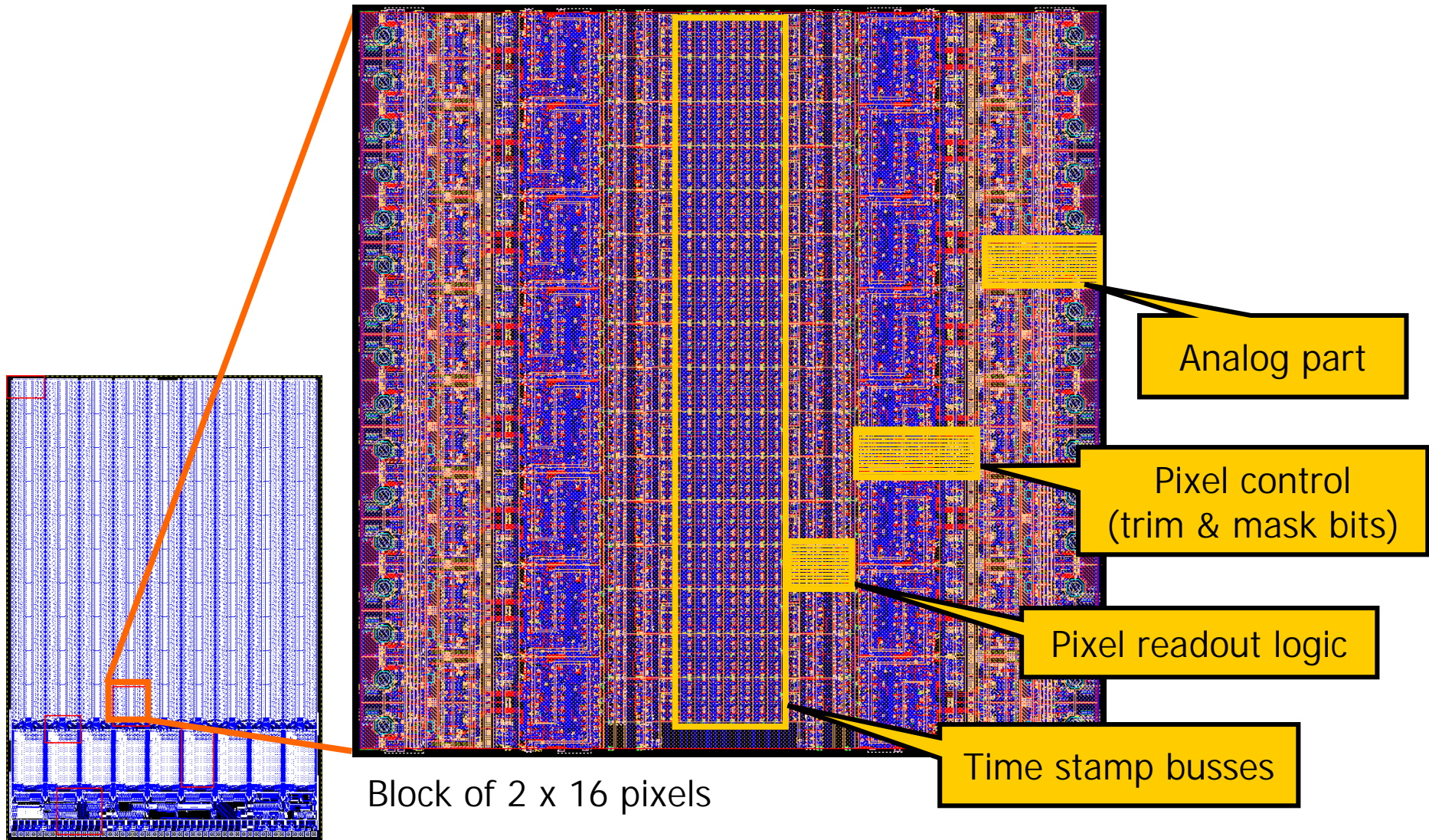


Simulation of hit losses in FED architecture

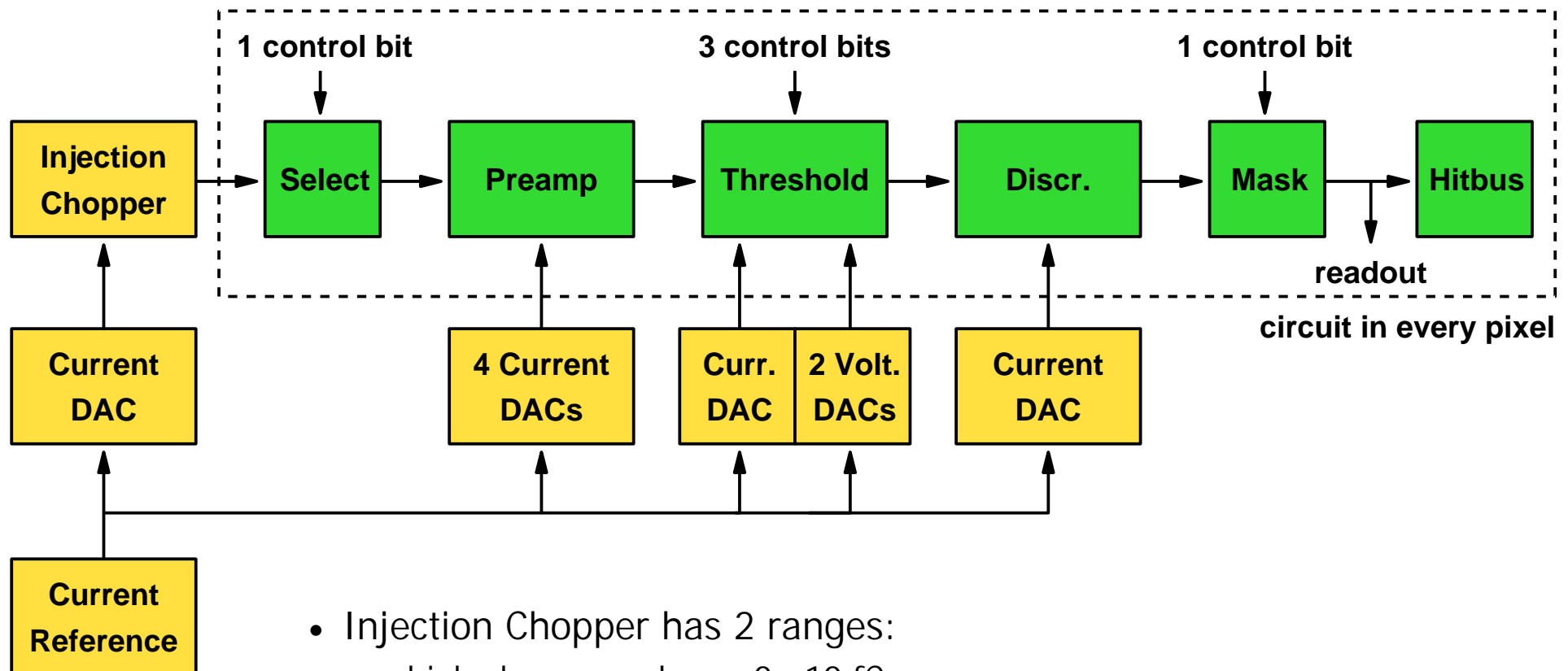
- Very realistic simulation taking into account many details of the architecture
- Full Luminosity using
 - Geant tracks
 - realistic sensor simulation
 - Lorentz Angle...
- Simulation done in Marseille
- Result:
 - 24 EoC buffers are ok (97% efficiency)
 - hope to implement more buffers in Honeywell design



FED readout: layout



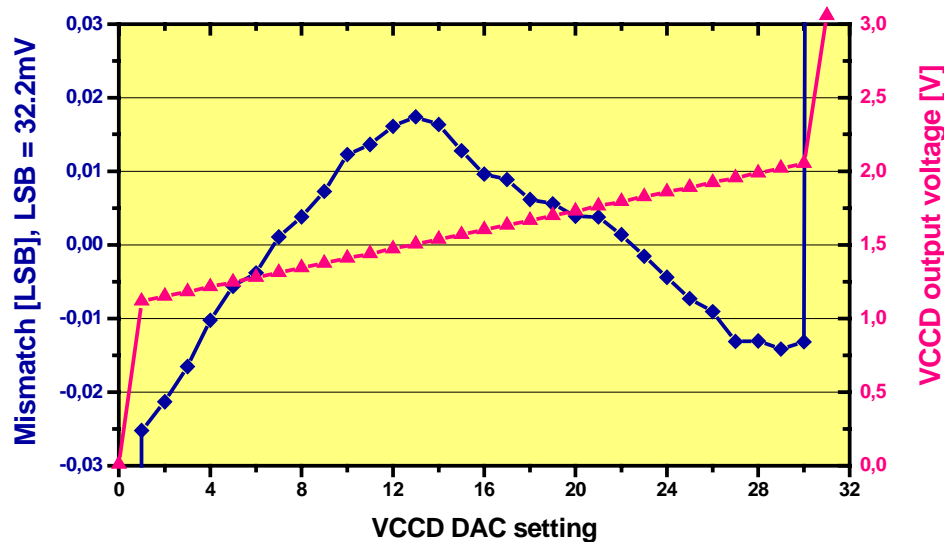
Additional analog control blocks on the FE chip



- Injection Chopper has 2 ranges:
 - high charge mode: $\sim 0 \dots 10 \text{ fC}$
 - low charge mode: $\sim 0 \dots 1 \text{ fC}$

Example of analog control blocks: DACs

VCCD output and nonlinearity

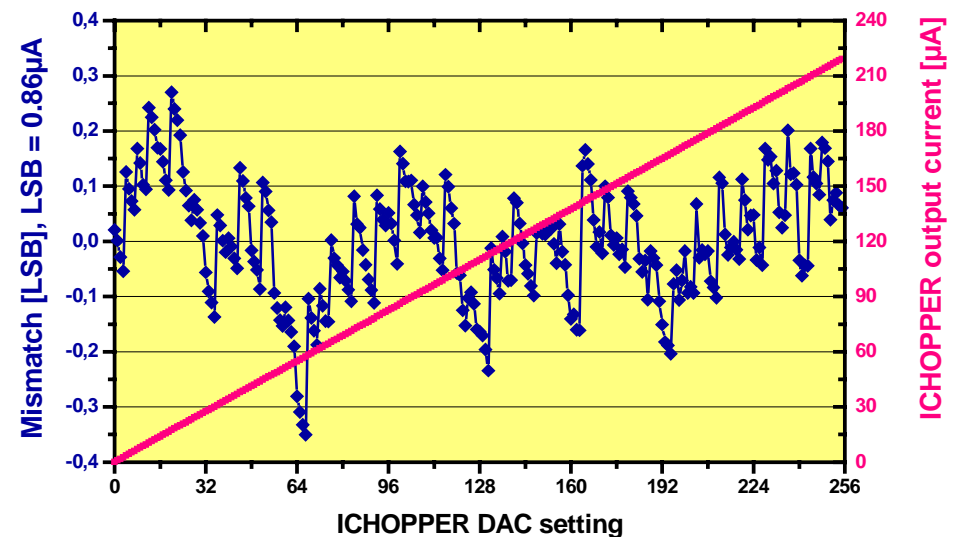


Two 5 bit voltage DACs:

- global threshold setting
- Shaping of AC coupling
- ‚rad hard‘ design

• **Nonlinearity < 0.03 LSB**

ICHOPPER output and nonlinearity



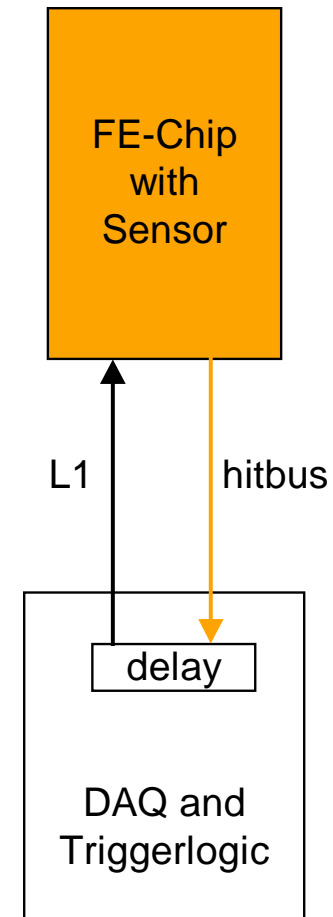
Seven 8 bit current DACs:

- Bias current setting
- Generation of voltage step through internal chopper
- ‚rad hard‘ design

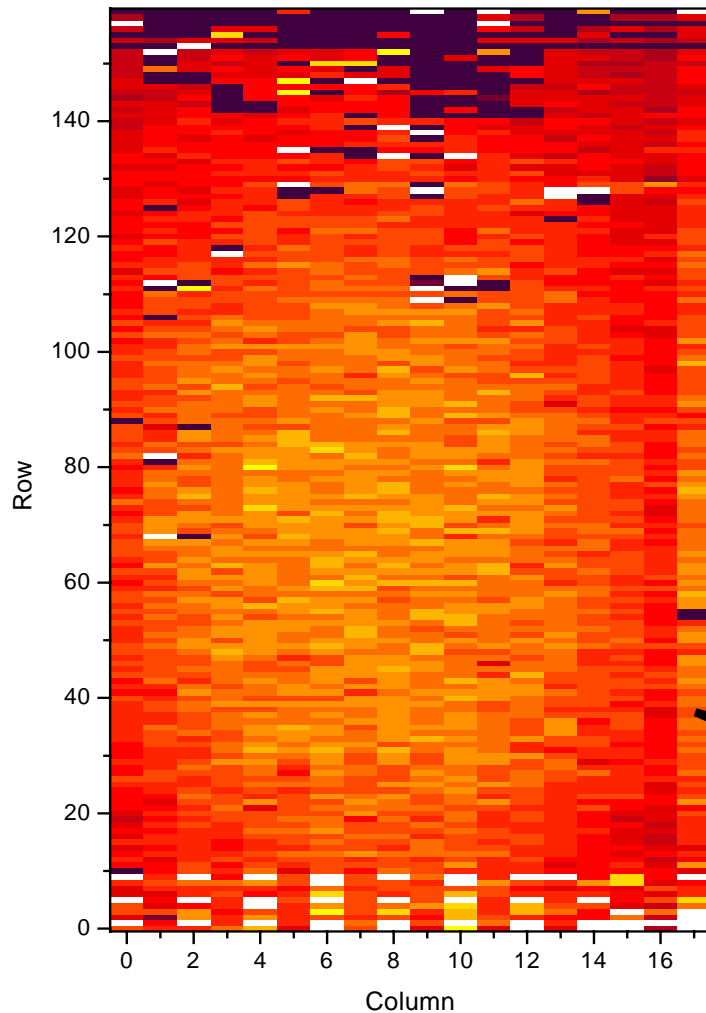
• **Nonlinearity < 0.4 LSB**

Source measurements: self triggering

- Problem in source measurements:
FE chip needs external trigger in true ATLAS mode
- One possibility:
Use scintillator → additional detector, not suitable for γ -sources
- Better solution:
 - use hitbus signal of the chip which signalizes a hit somewhere in the pixel matrix
 - Use this signal with correct delay as a trigger
- This is a ,fair' measurement using the readout in full ATLAS mode



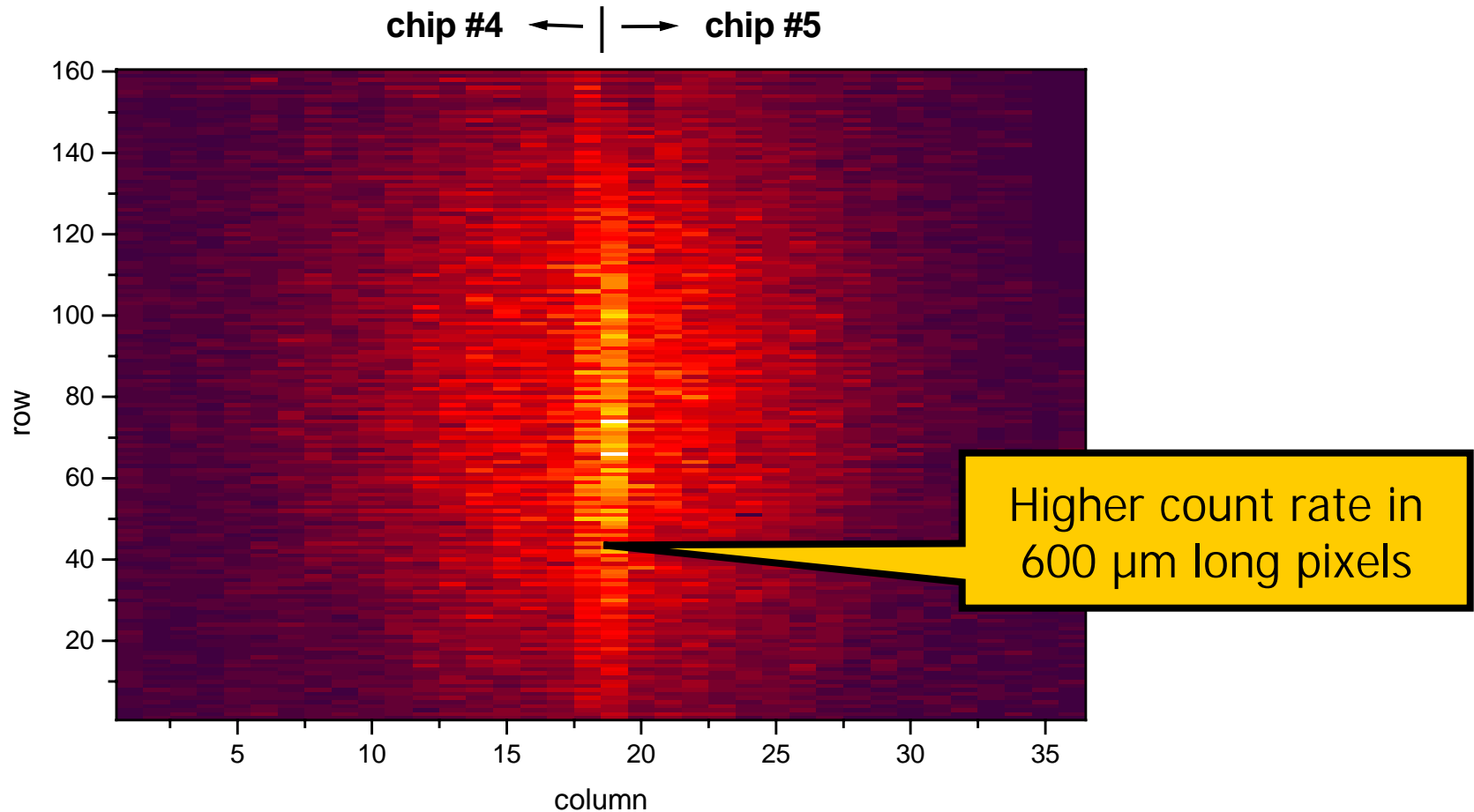
Source measurement with ^{55}Fe



- ^{55}Fe -source (6keV γ) deposits only **1700** eh-pairs
- FE-C chip with thresholds tuned to $\sim 1200e^-$
- Some bump problems at edge
- The chip can be operated at a **very low threshold**

600 μm long sensor pixels
-> higher rate

Source measurement on a module with ^{241}Am



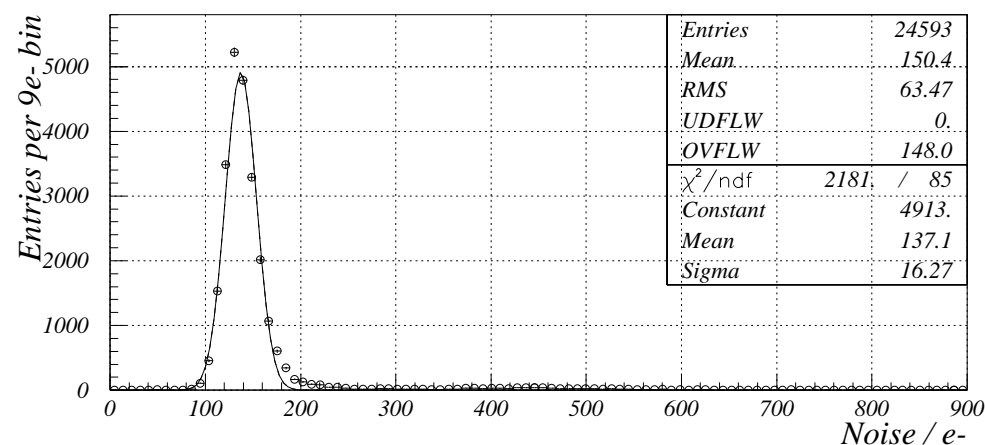
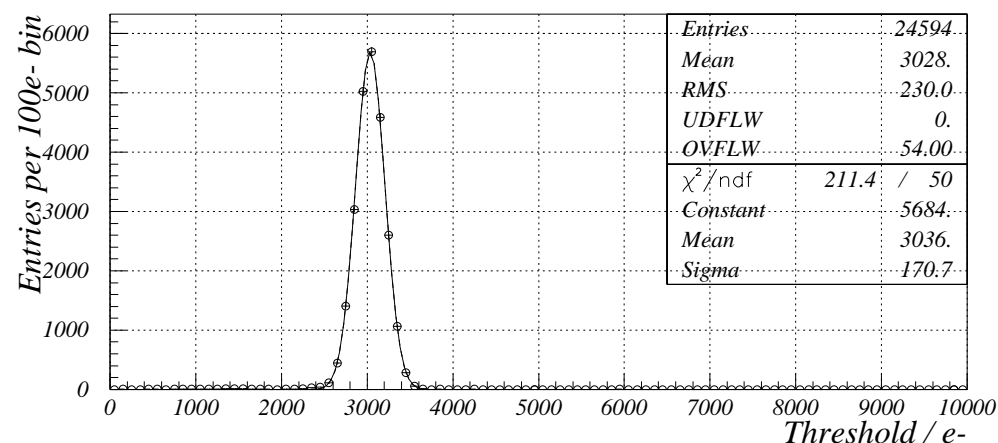
- Spot of ^{241}Am -source on **two neighbouring** chips of a module
- Module without MCC: chips were illuminated one after the other

Module performance (thresholds & noise)

- Module with 16 chips, here FEB
- Noise and ToT response are comparable to single chips.
- Performance of several modules:

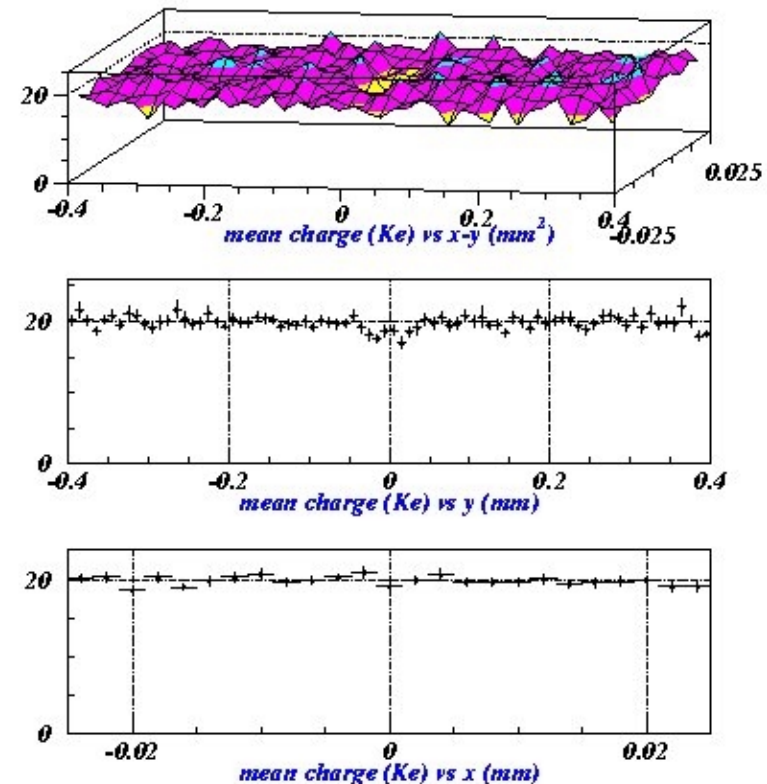
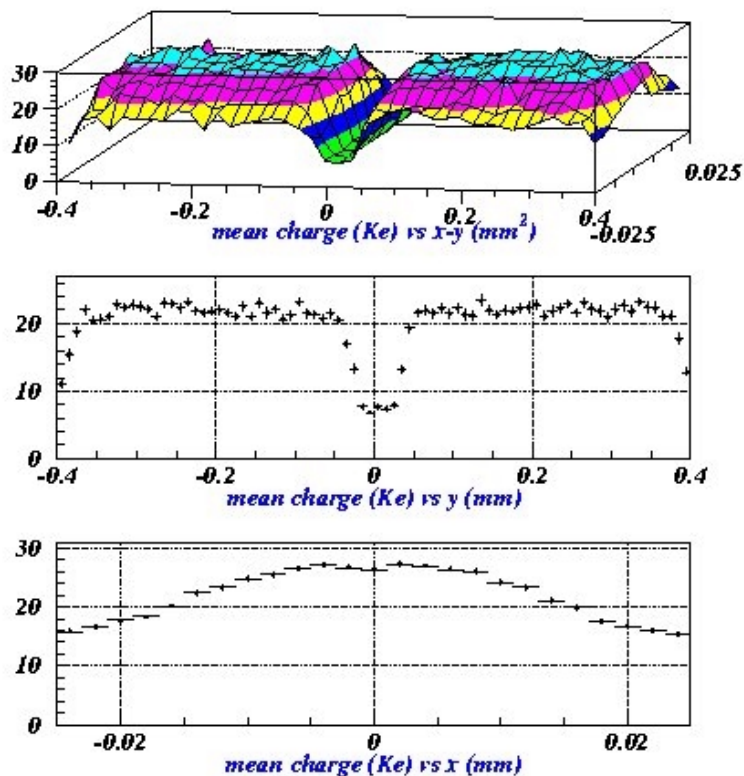
Module type	Front-end	Bump	Threshold [e]	Noise [e]
Bare	FEB	IZM	2000	140
Flex	FEB	IZM	2000	180
Bare	FEC	IZM	2500	140
Flex	FEB	IZM	3000	160
Flex	FEB	Alenia	3600	180

File : *tlizm_tune3k* Summary Plots



Testbeam: charge collection studies using ToT

- ToT gives information about collected charge
- ToT analysis in testbeam was able to show differences in charge collection between different sensor designs, e.g. two different p-spray sensors:



Summary and Outlook

- Non-rad hard ATLAS chips (FEs, MCC) are **close to meet our goals**.
- Radiation hard designs of **all chips** have been produced by DMILL
- Problems here are:
 - Very low yield in first FED run.
 'Strange' behaviour of chips not seen before with same architecture.
 - **Identical second ,backup' run has much higher yield.**
 - We need to understand what is going on.
- New **FED2 design is finished**.
 - Some small bugs are fixed, buffering of many digital signals improved.
- Full DMILL **MCC-D2 will be ready soon**
- **FEH will be submitted** late summer 2000 to Honeywell.