

Study of Indium bumps for the ATLAS pixel detector

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G.Gagliardi, [C.Gemme](#), P.Netchaeva, L.Rossi, E.Ruscino, F.Vernocchi
University and INFN of Genova, Italy

[A.M.Fiorello](#), [M.Varasi](#)
Alenia Marconi Systems - Rome, Italy

[M.Gilchriese](#)
LNBL, USA

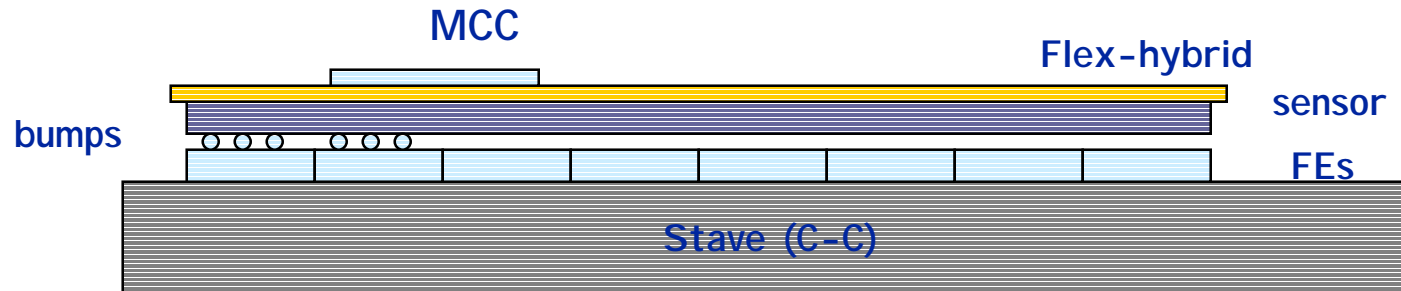
On behalf of the ATLAS Pixel Collaboration

Outline

- Introduction
- AleniaMarconiSystem (AMS) bump-bonding technique
- Results:
 - Mechanical properties
 - Electrical Resistance
 - Yield of Electrical defects
- Conclusions

Modules layout

Bumps are at the same time the electrical and mechanical connection between sensor and electronics in a module



Requirements:

pitch: 50 μm

density: 5000 contacts/cm²

bumps/module: ~50000

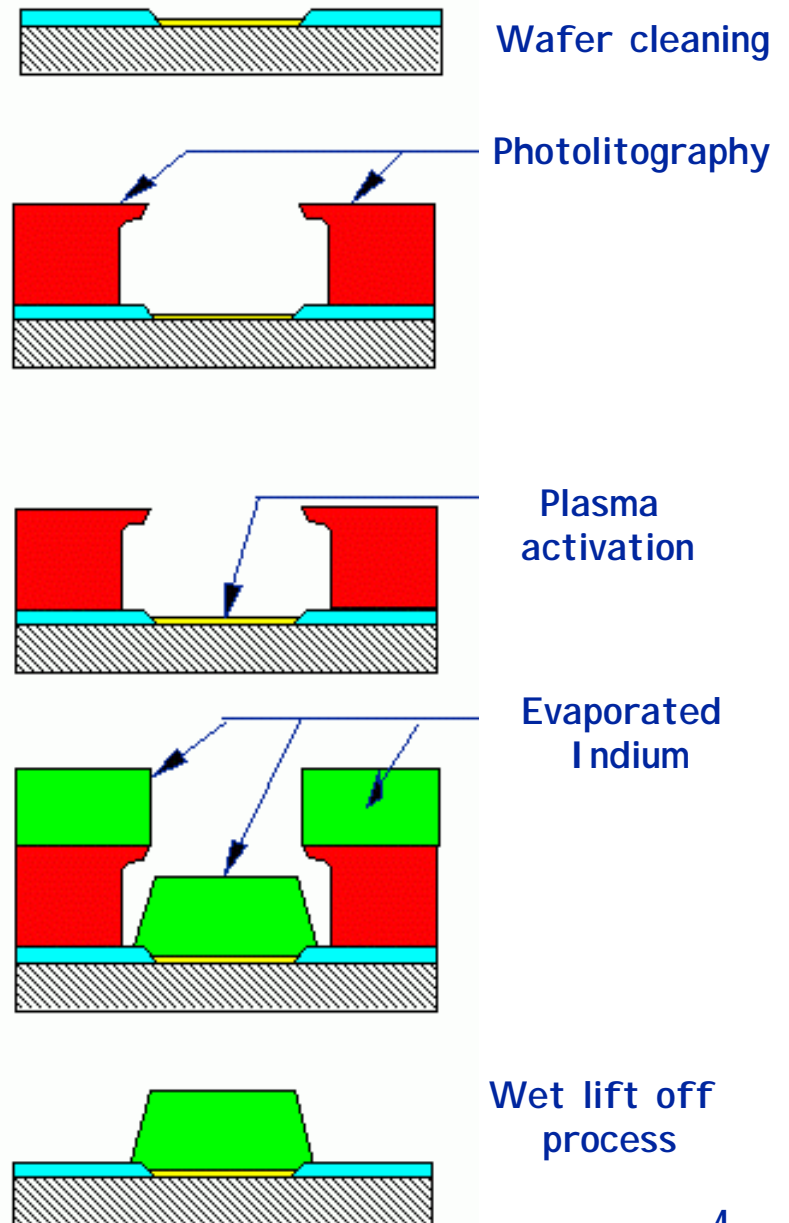
bumps/ATLAS: ~10⁸

The bump-bonding technology is used to join the front-end readout ICs to the silicon sensor substrate:

- * bump deposition
- * flip-chip assembly

AMS bump deposition

- More details during this evening round table
- Indium Bumps are deposited both on electronics and on silicon sensor wafers through metal evaporation
- Bump thickness:
 $6.8 \pm 0.2 \mu\text{m}$
- Thickness uniformity:
 $\pm 0.3 \mu\text{m}$ (6" wafer)
- Fault rate (by optical inspection):
 $(2.0 \pm 0.6) \cdot 10^{-5}$

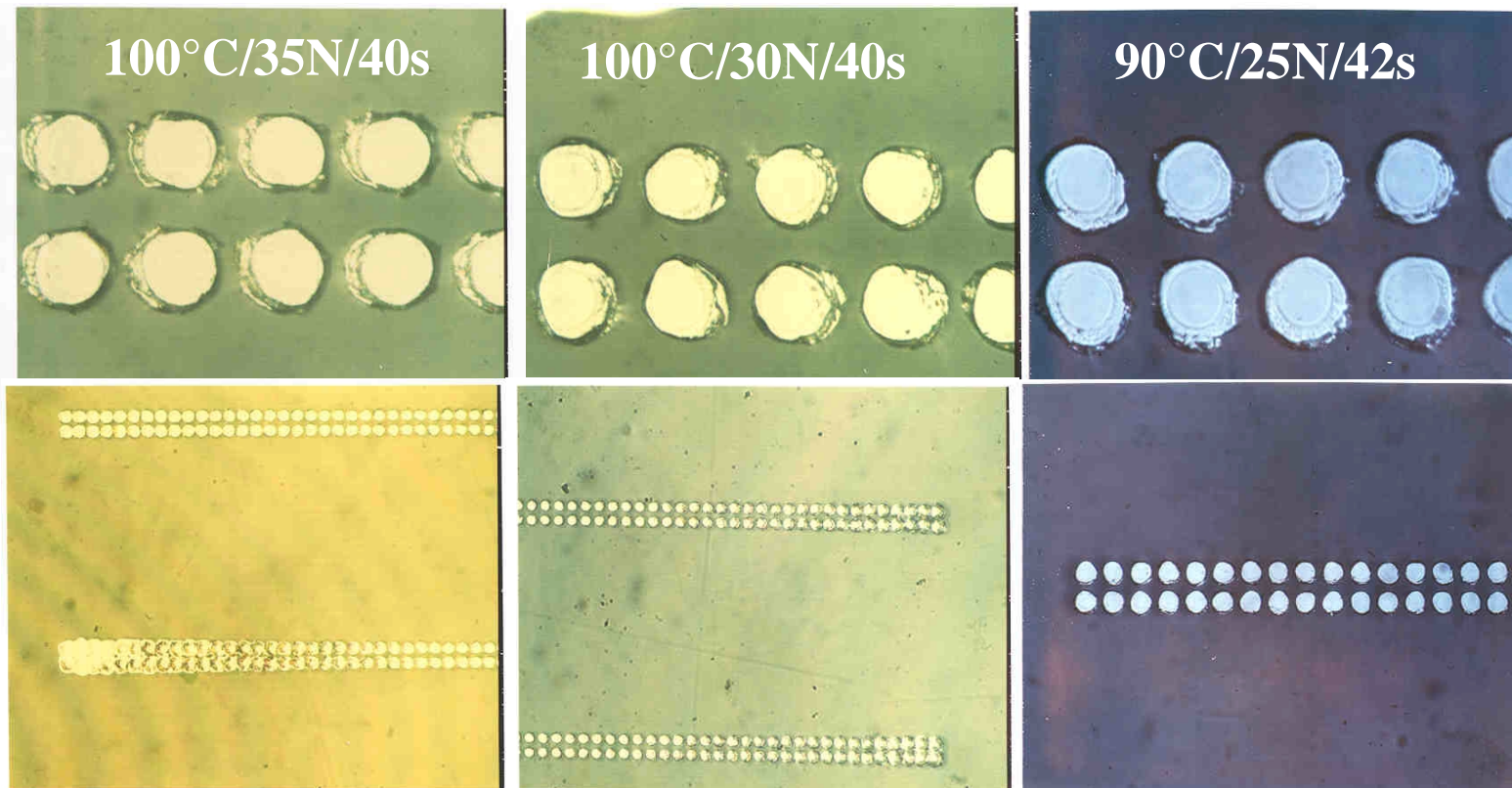


Flip-chipping Assembly

- Flip-chip is the process of mounting the integrated circuit die onto the silicon sensor substrate.
- Bumps previously deposited on both the silicon sensor and the IC die are accurately aligned and then joined under pressure (FC6 Karl Suss Bonder).
- Pressure, temperature and time are critical parameters to determine a good result of the flip-chip.

AMS Flip-chip

- The choice of flip-chip parameters is performed with glass substrates to better investigate effects on bumps

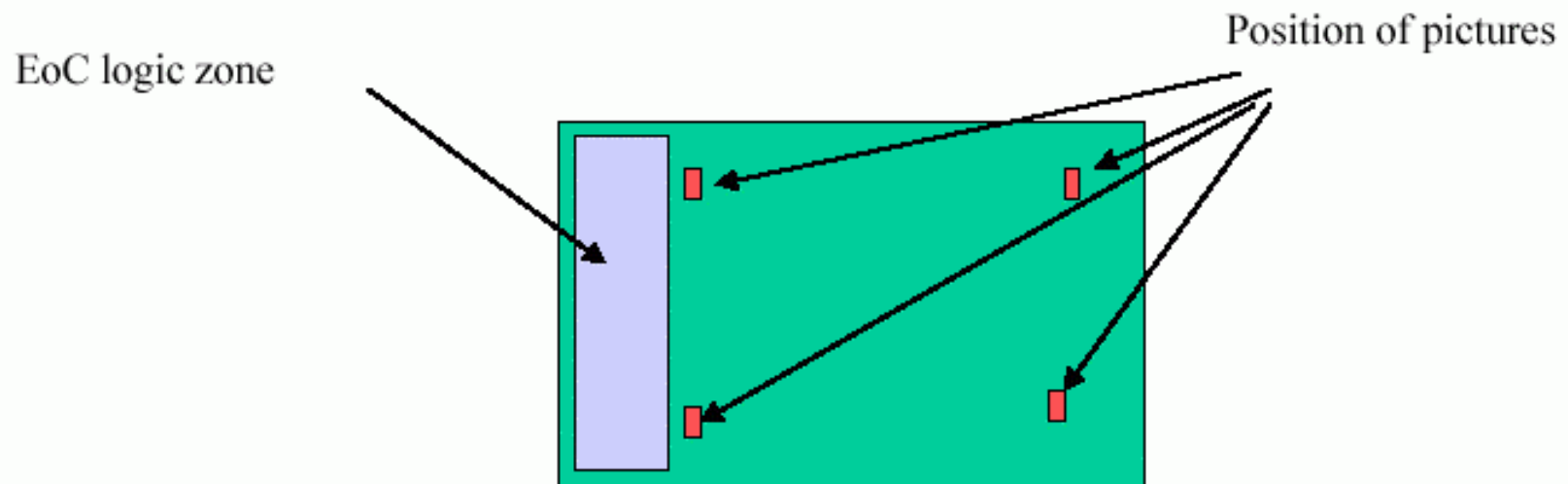


AMS Flip-chip

- Selected parameters:
 - Force: 25 N (per FE chip)
 - Substrate Temperature: 90 °C
 - Chip Temperature: 90 °C
 - Time: 42 sec
- Bumps height : ~8 μm (7 μm + 7 μm bumps pressed together)
- Bump diameter: ~20 μm
- Tensile strength: ~0.1 g/bumps *i.e.* ~3 N/FE
- Check Flip-chip planarity

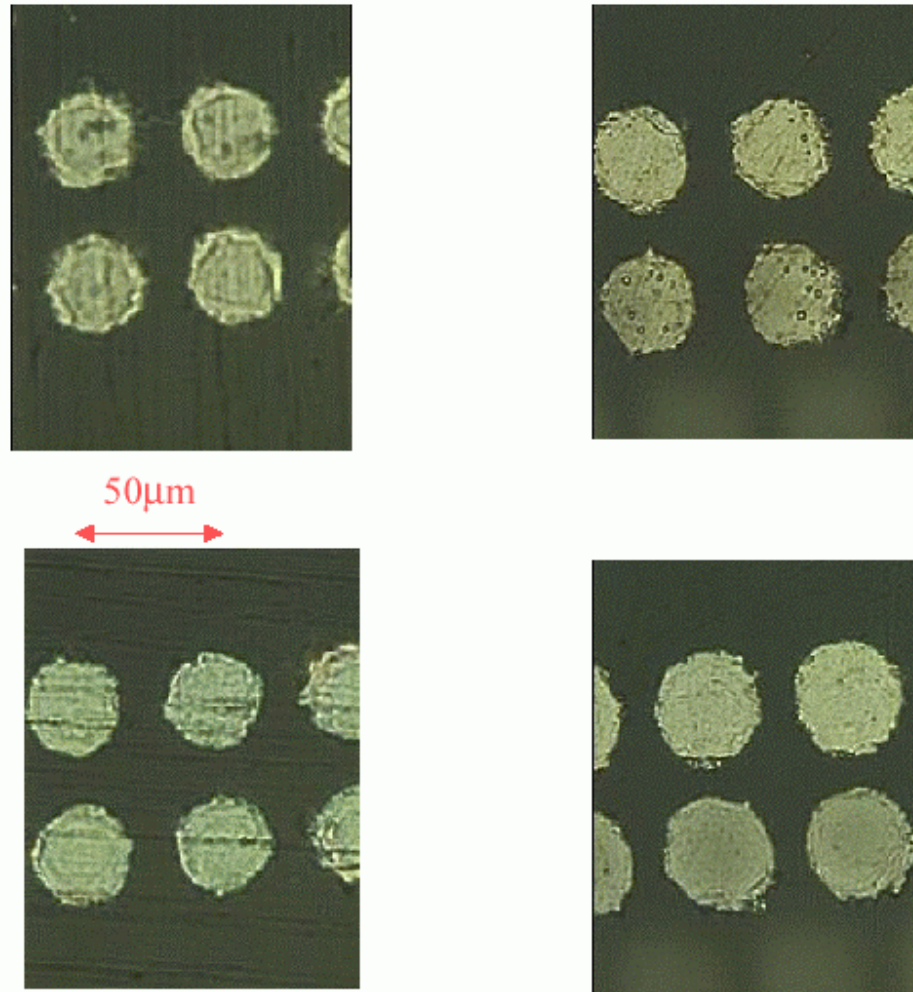
Test of flip-chip planarity

- To check the planarity in the flip-chip process, the flip-chip machine is tuned using bonded glass substrates and checks are done at the four corners of the chip



Test of flip-chip planarity

$T = 90^{\circ} \text{C}$
 $F = 25 \text{ N}$
 $t = 42 \text{ s}$



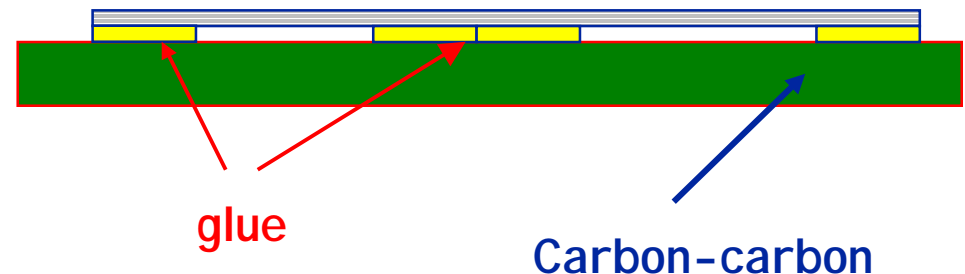
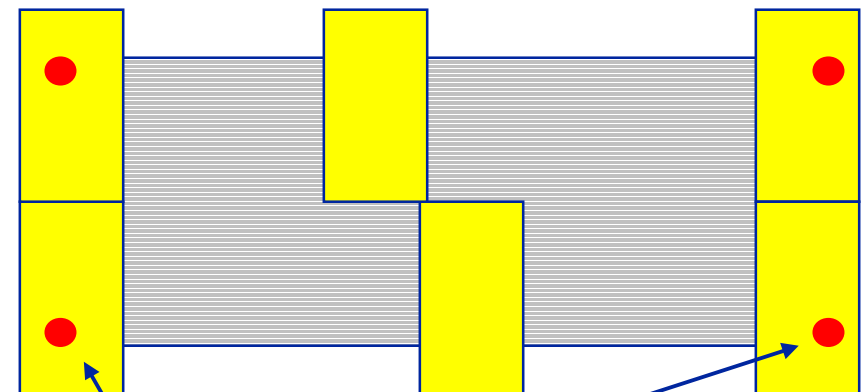
As uniformity of the bumps at the corner of the chip is verified, planarity obtained with the flip-chip machine is good

Mechanical Stresses on bumps in *real* conditions...

Bumps will be mechanically stressed during thermal cycles due to different CTEs of the materials they bond (detector build at room T but operating at T below 0°C)

Dummy module to simulate stress:

- **Tile** = 300 μm thick glass with In bumps by AMS.
- **Chips** = 550 μm thick FE chips with In bumps by AMS.
- **Flip-chip** in Genoa INFN lab.
- **Glue** between electronics and stave = cyanoacrylate, rigid glue to enhance stresses

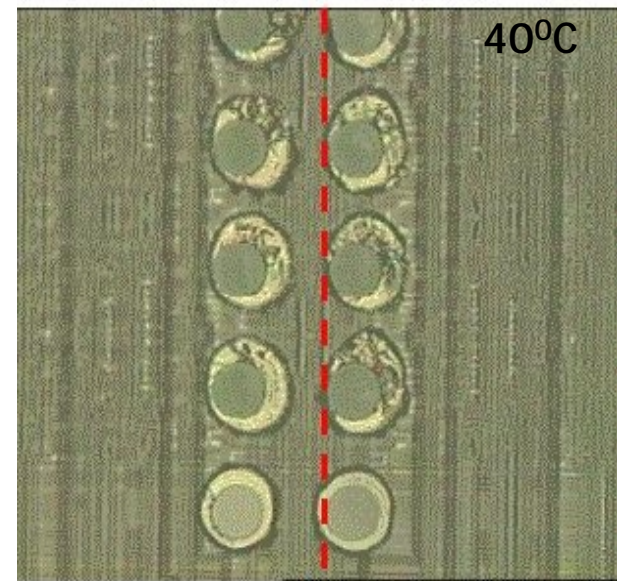
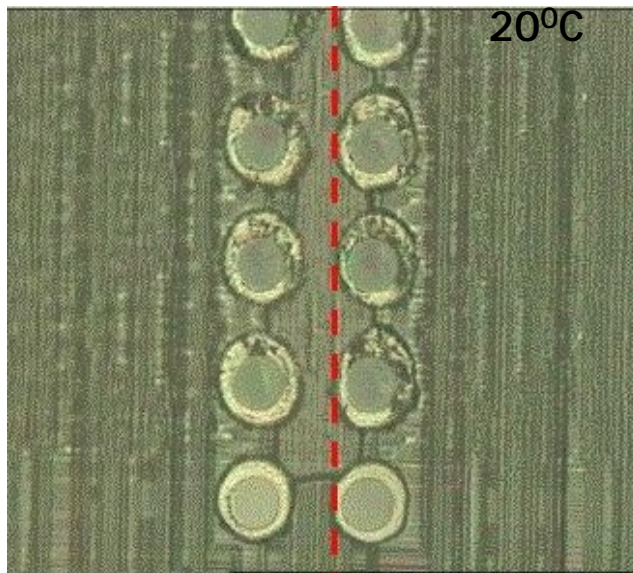
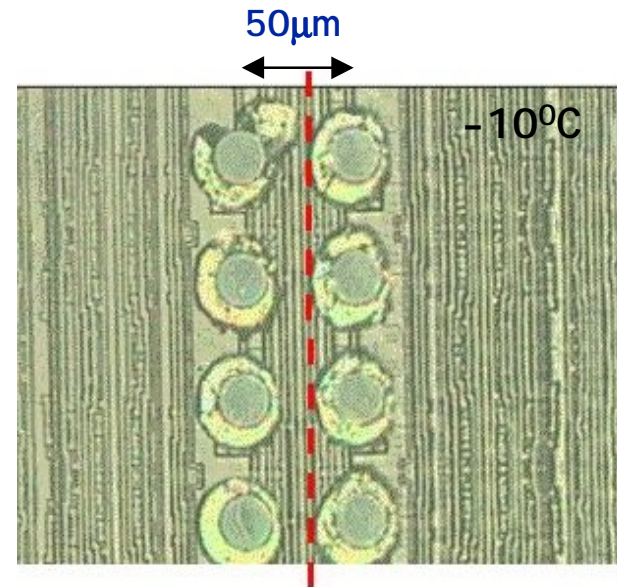


Mechanical properties

- Bumps displacement measured with microscope at edge of tile.
- Measurements at -10C , $+20\text{C}$ and $+40\text{C}$, T measured with IR thermometer.
- A dozen of cycles $[-20\text{C}$, $+20\text{C}]$, measured after each cycle in some cases rising to $+40\text{C}$ (90% of time at -20C , i.e. under stress).
- Periodically checked bump connectivity by measuring the bump gap with microscope focus: this was constant after each cycle and equal to $8 \pm 1 \mu\text{m}$ (typically $\sim 30 \mu\text{m}$ when bump is disconnected).

Left edge (low side)

- The red line represents a fixed position on the chip.
- Max displacement measured is $\sim 7.5 \mu\text{m}$ (for $\Delta T = 50^\circ\text{C}$)
- No problem with bump connectivity
- Due to different CTE between this glass and silicon, we expect for $\Delta T = 30^\circ\text{C}$ a displacement of $\sim 3 \mu\text{m}$

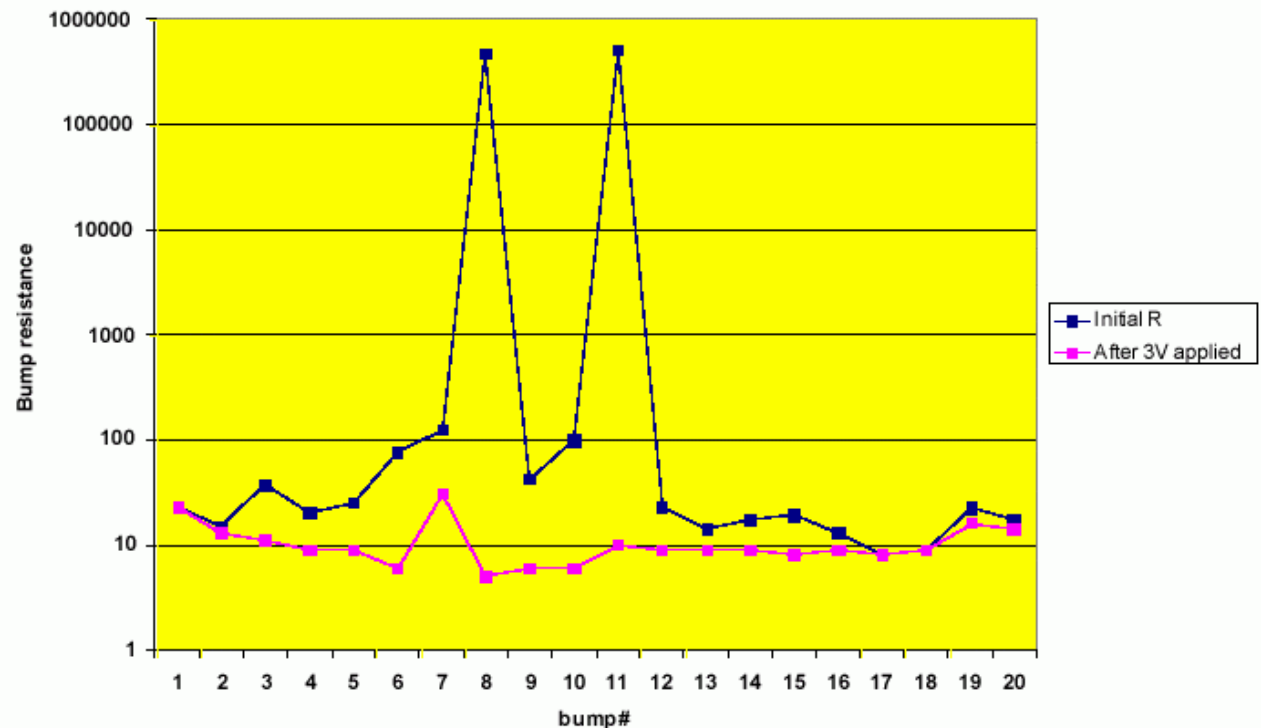


AMS bumping results: electrical measurements

- Bump connection resistance must be small not to significantly contribute to the front-end noise.
- It is well known that In develops an oxide layer once taken out of the vacuum tank where the bump deposition is done. In_2O_3 is an insulator.
- It is desirable that the oxide layer break automatically when the bias is applied to the electronics.

Constant voltage

- Resistance of the bumps with a digital ohm-meter for some bumps, before and after applying 3V
 - Only 10% of the bumps have initially an oxide layer
 - The oxide resistance is quite low ($\sim 500\text{K}\Omega$)
 - Once the oxide is broken the bump resistance is uniformly low ($\sim 10\Omega$) \Rightarrow $\sim 2\Omega$ after subtracting the probe needles resistance



Resistance measurements notes

- AMS In oxide is thin (low resistance $O(500K\Omega)$) and already broken in $\sim 90\%$ of the cases. Breaking the residual oxide requires low voltages ($O(50mV)$) for some minutes.
- The bump resistance after oxide breaking is low enough ($O(2\Omega)$) to allow proper operation of the FE electronics.
- The bump resistance after oxide breaking is stable in time and after thermal cycles.

How bumps work with real detector and real electronics:

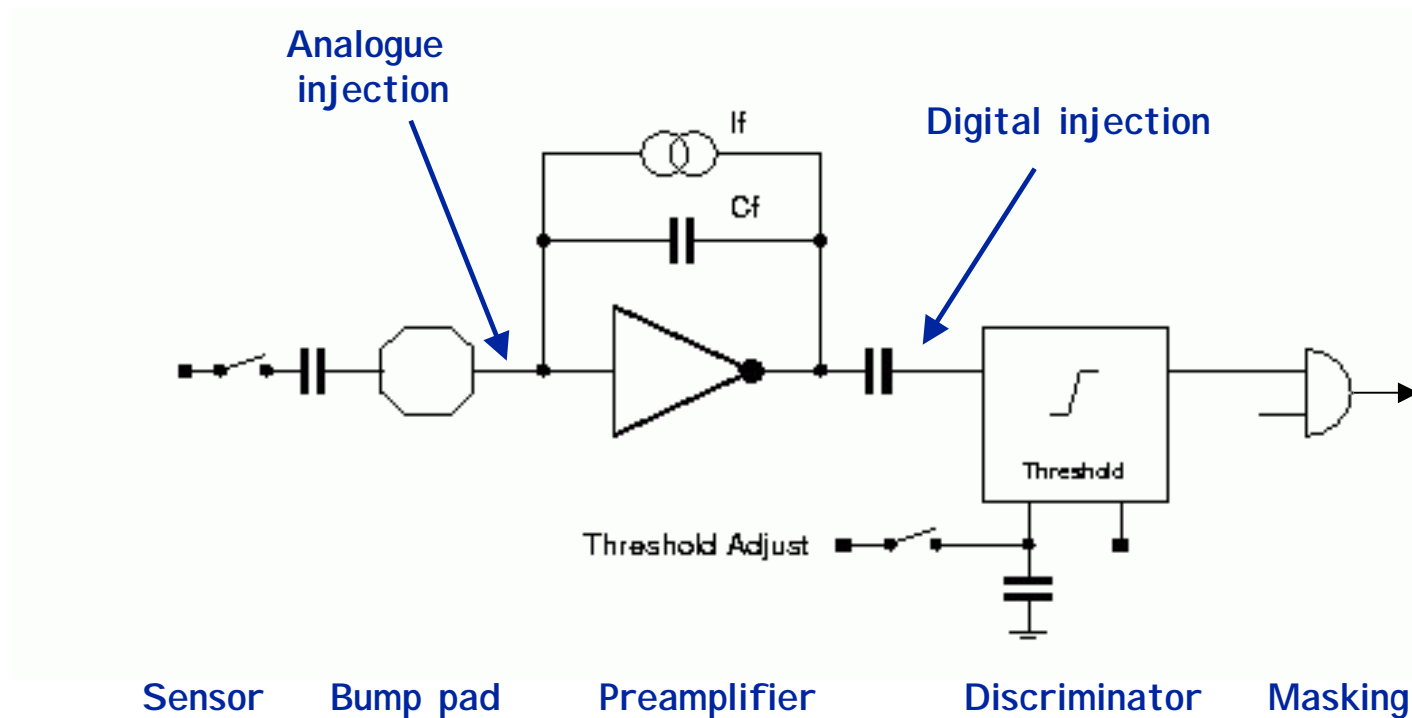
Modules and single chips with AMS bumps

- Different type of devices produced: single chips, modules, single chip and modules with thinned electronics.
- A total of about 100K channels investigated
- It is possible to investigate defects due to the bump bonding:
 - Merged pixels: neighbouring bumps are connected
 - Missing pixels: no contact between sensor and electronics
- X-ray analysis of some flip-chipped devices offers the opportunity to correlate the bump defects and the electrical behaviours of the pixels.

Pixel test

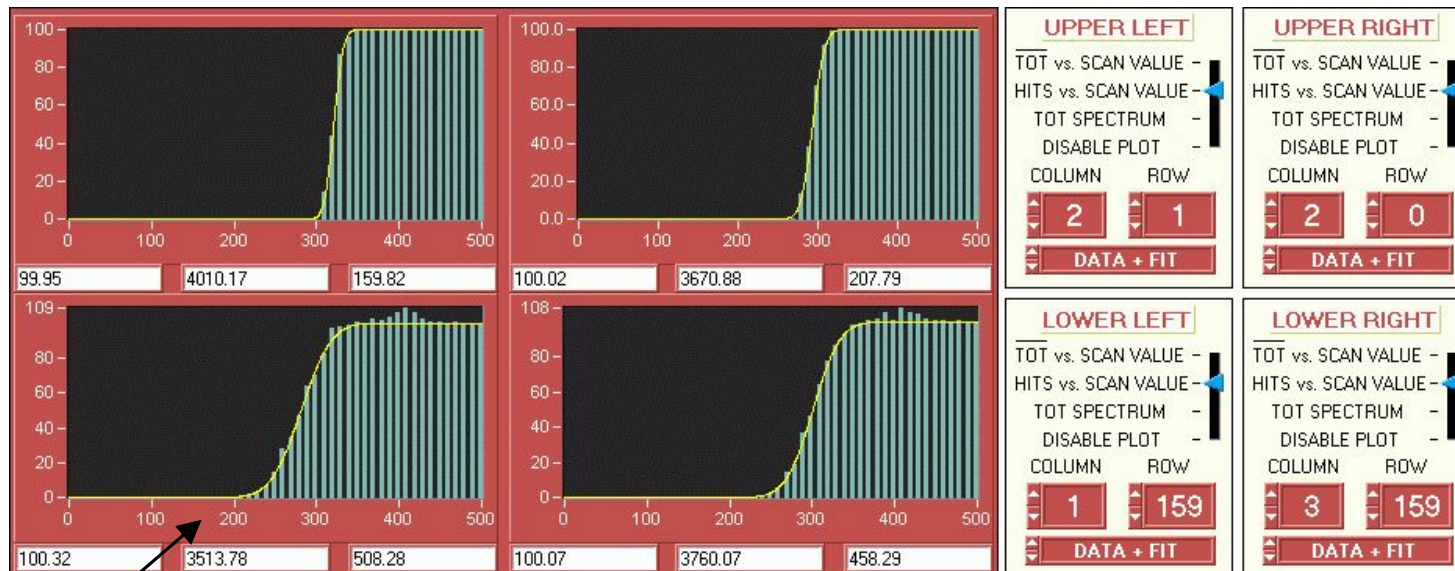
- In our lab we can test each pixel by a **digital injection**, an **analogue scan** and with a radioactive **source**.

Block diagram for one pixel



Test procedure

- **Digital injection** to test the digital part of the pixel electronics and the overall FE electronics.
- **Analogue scan** to measure threshold and noise for each pixel.



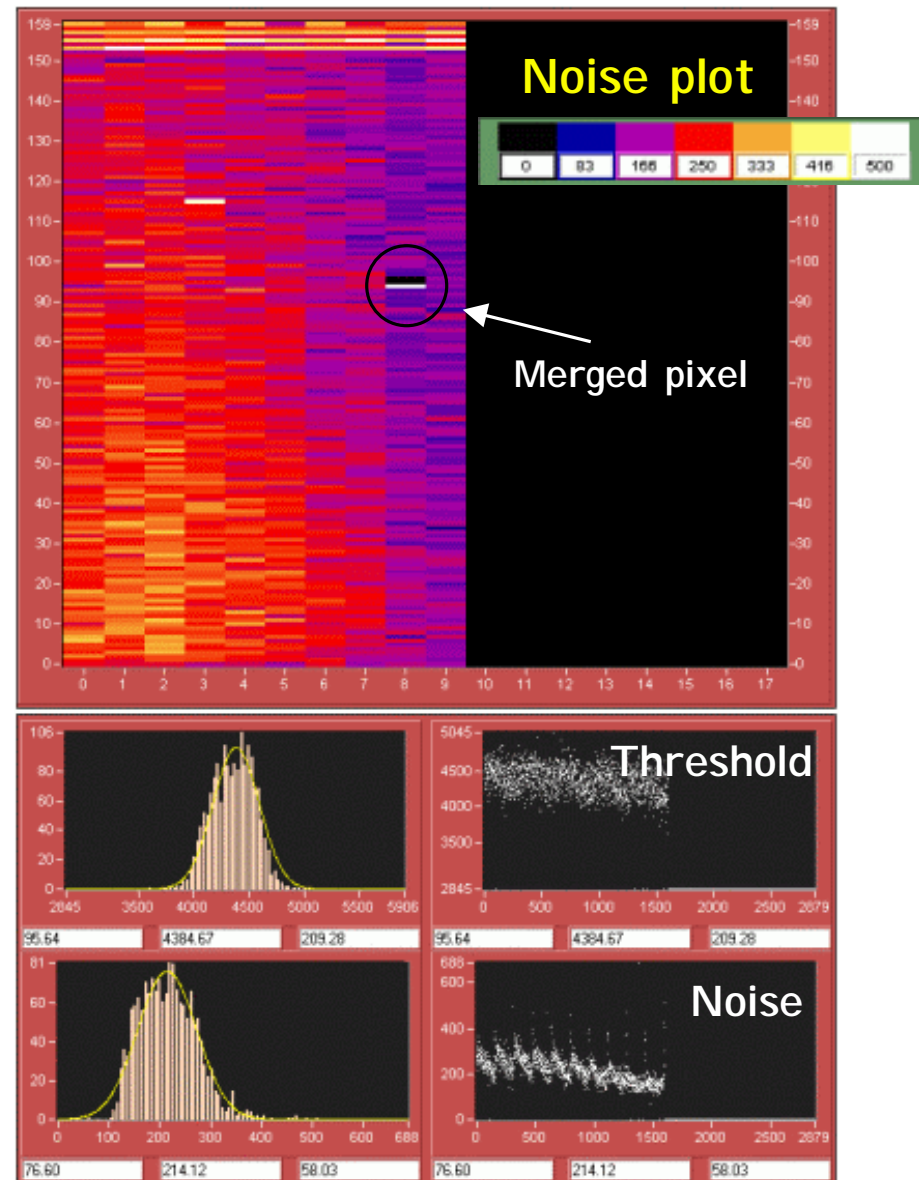
Scan voltage(mV)

Threshold(e⁻)

noise(e⁻)

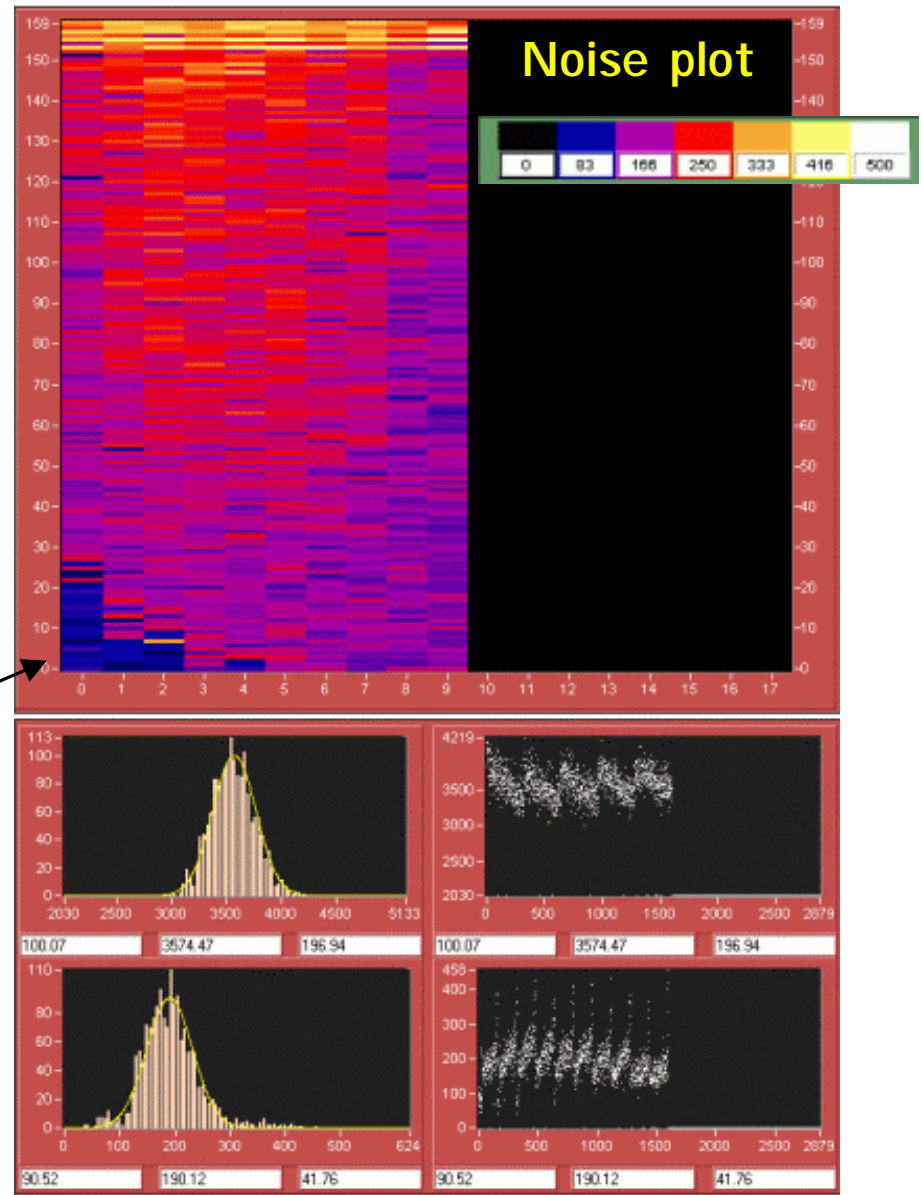
Test procedure: looking for merged bumps

- From the analogue scan we identify:
 - Good electronics channels
 - Bad pixels (never responding to the injection):
 - High threshold
 - Non-working preamplifier
 - Merged bumps:** charge goes in a neighbouring pixel which results noisier as it sees more sensitive area
 - With an automatic program suspected merged pixels can be identified



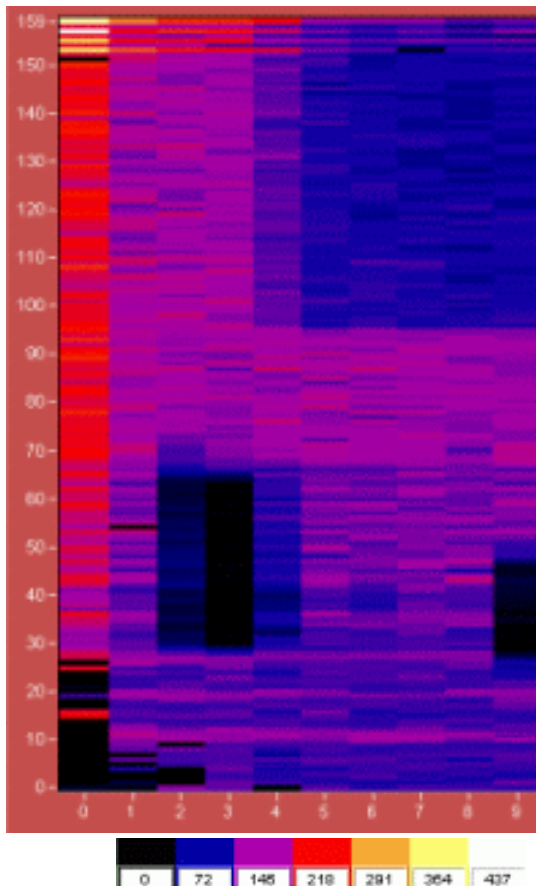
Test procedure: looking for missing bumps

- From the analogue scan:
 - Suspected missing pixels:
 - Good electronics channels with low noise ($<100e^-$)
 - Missing contacts could be due to:
 - missing bumps in the deposition process
 - detachment during handling (figure)

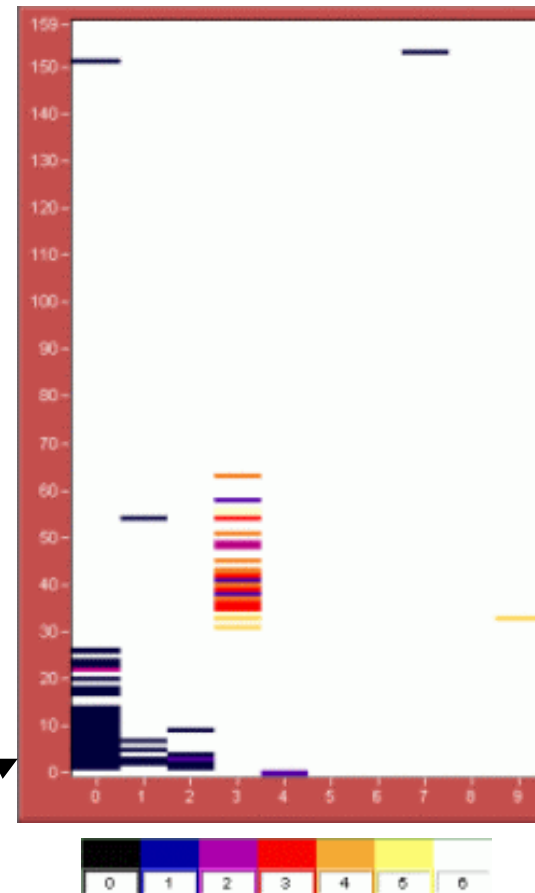


Test procedure: looking for missing bumps (cont'd)

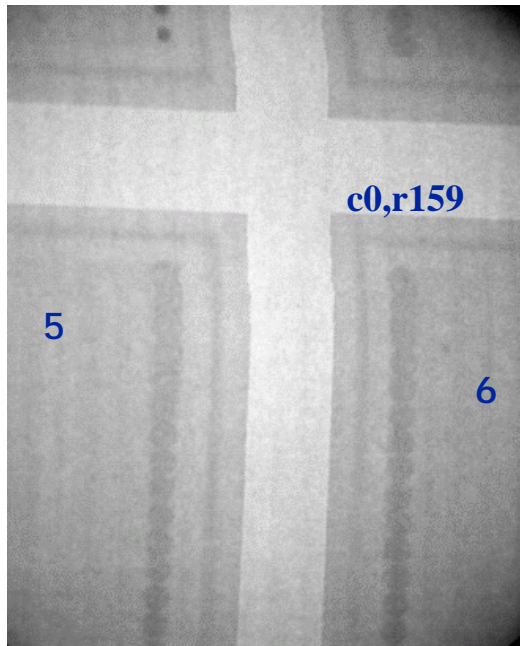
- **Source scan** can test the connectivity of the sensor with the electronics:
 - Missing bumps if good electronics and nothing seen with source



Cd109: Raw hits distribution
Shape of components on the flex are visible (MCC, resistors)



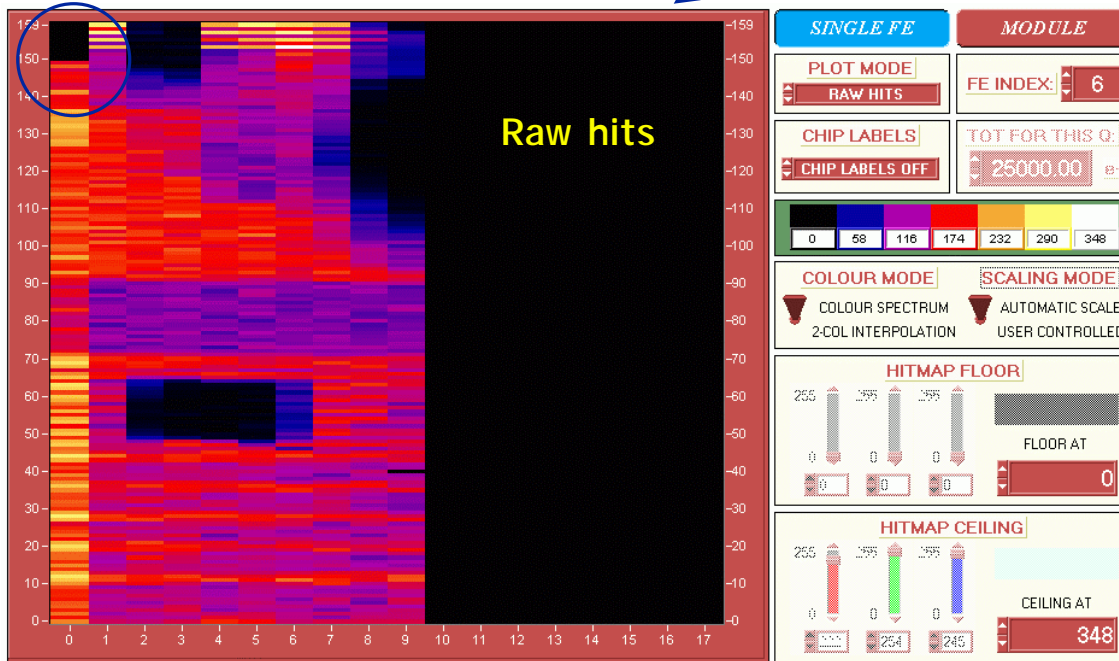
X-ray comparison: merged pixels



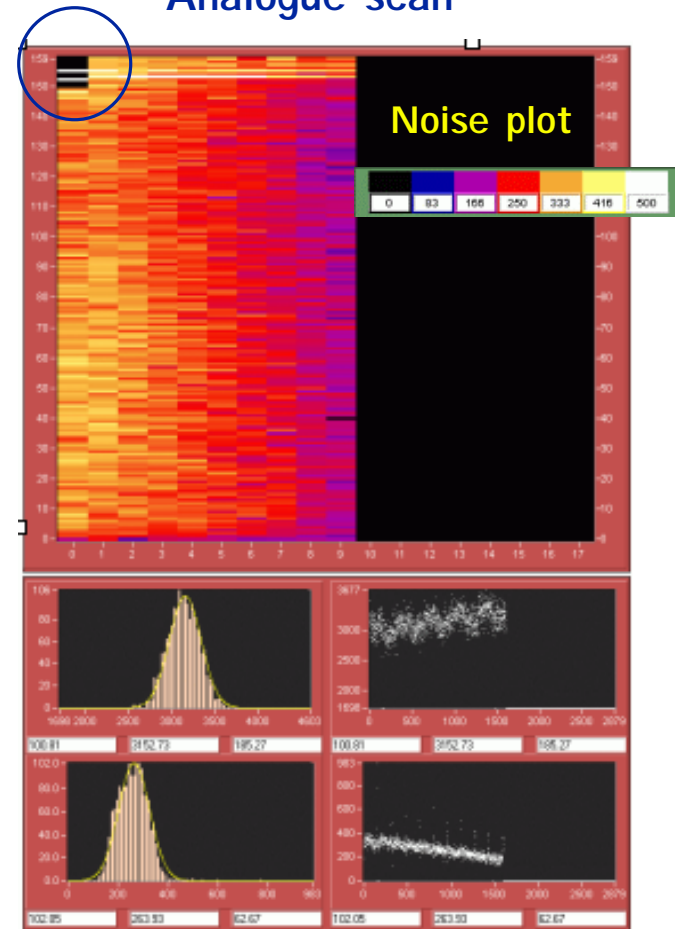
X-ray



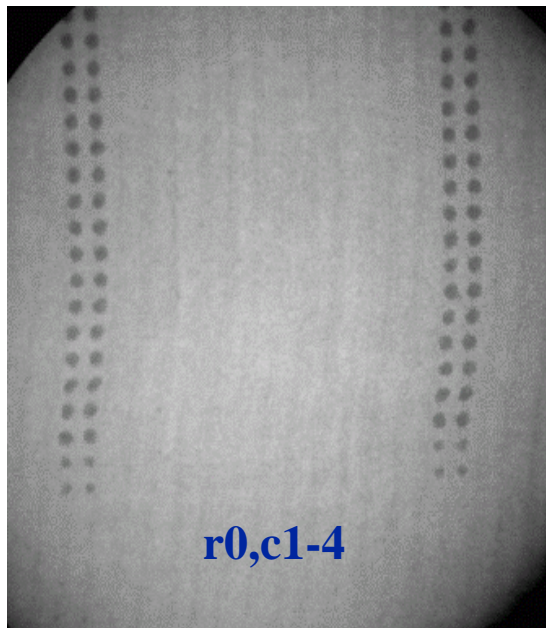
Cd source scan



Analogue scan



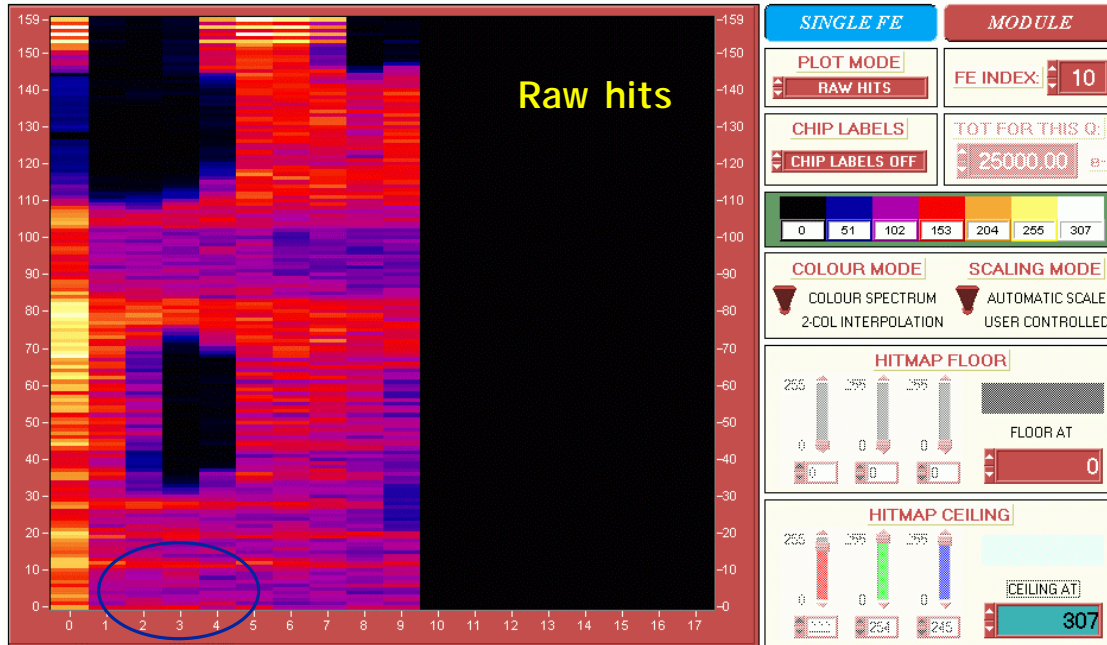
X-ray comparison: small bumps



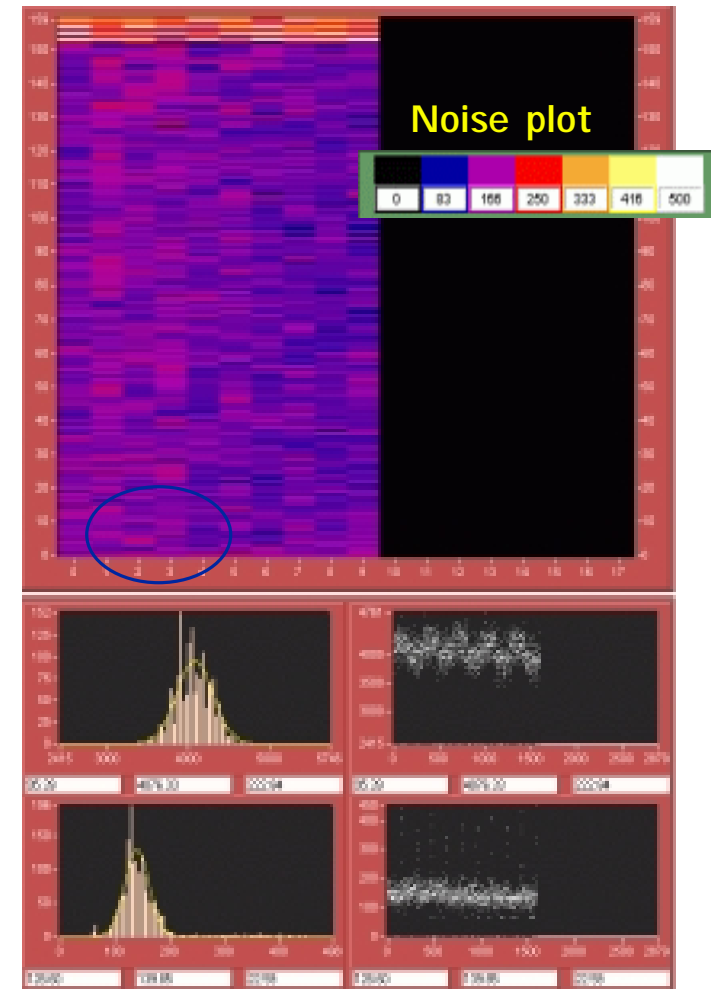
X-ray



Cd source scan



Analogue scan



Global yield

- ~100K analysed channels (4 modules, some single chips)
- Mean threshold $\sim 4000 e^-$, mean noise $\sim 200 e^-$
- Some large zones (mainly in col0) of merged pixels
- **Merged** channels (*i.e.* bad channels coupled with a very noisy pixel):
 - 0.1% *i.e.* ~ 2 pixels/FEchip
- **Missing** channels (*i.e.* good electronics pixels but no signal with source):
 - $\sim 2 \cdot 10^{-5}$

Conclusions

- The AMS bump-bonding technique has been reviewed
- Bumps have an electrical resistance ($O(2\Omega)$) which fits the FE electronics requirements
- Bumps can stand transverse displacements of $\sim 8 \mu\text{m}$ without problems on the connectivity
 - Still to be checked with long term test
- The defect yield is small:
 - ~ 2 merged pixels/FE chip (0.1%)
 - $\sim 2 \cdot 10^{-5}$ missing pixels