

# Radiation Hard/Tolerant Technologies (Pixel Detector)

- Introduction
- Radiation hardened technologies
- Rad-tol deep submicron technologies
- Summary

P.Jarron

G. Anelli, F. Anghinolfi, M. Campbell, F. Faccio, J. Kaplon, K. Kloukinas  
E.Heijne, A. Marchioro, A. Paccagnella, A. Rivetti, W. Snoeys .. RD49



# Radiation Hard Technologies

- History and trends
- Experience in HEP community
- Design aspect
- Yield



# What technology for readout chips of Pixel detector

- Challenging specifications
- Technology choice driven by device and layout density (vital)
  - better with advanced CMOS technologies
- Present technology options
  - Use radiation hardened technology with “guaranteed” hardening
  - Use deep sub micron CMOS with radiation tolerant design



# Brief History

- Impressive number of hardened technologies tested by HEP community since 10 years
  - UTMC, TCS-HSOI3HD, HARRIS...
  - Honeywell Bulk-0.8, Honeywell SOI-0.8, DMILL
  - and finally the Radtol deep submicron approach
- One mistake
  - hardening circuit = rad hard technology
- Issues
  - disappearance of rad hard technologies
  - hardened processes behind main stream technologies



# In 1994: Perry COTS Initiative

- Buy more commercial technology/products
- Use industrial specifications
- Reduce costs

*(1) Willam J.Perry, "Specifications and standards - a new way of doing business"  
Memorendum, 1994.*



# Controversy: Is radiation hardened technology necessary

SATELLITE SURVIVABILITY

## The Commercial and Military Satellite Survivability Crisis

*Whether it's natural radiation or radiation from a nuclear blast, can satellites survive? Unless you harden it, the Defense Nuclear Agency doesn't think so.*

*Since Secretary of Defense Perry's memo to buy commercial off-the-shelf products, military questions have been raised about what the impact would be. Defense Electronics has addressed this important issue in previous articles. DE continues this focus with an exclusive article written by key individuals from the Defense Nuclear Agency who share their concerns over the impact of radiation on both commercial and military satellites.*

**G**lobal information exchange has rapidly become the cornerstone for assuring the vitality of worldwide economic, as well as military, institutions. The commercial satellite industry has rapidly grown to support this demand for near instantaneous information exchange around the world. The military has leveraged its commercial assets in recent conflicts and plans to respond to future military conflicts by an even greater exploitation of satellites under an evolving doctrine known as "Information Warfare." Quite simply, the use of commercial satellites is now so critical to our national and global endeavors that the consequences of the loss of these assets is unthinkable, yet such a loss is a very real possibility.

Studies by the Defense Nuclear Agency (DNA) show that the explosion of a single high altitude low yield nuclear weapon could destroy \$14 billion worth of low earth orbit satellites that would transit through the environment of radiation he is produced by such a nuclear event. This paper discusses the threat to commercial satellites from the natural radiation environment and a credible yet conservative assessment. Third World nuclear threat, the role that radiation tolerant microelectronics play in satellite systems, the impact of the post-Cold War budget realities on the radiation tolerant microelectronics and satellite industries, and development programs that, in cooperation with commercial semiconductor vendors, developed radiation hardened semiconductor devices that followed the rapidly evolving commercial semiconductor market. This continuous development cycle supported military needs and commercial satellite requirements both required DOD budgets resulting from the end of the Cold War, has development cycle has naturally slowed and the devices presently in use are rapidly becoming obsolete. The continued success of reduced industrial and government sponsored research and development and the rapid maturation of radiation tolerant integrated circuits has resulted in the erosion of domestic radiation tolerant vendors, i.e., the 20 vendors available in 1990 have been reduced to 4 today. This vital domestic resource is in peril of disappearing. DOD support will be required to ensure that future generations of microelectronics are radiation tolerant. Lack of this support and potential unavailability of future generations of radiation tolerant microelectronics from domestic sources also will jeopardize the vital U.S. satellite industry.

The Van Allen radiation belts, and solar and galactic high energy particles

**By R.C. Webb, Les Paikuti, Lew Cohn, Lt. Col. Glenn Kweder and Al Costantine**

radiation tolerant microelectronics and satellite industries, and concludes by describing what is required to ensure the long term availability of radiation tolerant microelectronics through domestic suppliers.

**Background**

Satellite designers are continually constrained by the demands for increased capability, decreased power consumption and lower costs per bit. Thus, they strive to increase the performance of their systems under these constraints. Unfortunately, as microelectronics devices grow in sophistication, increased integration density and higher operating speeds they become increasingly vulnerable to radiation, as illustrated in Figure 1.

To meet the demands of the harsh natural radiation environment, radiation tolerant microelectronics must be used in space systems. During the Cold War the need to harden strategic

Category	Effect
Total Ionizing Dose	Degradation and/or failure as a function of ionizing radiation accumulation (i.e., months - years)
Single Event Effects	Relatively instantaneous device upset or destruction (e.g., latchup, burnout or gate rupture)
Displacement Damage	Degradation of solar cells, charge-coupled sensors, fiber optics, etc. over a period of time due to lattice effects less severe than SEE on neutralizing dose effects

Table 1. Effects of space radiation on semiconductor devices. (Table courtesy of the DNA)

JULY 1995 DEFENSE ELECTRONICS AUGUST 1995 21

From "defense Electronics" August 1995

"... Can Satellite survive? Unless you harden it, the defense Nuclear Agency doesn't think so..."

consequence of post cold war DOD budget:

"20 rad-hard vendors in 1990, 4 today...."

Source L. Dusseau/Montpellier



# Radiation hardened technologies

- HEP has contact with 2 vendors
  - Honeywell: thin SOI RICMOSIV
  - TEMIC: thick SOI DMILL
- Other vendors
  - Lockheed Martin
  - Sandia Lab
  - Fabless vendors, SOS Peregrine
- Market driven by defense and Space
  - Defense: TID tens of krad
  - Space: TID hundreds of krad
  - Readout chips for pixel, TID up to 30 Mrad



# Technologies for Pixel readout

	ALICE LHC-b	ATLAS	CMS	BTeV
<b>Devices</b>				
/cell	1500	250	125	
/cm <sup>2</sup>	7.5 M	1.2 M	0.6 M	
<b>Pixel cell size</b>	420 μm x 50 μm	400 μm x 50 μm	150 μm x 150 μm	400 μm x 50 μm
<b>Techno</b>	I .25 μ	DMILL RicmosIV	DMILL RicmosIV	I .25 μ T .25 μ



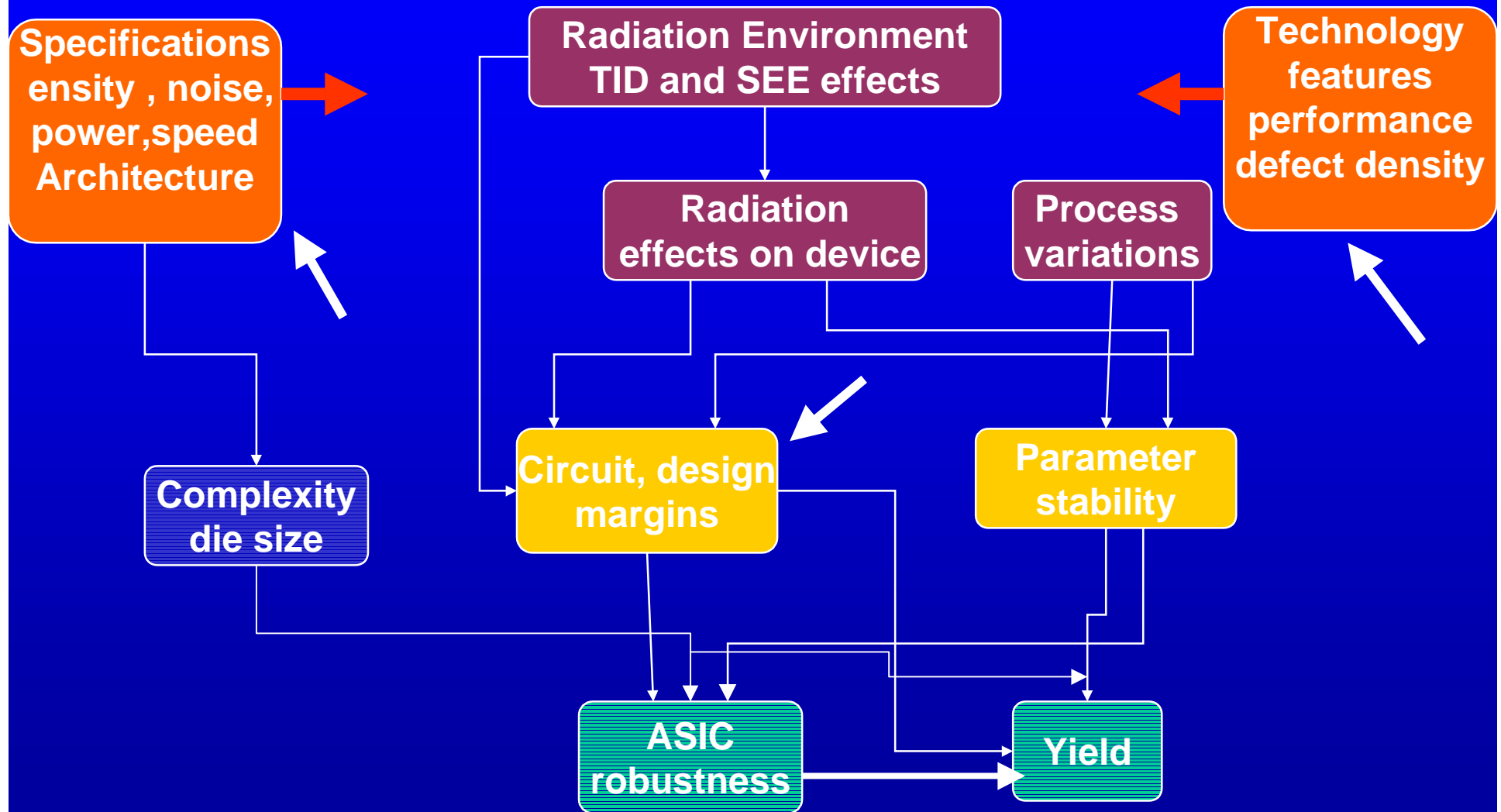


# Rad hard Technologies: comments

- **Radiation hardening**
  - DMILL and RICMOSIV have radiation induced parameter shifts of devices “manageable”
  - Circuit design has a big impact
  - SEU : better with RICMOSIV (see CMS note 2000/036 R. Horisberger et al.)
- **Yield, a difficult story...**
  - rad hard technologies are low volume
  - special processes, not main stream
  - design margins not sufficient
- **Density**
  - RICMOSIV better density, 3 metal layers
  - 2 metal layers, lost silicon in DMILL



# Design-process-yield-hardening



**In production: good radiation hardening and yield**

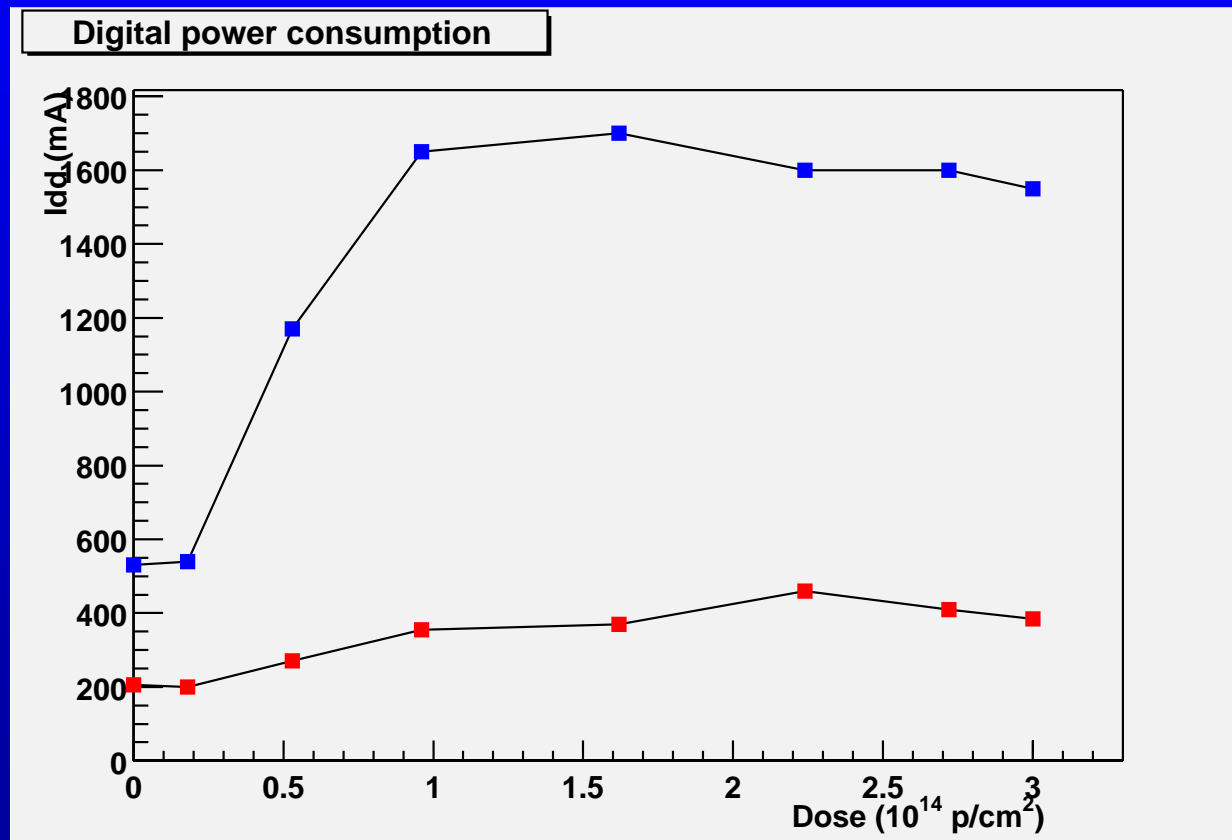
*Pixel2000 Genoa 6 June 2000 P. Jarron-CERN*



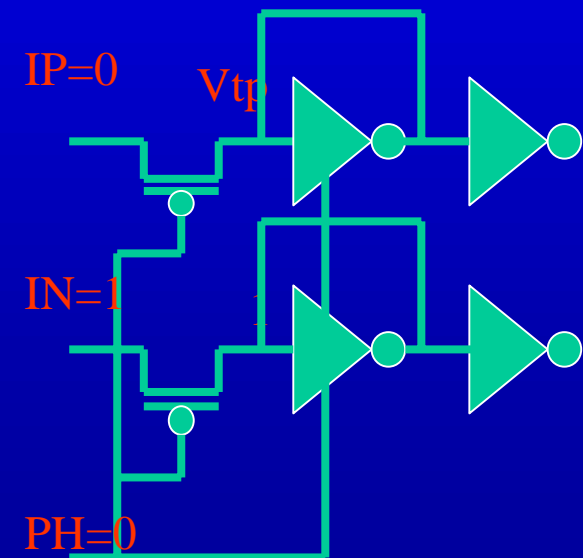
# Hardening and design

## Radiation response of 2 ABCD2T -DMILL lots

Problem with a modified transmission gate latch



Transparent mode  
input switches on  
inverters can be in  
conduction regime

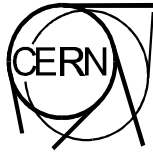


# Yield of rad hard ASICs

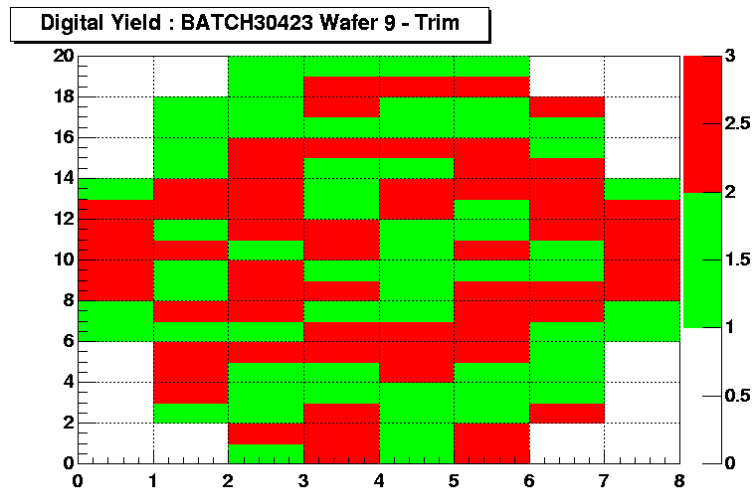
- Very few statistics
  - ATLAS: SCT ABCD2T , TRT DTMROC
    - yield 50% on the digital CMOS part for 50 mm<sup>2</sup> , 200 000 transistors, 27% with bipolar circuits
    - digital yield improved to 60%, and 37% in the back up lot
  - Pixel ATLAS
    - no yet conclusive
  - Pixel CMS
    - not yet available
  - SVX3:
    - see R. Yarema (Perugia), not yet solved



# Yield: wafer mapping on DMILL



Digital tests - results from  
30423 wafer #9



Map of the wafer with the ABCD chips tagged according to the results of digital tests

- RED - no defect in the digital part
- GREEN - defect(s) in the digital part

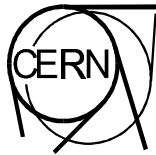
**Yield of CMOS circuit: 50%**

11-May-00

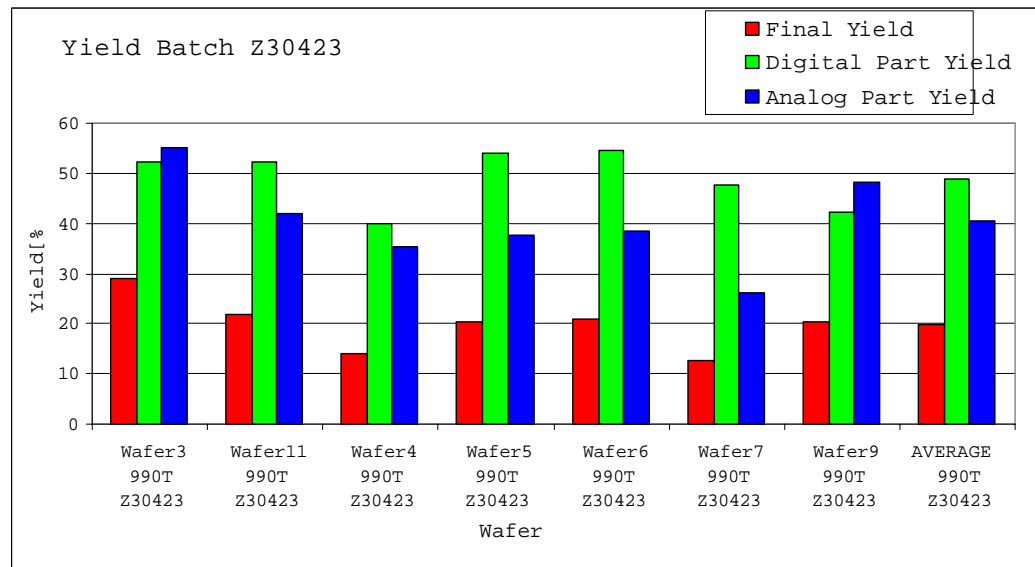
IV meeting on FE electronics for high resolution tracking detectors, PERUGIA May 16-19th, 2000



# Yield: DMILL wafer to wafer



## Yield results



Yield for analogue part of the ABCD (based on calculation of defects in analogue part for the ABCD2T for chips with no defects in the digital p

ABCD2T  
J. Kaplon

11-May-00

IV meeting on FE electronics for high resolution tracking detectors, PERUGIA May 16-19th, 2000

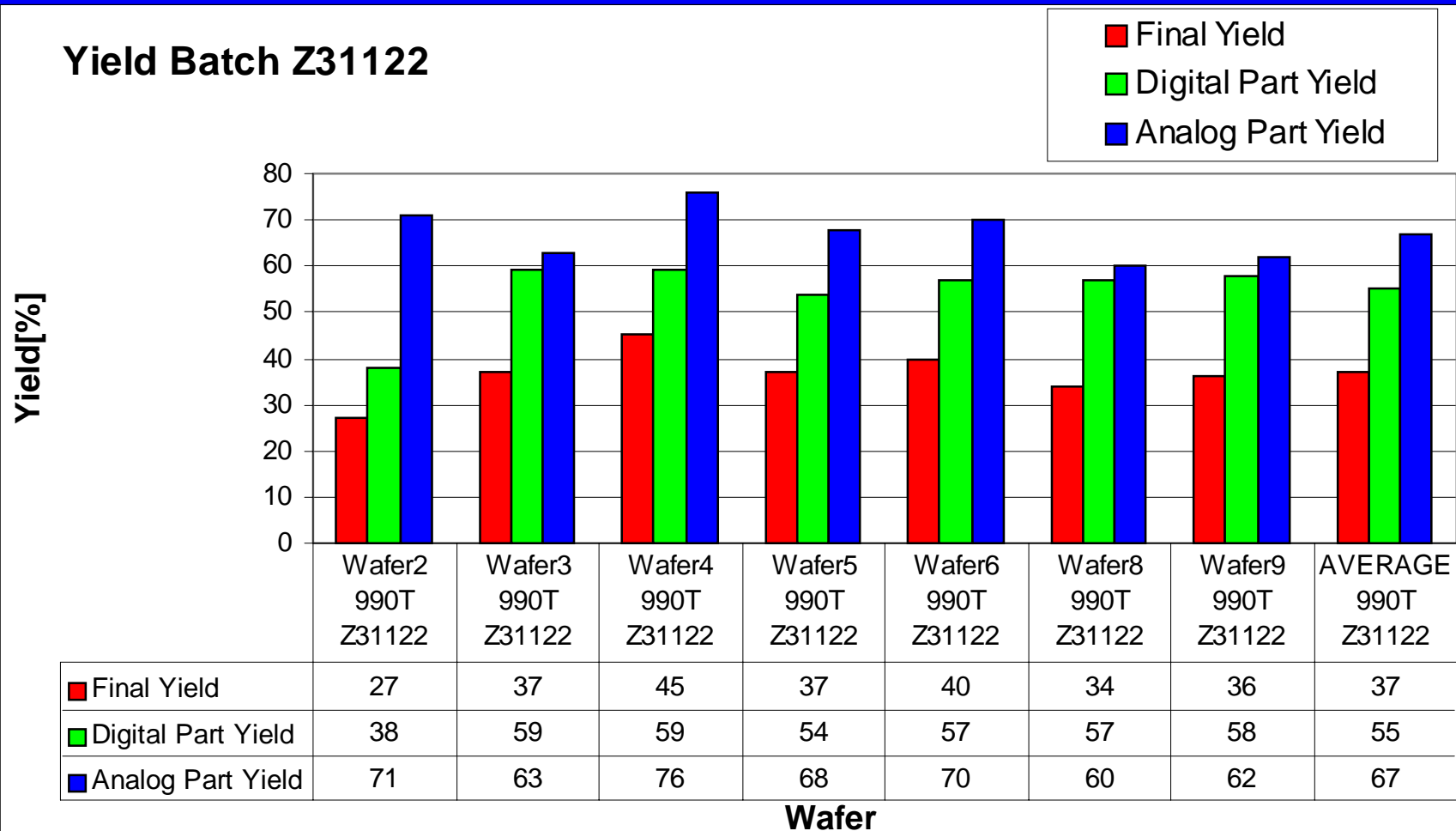


# Yield of the back up ABCD2T lot

## 1st June 2000

Jan Kaplon

Yield Batch Z31122



# Deep submicron technologies

- Trends with device scaling
- Availability of vendors
- Radiation tolerance
- Issues



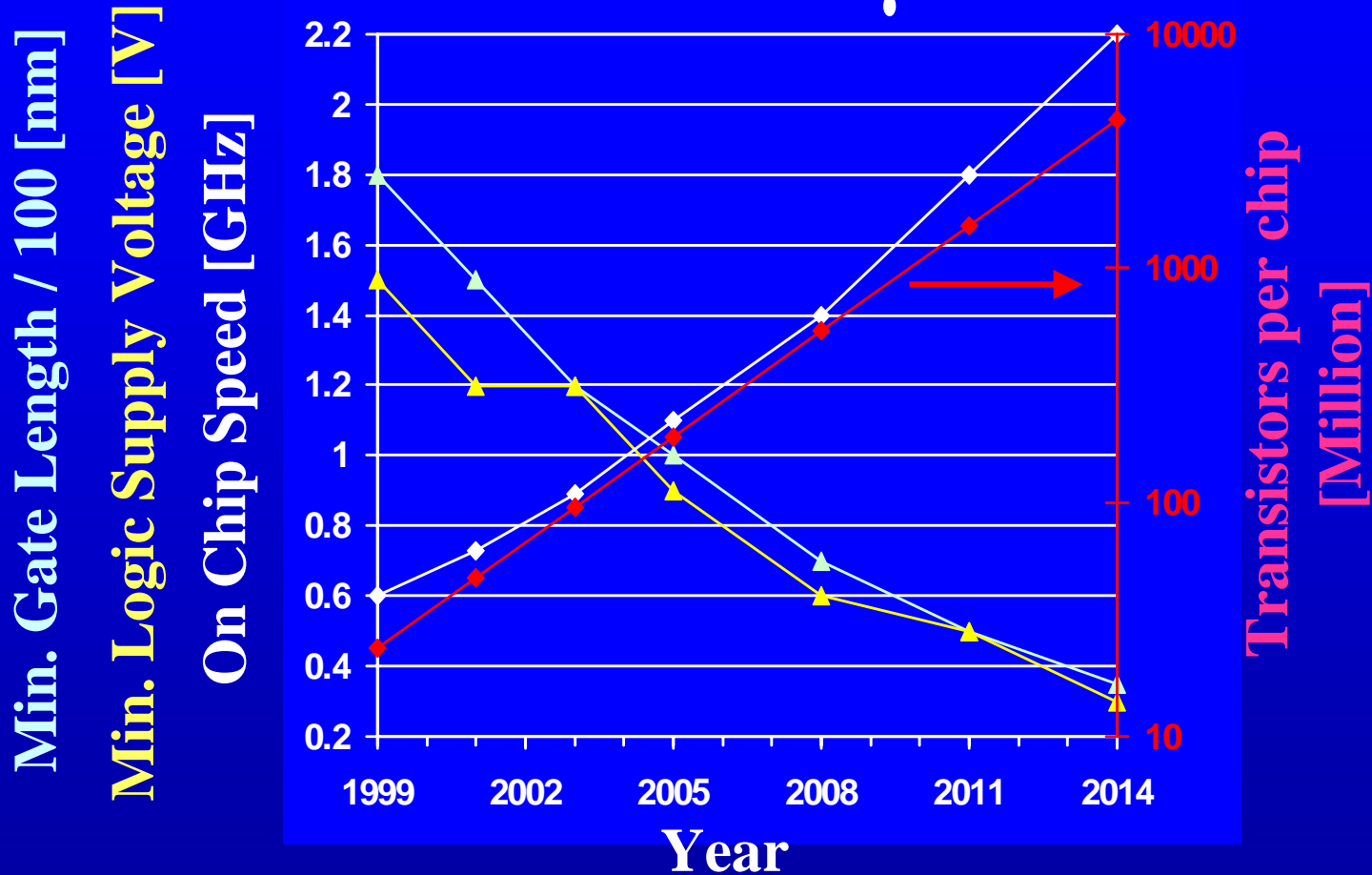


# Motivation of the radiation tolerant approach in 0.25 (RD49)

- Radiation tolerance of thin gate oxide
  - rad-induced holes removal by e tunneling
  - very few rad-induced interface traps
- Features of deep sub micron technology
  - large scale integration - density
    - acceptable density of rad tol design
  - performance
    - speed, noise and matching are good
  - low power
  - main stream, large volume process
    - high yield, low cost
  - attractive for pixel readout chip



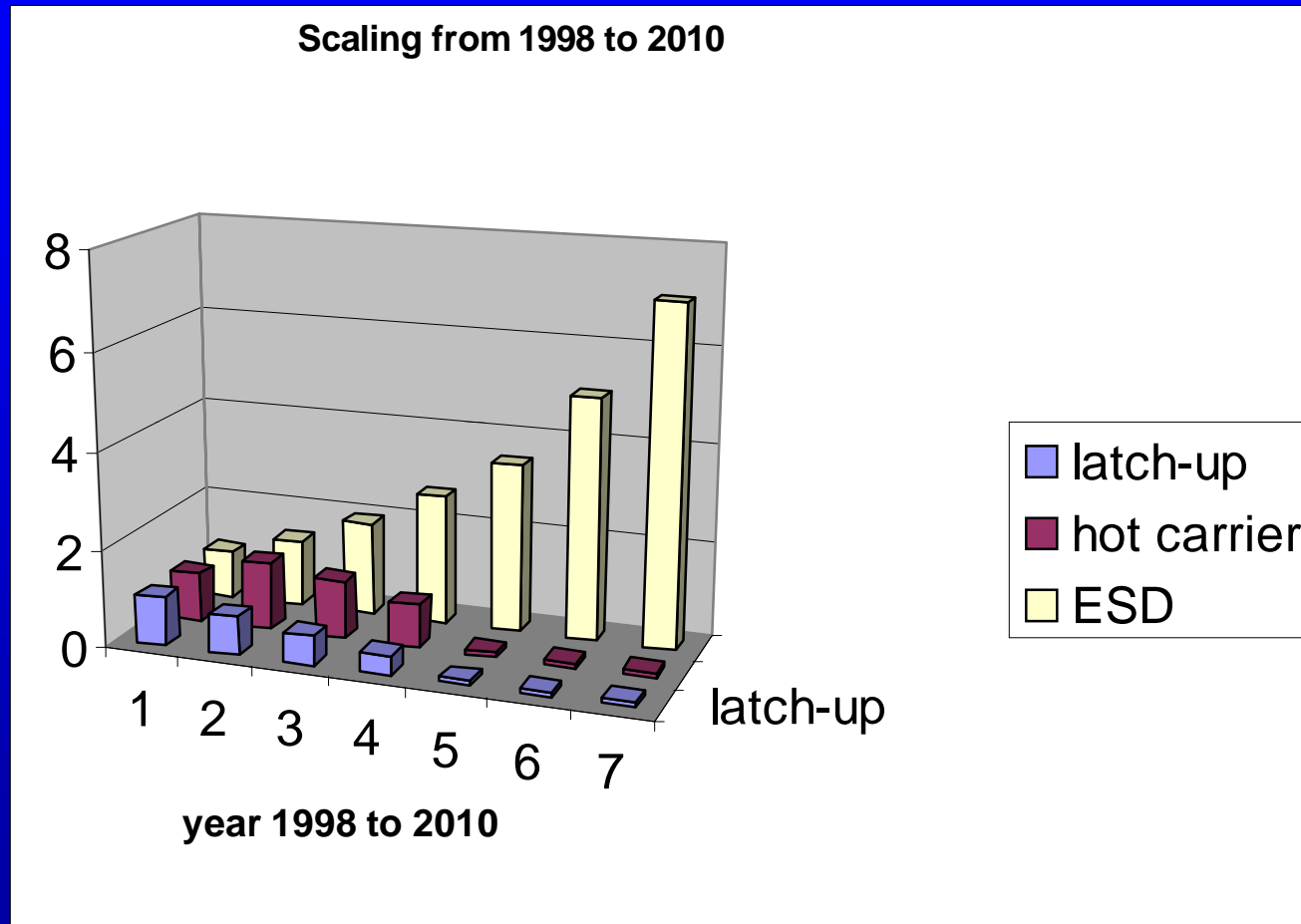
# Technology scaling beyond CMOS 0.25 $\mu\text{m}$



Compiled by G. Anelli Semiconductor Industry Association  
The International Technology Roadmap for Semiconductors (1999 Edition)



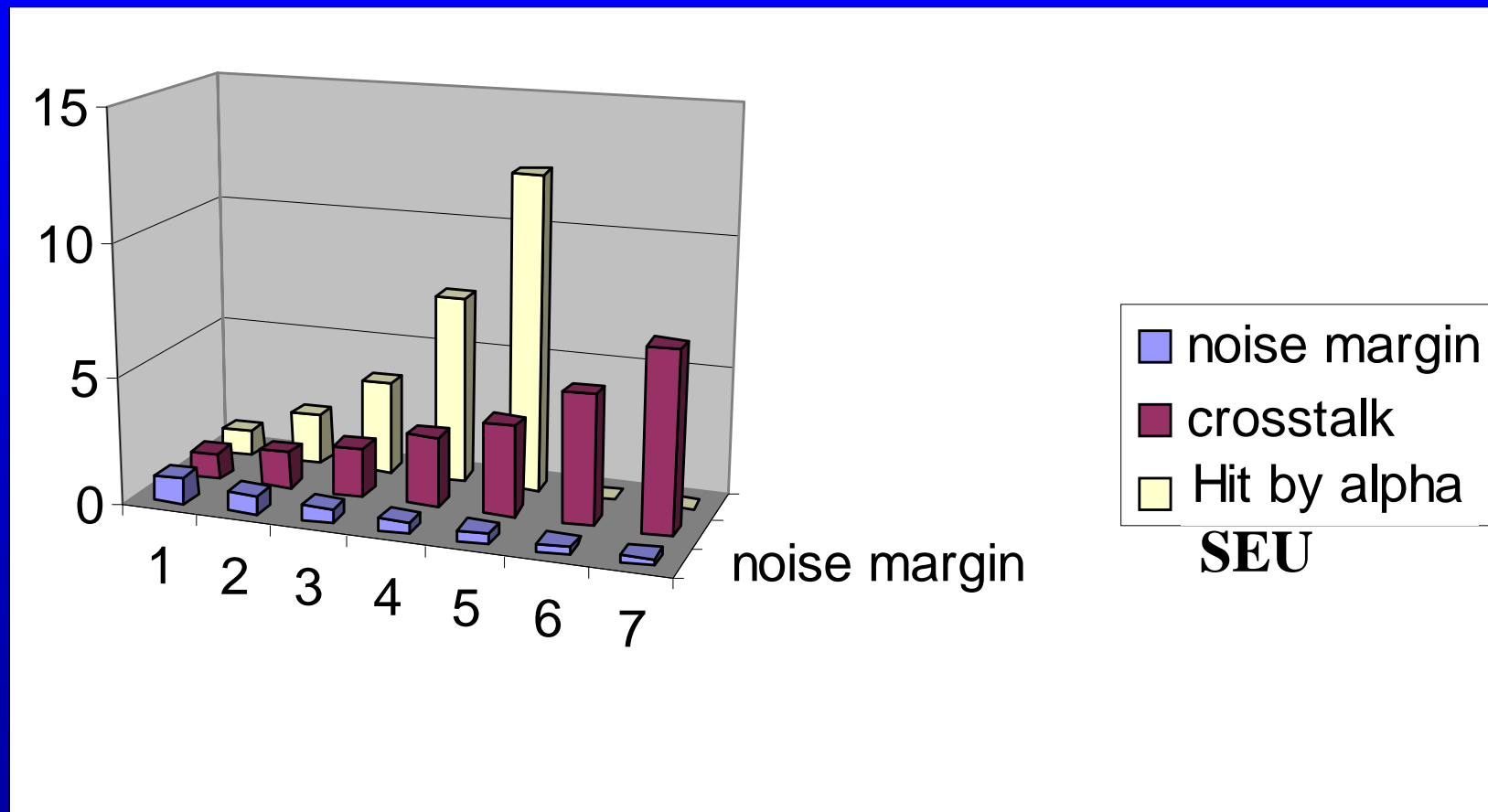
# Trends with device scaling



H. Veendrick, "Deep-Submicron CMOS ICs", Kluwer Academic Publishers, 1998



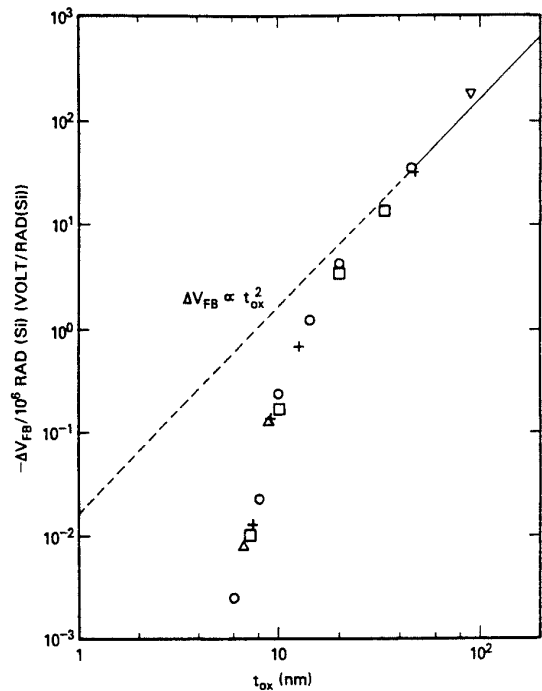
# Trends devices scaling



H. Veendrick, "Deep-Submicron CMOS ICs", Kluwer Academic Publishers, 1998

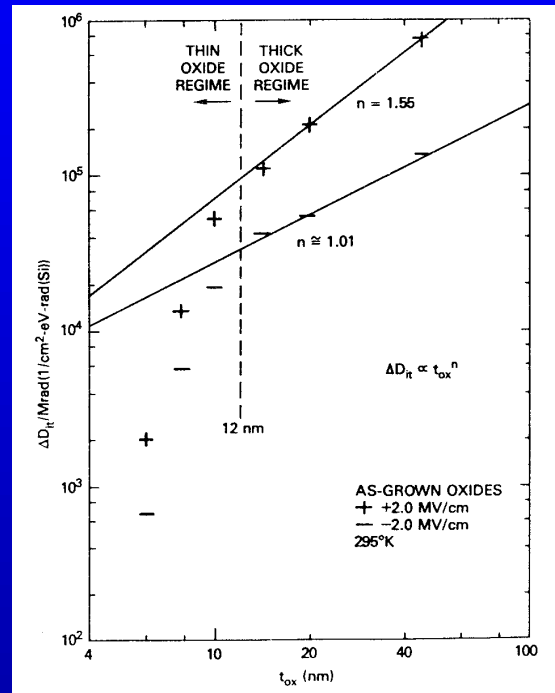


# Radiation effects and $t_{ox}$ scaling holes removal by e tunneling



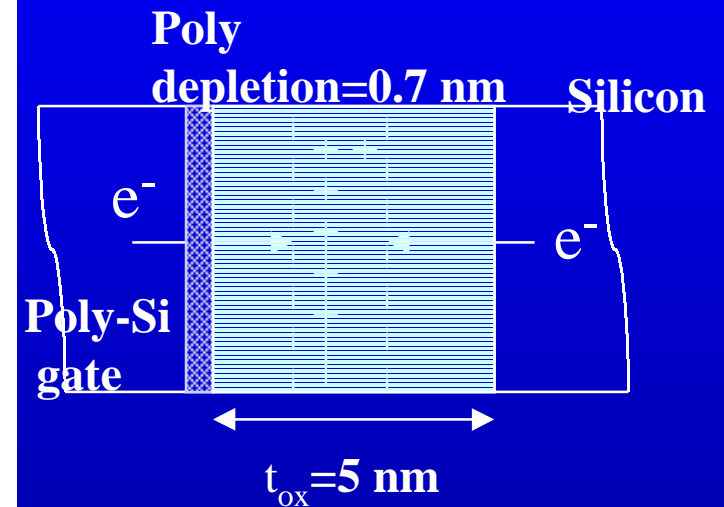
**Vt-shift**

N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986



**Interface traps**

**Today 0.25 technology**



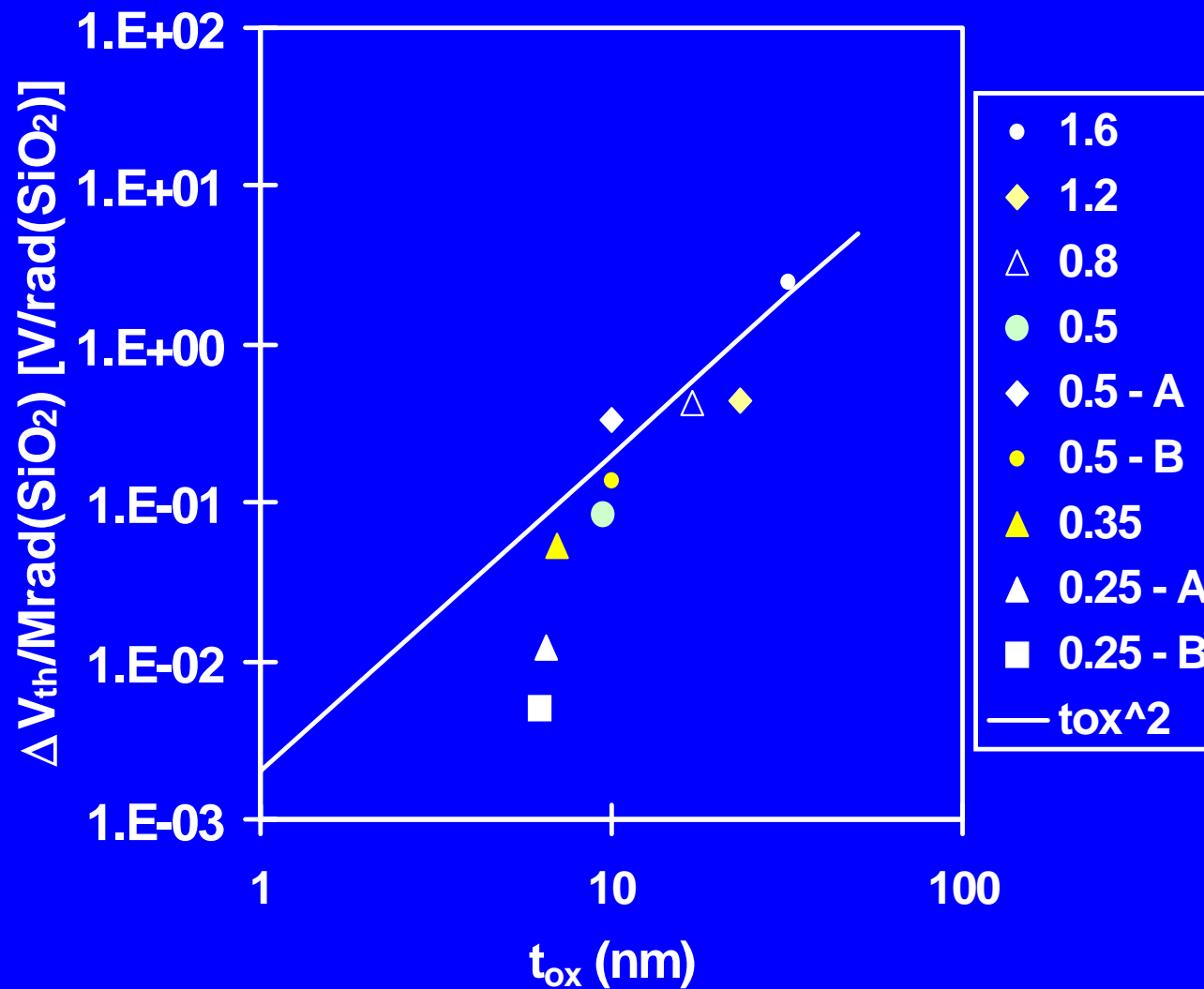
**Annealing  $\propto \text{Log } t$**

**Front speed  $\approx 0.2 \text{ nm/t-decade}$**

**Holes removal takes few hours  
in 5nm oxide**



# RD49 results on several technologies

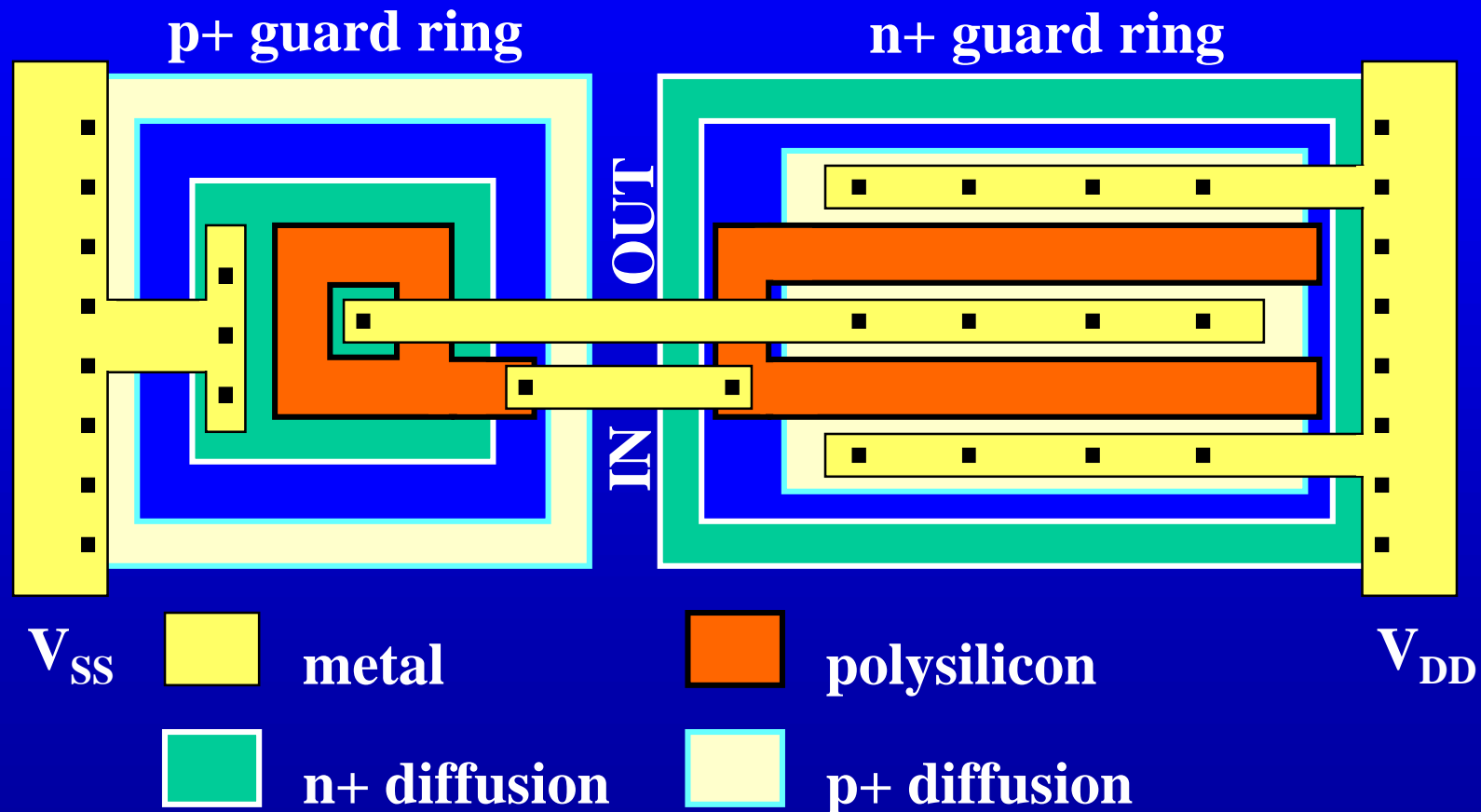


# Conclusion of the recent book of T. Oldham

- Radiation Ionizing effects in MOS oxides :  
ISBN 981-02-3326-4
  - Update of Ma and Dressendorfer book  
published 3months ago
  - “... the general problem of radiation induced, gate  
oxide, threshold-voltage shifts may eventually be  
eliminated by the natural development of more  
advanced microelectronic technology with thinner  
oxides. At this point, the special radiation  
problems in electronics devices will be found in  
isolation structures.”
  - and SEU!!

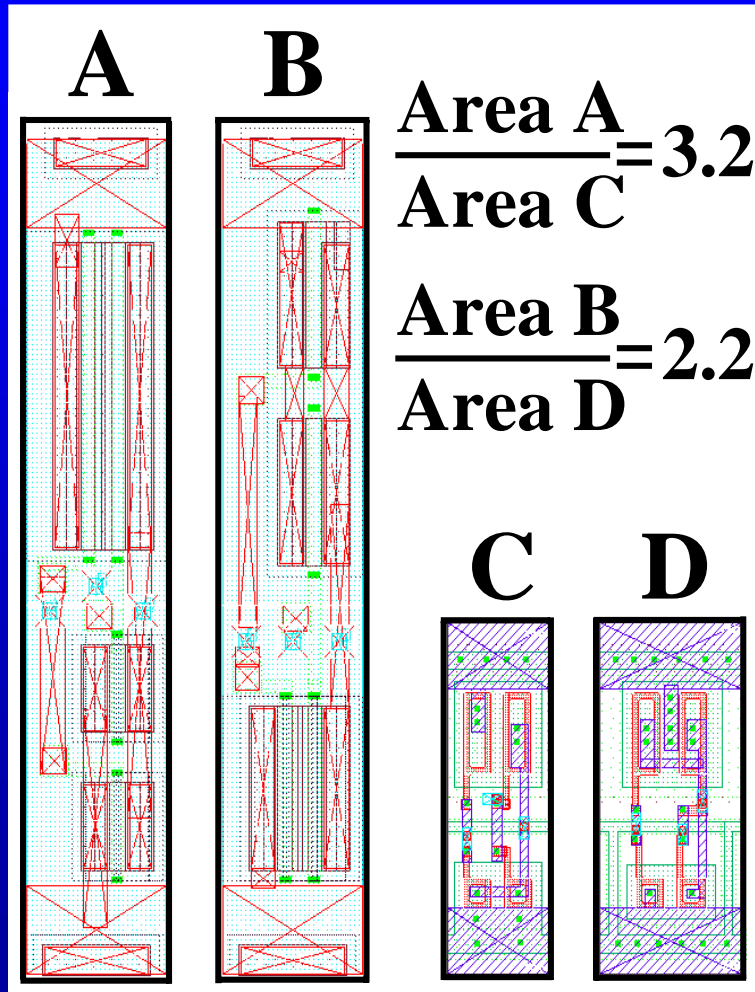


# Radiation tolerant layout approach - RD49





# Density and speed from CERN radtol lib



**A & B : 0.6  $\mu\text{m}$  standard**  
**C & D : 0.25  $\mu\text{m}$  rad-tol**

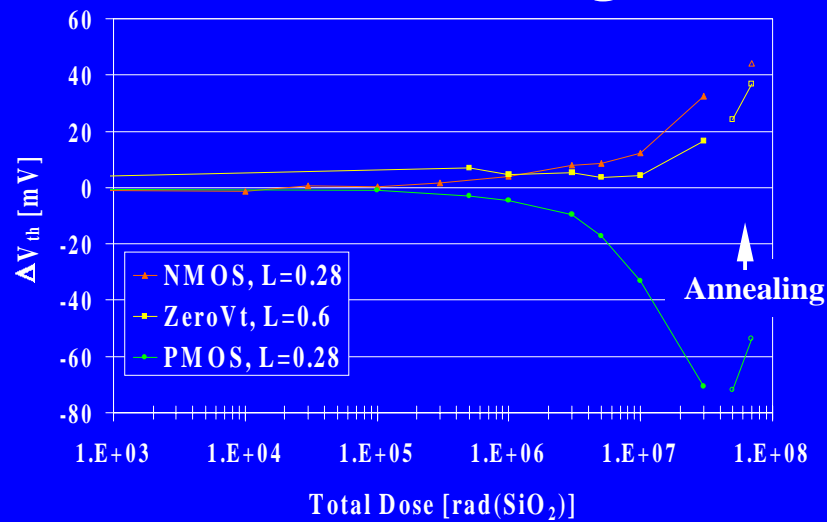
**Inverter with F.O. = 1**

	0.6 $\mu\text{m}$	0.25 $\mu\text{m}$
$V_{DD}$ [V]	3.3	2
Delay [ps]	114	48
Pwr [ $\mu\text{W}/\text{MHz}$ ]	1.34	0.14
Area [ $\mu\text{m}^2$ ]	162	50

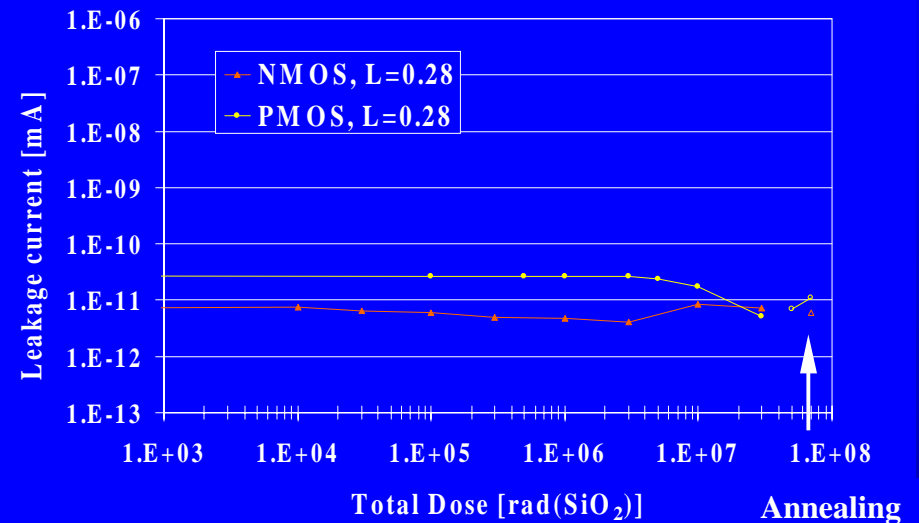


# Total dose results up to 30 Mrad 0.25 $\mu\text{m}$ technology

## Threshold voltage



## Leakage current



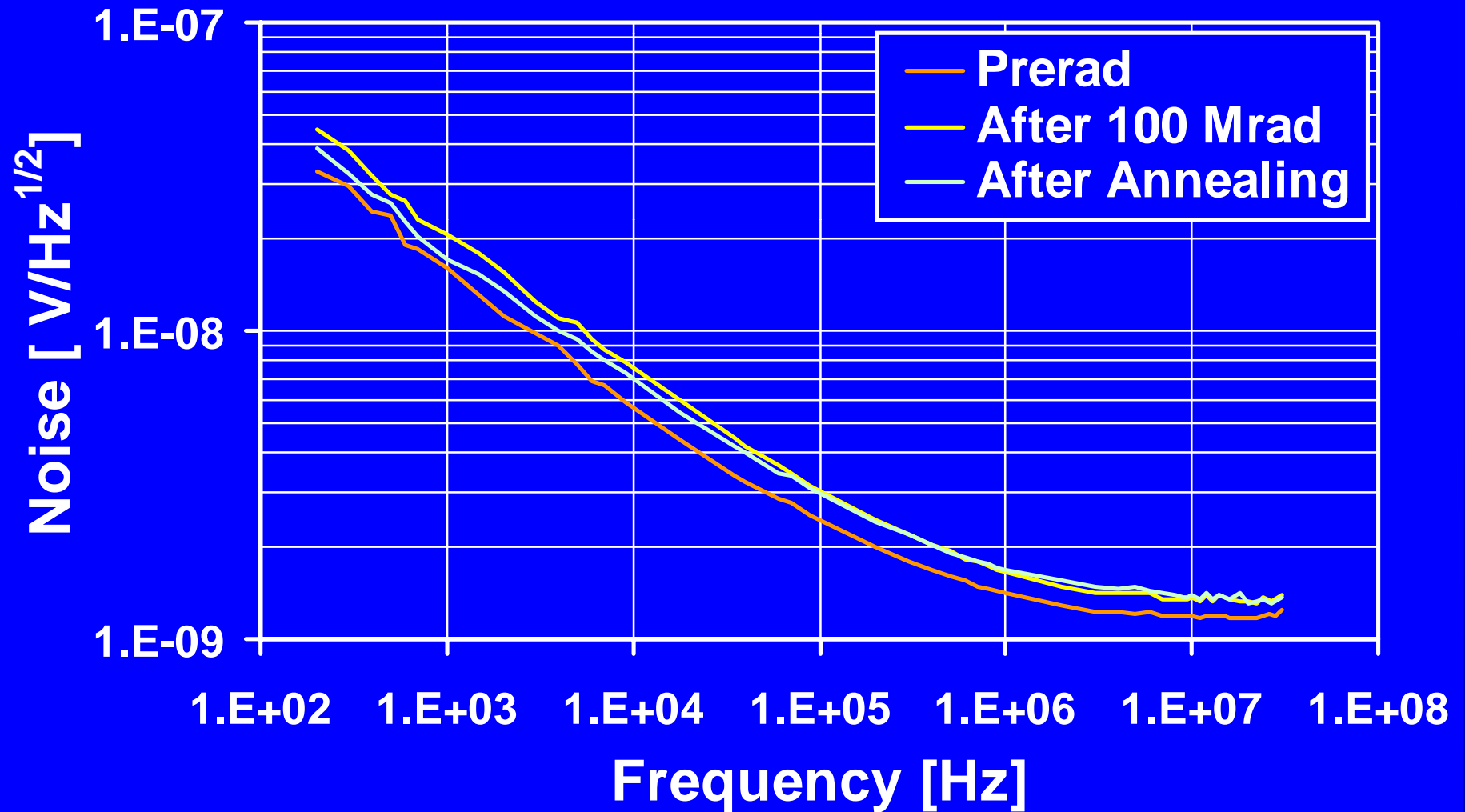
**Mobility degradation:**

**< 6% NMOS**

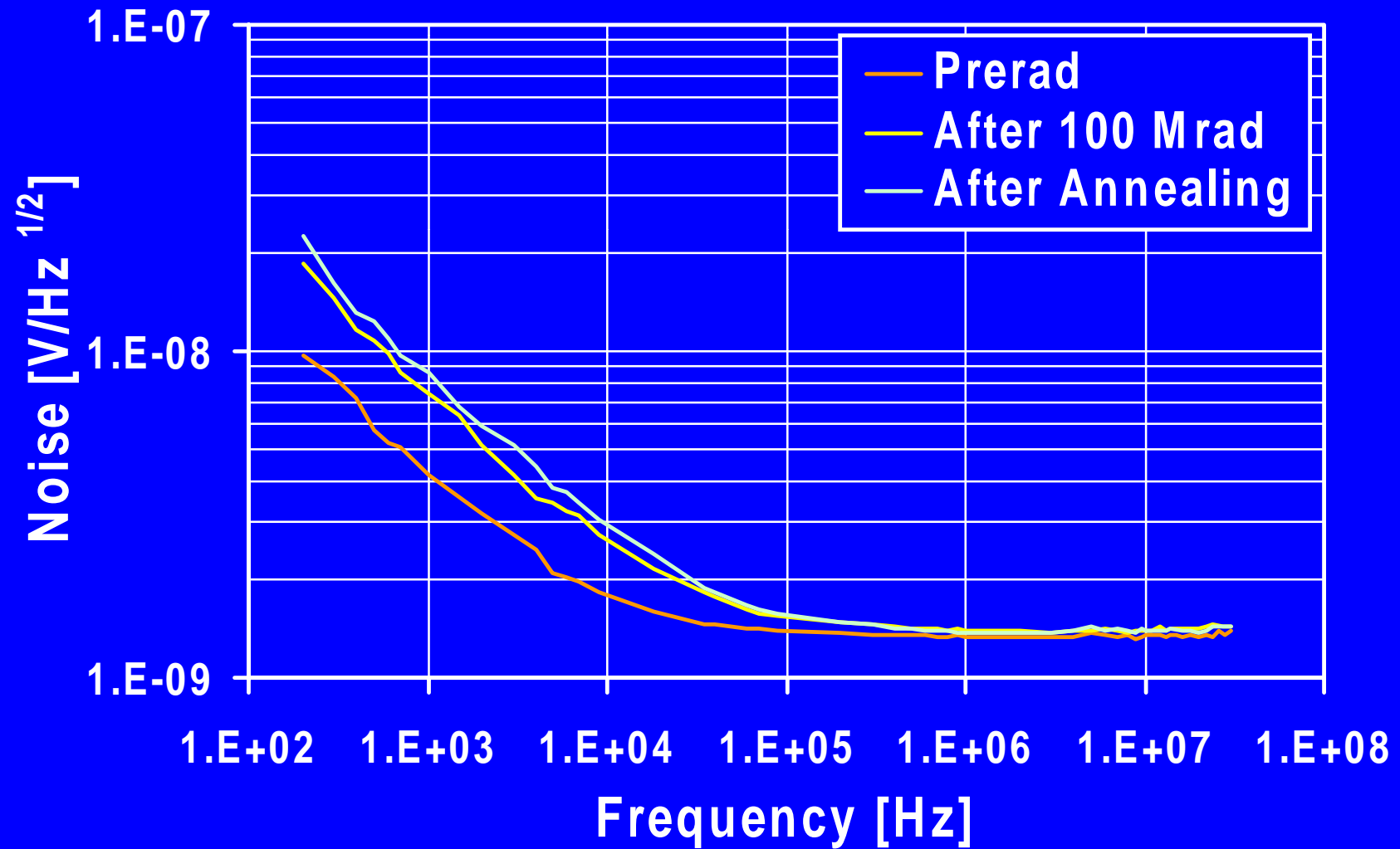
**< 2% PMOS**



# N-channel noise spectrum



# P-channel noise spectrum



# 0.25 $\mu$ m radtol HEP ASICs

- Designed, fabricated and tested
  - ALICE2, APV25, 10 Mhz 10bit ADC, 2V dynamic range analog memory, 1Gb/s serialiser, optical receiver, BTeV pixel readout +....
- Full FE chip designed, in fabrication
  - ALICE-LHC-b pixel readout
  - ALICE SDD readout
  - LHC-b silicon readout
  - +...
- So far, positive results



# Access to DSM technologies

- **0.25 $\mu\text{m}$  ( $V_t = 0.5\text{V}$ )**
  - CERN (MPW), RAL(support) radtol lib
  - IMEC UMC radtol lib
  - TSMC direct access, no radtol lib
  - CMP ST no radtol lib
  - MOSIS- TSMC
  - +....
- **0.18  $\mu\text{m}$  ( $V_t=0.4\text{V}$ )**
  - IMEC UMC radtol lib
  - CMP ST, possible radtol lib from ST
  - TSMC, no radtol lib
  - MOSIS TSMC
- **0.15  $\mu\text{m}$  TSMC direct access**



# UMC 0.25 $\mu$ CMOS

## ▼ Base technology is the logic process (1 poly, 5 metal)

<b>Well formation</b>	<b>Shallow-Trench (STI)</b>
<b>Isolation</b>	<b>Shallow-Trench (STI)</b>
<b>Poly Gate</b>	<b>N+, P+ Poly / Salicide</b>
<b>Gate Oxide</b>	<b>50 Å</b>
<b>N/P MOS length</b>	<b>0.24 / 0.24 <math>\mu</math></b>
<b>Contact / Via size</b>	<b>0.32 / 0.4 <math>\mu</math></b>
<b>Vt N/P MOS</b>	<b>0.5 / -0.6 V</b>
<b>Idsat N/P MOS</b>	<b>620 / 280 <math>\mu</math>A/<math>\mu</math>m @ 2.5 V</b>
<b>Gate Delay/Stage</b>	<b>40/36 ps @ 2.5 V</b>

Source : UMC

## ▼ Added with analog options

- high res poly
- capacitors : double poly or MM capacitors

# UMC 0.18 $\mu$ CMOS - logic process

<b>Key Process Features for the L180 Families</b>	
Technology Node :	0.18um
Core Voltage :	1.8V
I/O Voltages :	2.5V/3.3V
Poly/Metal Layer :	1P6M (max. 6 metals)
Substrate/Well formation :	P-sub, Twin-Well
Isolation :	Shallow Trench Isolation
Gate Oxide thickness :	35A/50A(2.5V I/O)/65A(3.3V I/O)
Silicide :	Cobalt Salicide
ILD Planarization :	HDP/PE-PSG (CMP)
Interconnect :	W-plugs/Al metallization w/ top 2 layer Cu option
Passivation :	HDP/PSG/PESIN with Polyimide option
Poly pitch :	0.46um
Metal Pitch:	0.52um for metal 1
	0.56um for metal 2 to 5
	0.88um for top metal
<b>Speed</b>	
Ring Oscillator Delay :	27 ps
<b>Leakage</b>	
Standby Current (Ioff norm) :	0.01 nA/um

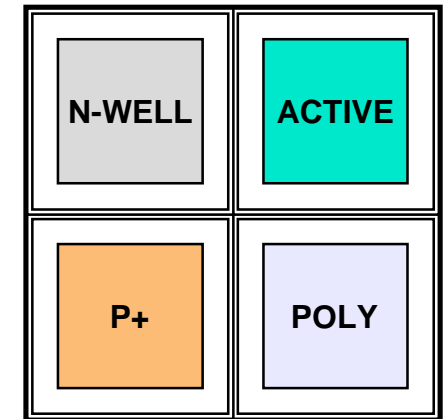
Source : UMC



## Multi Level Mask (MLM) techniques reduce the high mask costs

- ▼ Standard mask set is very expensive
  - Full mask with one mask per design layer
  - 60 k\$ @ 0.35 $\mu$  CMOS . . . 300 k\$ @ 0.18 $\mu$  CMOS
  - only possible for high volumes or “XXL” chips

- ▼ Multi Level Mask set
  - 4 design layers per mask
  - mask costs reduced by about 60%
  - IC area limit : 9.5 x 9.5 mm
  - ideal solution for
    - prototyping of “L” chips
    - pre-series
  - Run start at any time



**RETICLE (20 x 20 mm)**  
4 layers per reticle

- ▼ Available for Alcatel Microelectronics +ESM

# Qualified Cell libraries and design kits are key to success

## ▼ Libraries

- Standard cell library (digital and analog) from foundry
- Available for all technologies
- For UMC 0.25 $\mu$  CMOS : third party libraries from Virtual Silicon Technology

## ▼ Design kits

- for most of popular **EUROPRACTICE** software tools
  - Cadence, Mentor Graphics, Synopsys, Tanner, ...
- about 45 design kits

## ▼ FREE distribution by **EUROPRACTICE** on CD-ROM

- Customer signs NDA with IMEC and receives CD-ROM + key
- Layout stays at IMEC

# Hardness of DSM technology

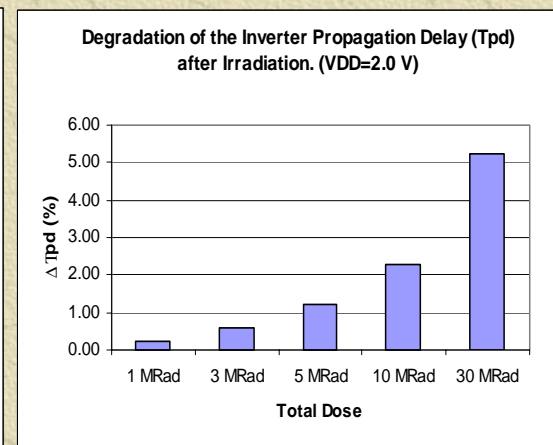
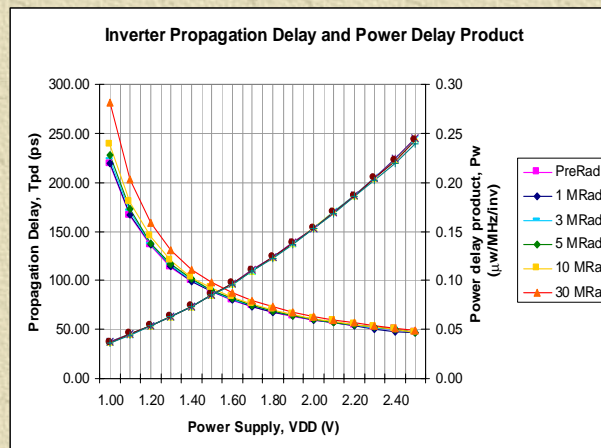
- No indication of TID problem with  $0.25\mu$
- No evidence of hard failure
  - latch-up and single event gate rupture ( see A. Paccagnella work and last RD49 report)
- SEU is an issue
  - not specific to DSM and technology dependant
  - mitigated by design for static FF and memory
- For technologies below  $0.25\mu$ 
  - trends are positive for TID, latchup, not for SEU
  - trends of SEGR not well known
  - pay attention to thicker oxides used in I/O



# CERN radtol 0.25 library: 30Mrad

## Radiation Hardness Test

- # Total Dose Radiation Hardness Test
- # Test Circuit: Ring Oscillator (1001 inverters)



- # Test Conditions:
  - Dose Rate: 29KRad/min
  - Under bias (2.0V) during irradiation @ 25°C

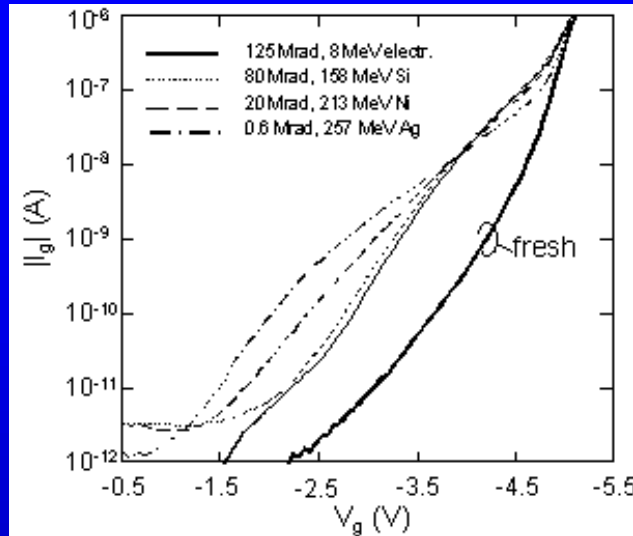
December 9, 1999

KLOUKINAS Kostas, CERN EP/MIC

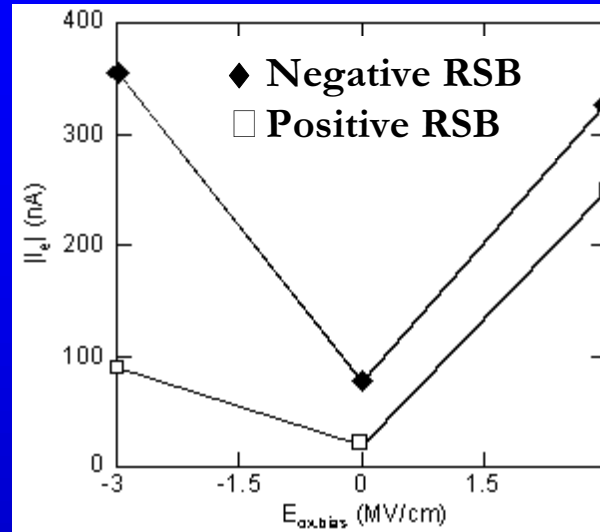
18



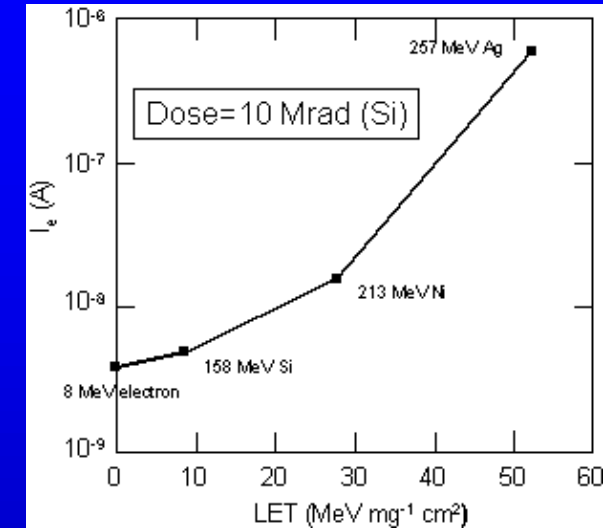
# Rad induced gate rupture in 0.25 ?



$I_g/V_g$



Field dependence



LET dependence

## 2 Non-catastrophic phenomena observed

- radiation induced leakage current RILC (TAT)
- Radiation induced Soft Burnout (heavy ions)

## A. Paccagnella's work on 1mm<sup>2</sup> 4nm gate structure

M. Ceschia, A. Paccagnella, A. Cester, A. Scarpa, and G. Ghidini, "Radiation Induced Leakage Current and Stress Induced Leakage Current in Ultra-Thin Gate Oxides NS-45, No. 6, pp.2375-2382, December 1998.

M. Ceschia, A. Paccagnella, S. Sandrin, G. Ghidini, J. Wyss, M. Lavale, and O. Flament "Low Field Leakage Current and Soft Breakdown in Ultra-Thin Gate Oxides After Heavy Ions, Electrons or X-ray Irradiation", RDAECs 99

L. Larcher, A. Paccagnella, M. Ceschia, and G. Ghidini "A Model of Radiation Induced Leakage Current (RILC) in Ultra-Thin Gate Oxides", *IEEE Transactions on Nuclear Science*, to be published



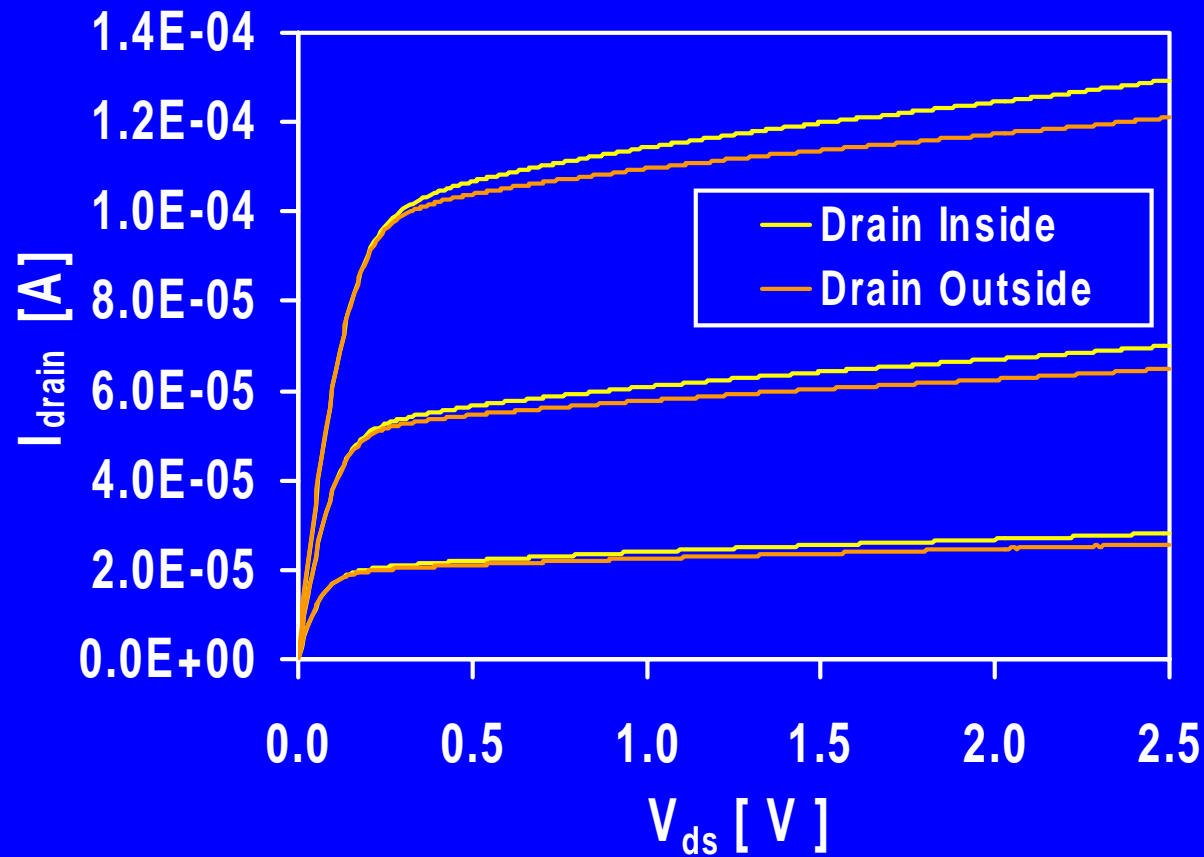
# Radtol DSM: design issues?

- Radtol design rules
  - Minimum  $W/L=5$  of enclosed n-channel
  - Big enclosed n-channel
  - Problem with long n-channel
  - Output conductance asymmetry
  - matching a bit worse for enclosed devices
- Technology
  - $1/f$  noise of short n-channel
  - CMOS switch limitation
  - SEU



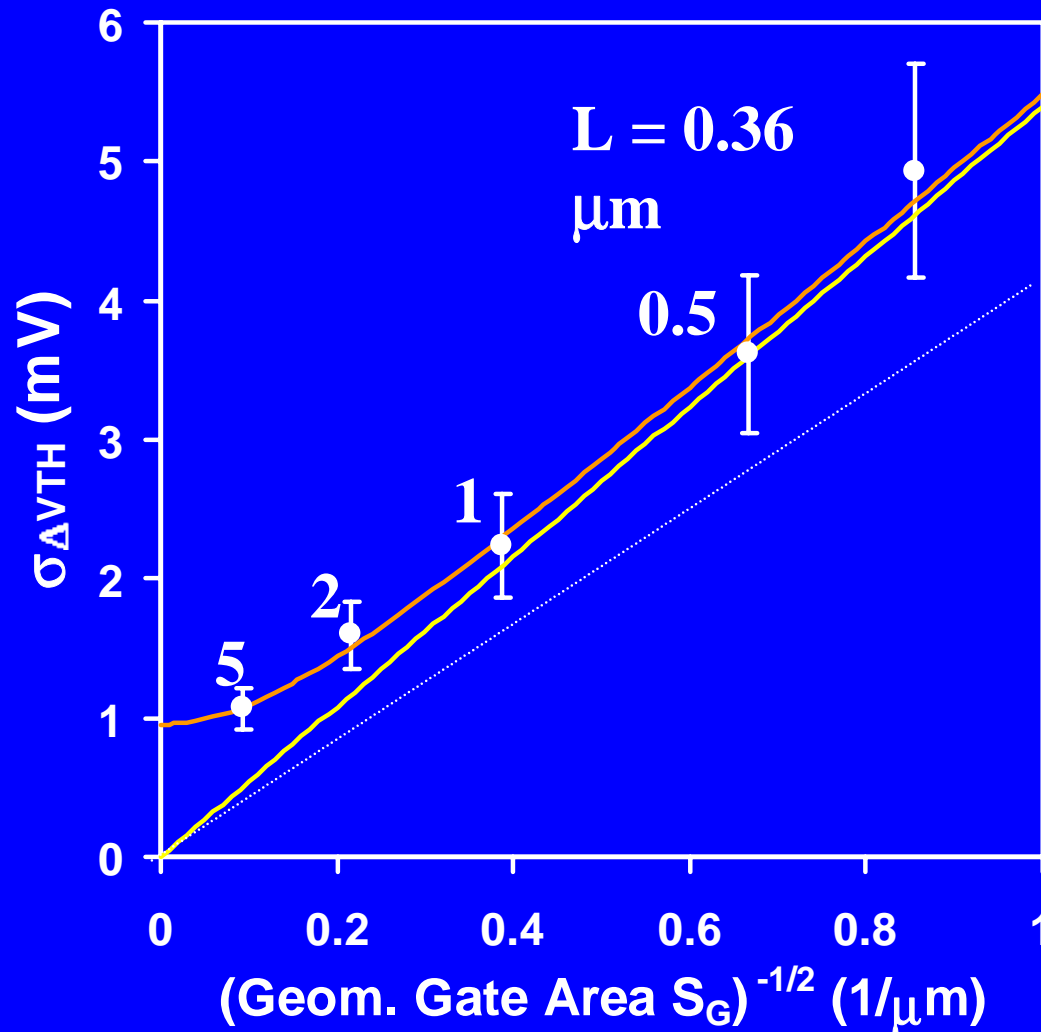
# Output Conductance

$L = 0.28 \mu\text{m}$     $G_{\text{DI}} = 11.9 \mu\text{S}$     $G_{\text{DO}} = 9.6 \mu\text{S}$



$L$ ( $\mu\text{m}$ )	$\Delta G/G_{\text{DI}}$
0.28	19 %
0.36	23 %
0.5	33 %
1	53 %
3	70 %
5	75 %

# Matching of enclosed n-channel



$$\sigma_{\Delta P}^2 = \left( \frac{A_P}{\sqrt{S_G}} \right)^2 + \sigma_0^2$$

$$A_{V_{th}} = 5.4 \text{ mV} \cdot \mu\text{m}$$

$$\sigma_0 V_{th} = 0.95 \text{ mV}$$

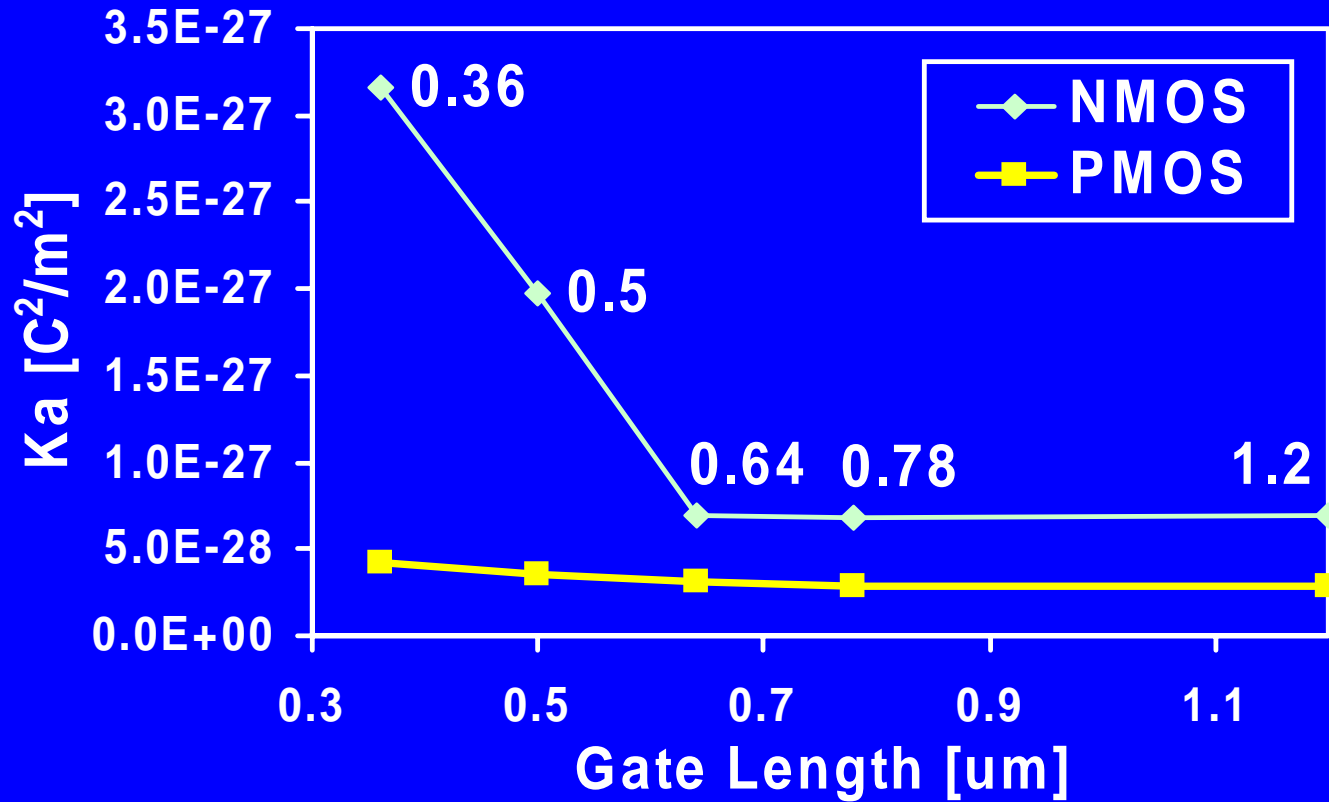
$$A_\beta = 1.5 \% \cdot \mu\text{m}$$

$$\sigma_0 \beta = 0.33 \%$$



# 1/f noise short n-channel

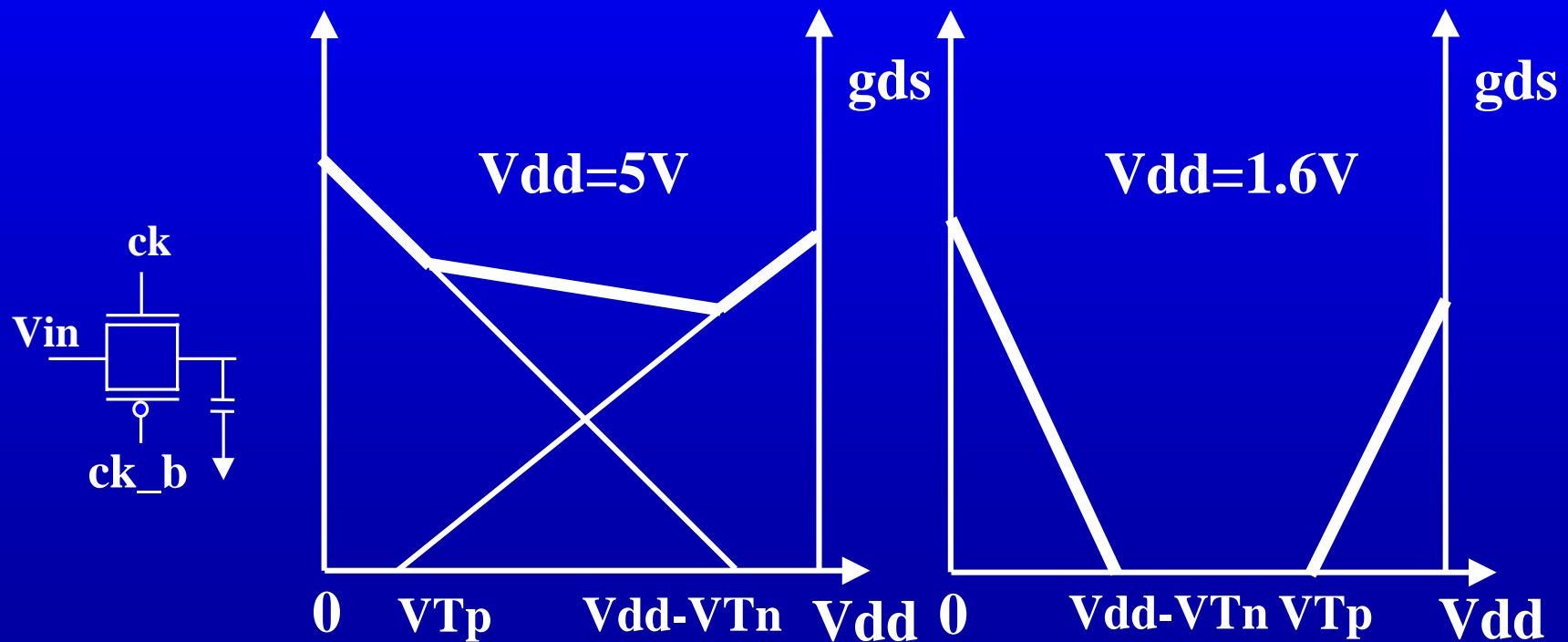
$$S_v = \frac{K_a}{C_{ox}^2 W L f^\alpha}$$



G. Anelli



# SC circuits dynamic range



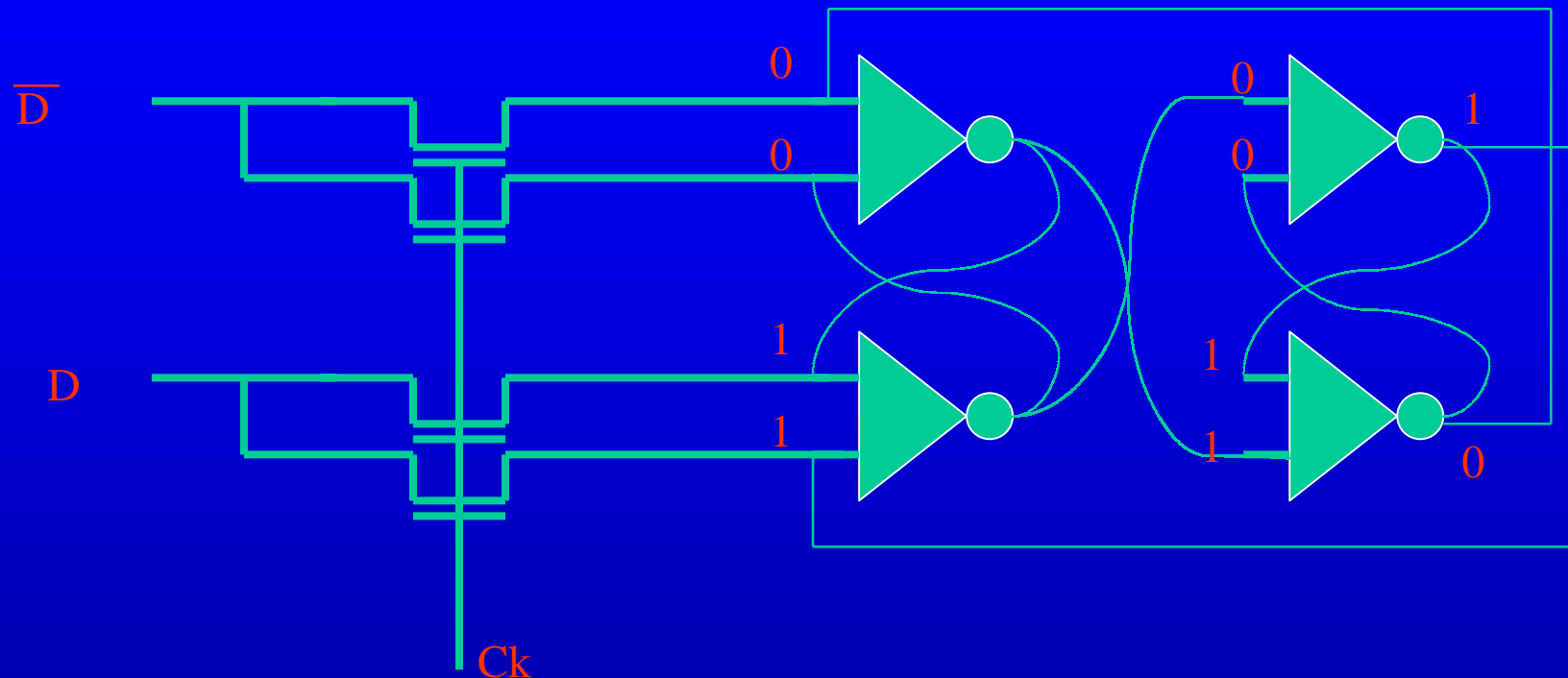
# Summary of SEE for 0.25 radtol circuits RD49

- **SEU test with Heavy ion: see F.Faccio's work**
  - **Static register**
    - oversized design : upset rate **2x lower** than standard
    - C-overloaded design: upset rate **10x lower** than standard
  - **dynamic register**
    - much more susceptible than static register: **factor 300**
- **SEU test with 60 MeV protons**
  - static register no upset observed:  $\sigma < 6 \cdot 10^{-15} \text{ cm}^2$
  - dynamic register upsets observed:  $\sigma = 4 \cdot 10^{-13} \text{ cm}^2$
- **No latch-up for ions of LET=89 MeV cm<sup>2</sup>/mg**
- **Risk of SEGR**
  - no evidence with ALICE 2 test chip up to  $9 \cdot 10^{14} \text{ pr/cm}^2$
  - RILC and RSB gate leakage, no evidence of hard burnout



# SEU mitigation

## DICE memory cell principle



- “2-input” inverter - gates disconnected
- **Writing:** load input FF, close inverters
- **Storage:** input FF biased by second FF
- **SEU:** no memory upset for one node upset

Patented by ST  
Calin et, al.  
NSS Vol43, Dec 96



# SUMMARY

- Rad hard technologies
  - Yield and hardness reasonable for ABCD2T and DTMROC, see yield on pre production
  - more problems with pixel readout chips
  - Issues: design margins and process stability
- Rad tolerant 0.25  $\mu\text{m}$  CMOS
  - radtol approach compatible with all standard deep submicron technologies - present and future
  - impressive hardening level and device density
  - superb results obtained on several circuits
  - attractive for new development of pixel readout chips

