Pixel2000, Genova, 5th June 2000

THE CMS PIXEL DETECTOR

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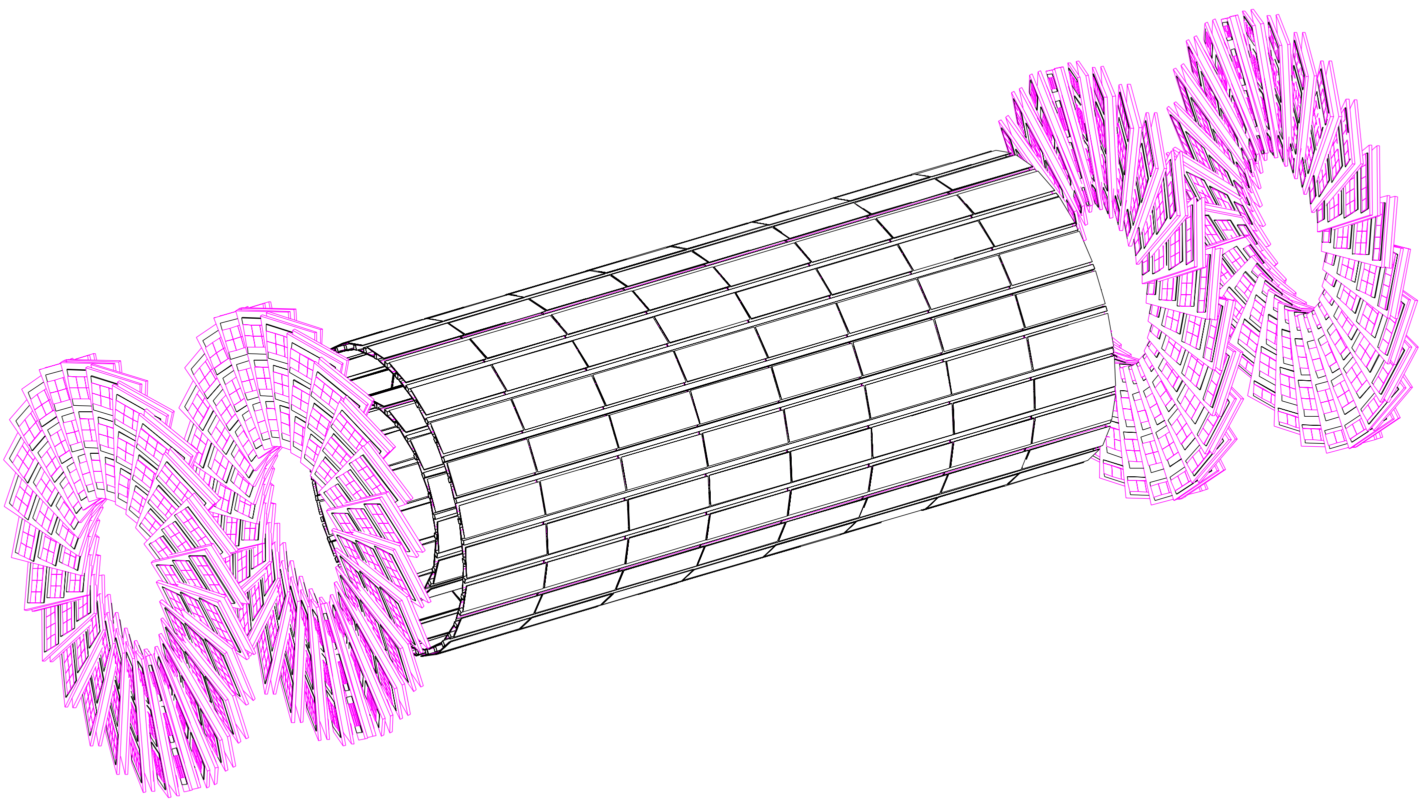
OUTLINE :

- Detector design, mechanics.
- Data rates, readout architecture.
- Simulation of the readout efficiency.
- Sensor development.
- Performance, possible pixel 2nd/3rd level triggers.
- Summary.

CMS PIXEL SYSTEM



- 3D - tracking points
- **σ (z) ~ σ (rφ) ~ 15μm** for precise impact parameter in **rφ & z**

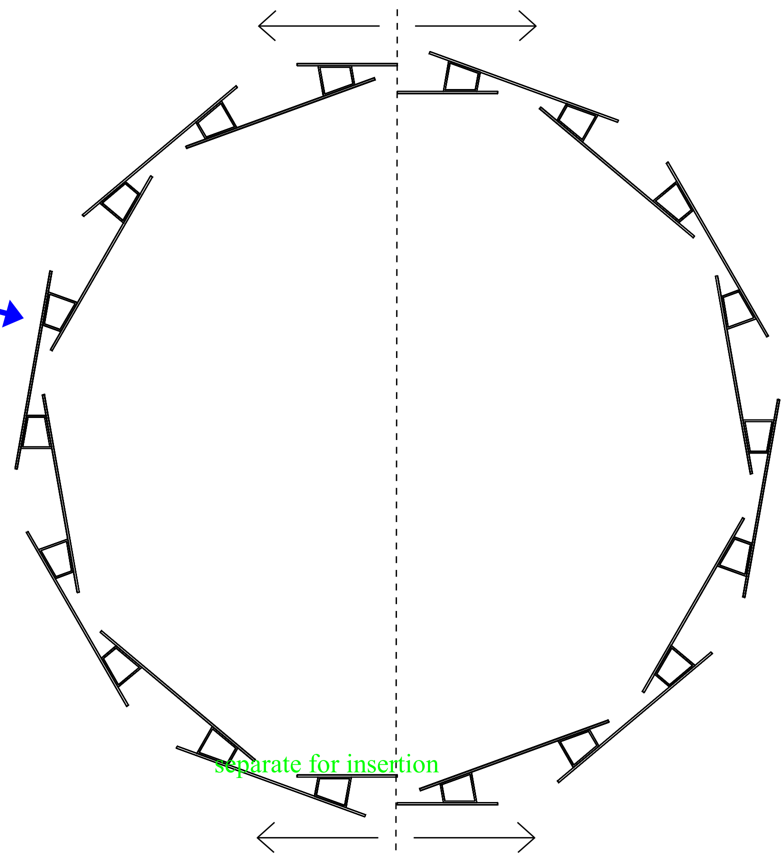
- LAYERS: **r=** 4.3cm 7.2cm 11.0cm

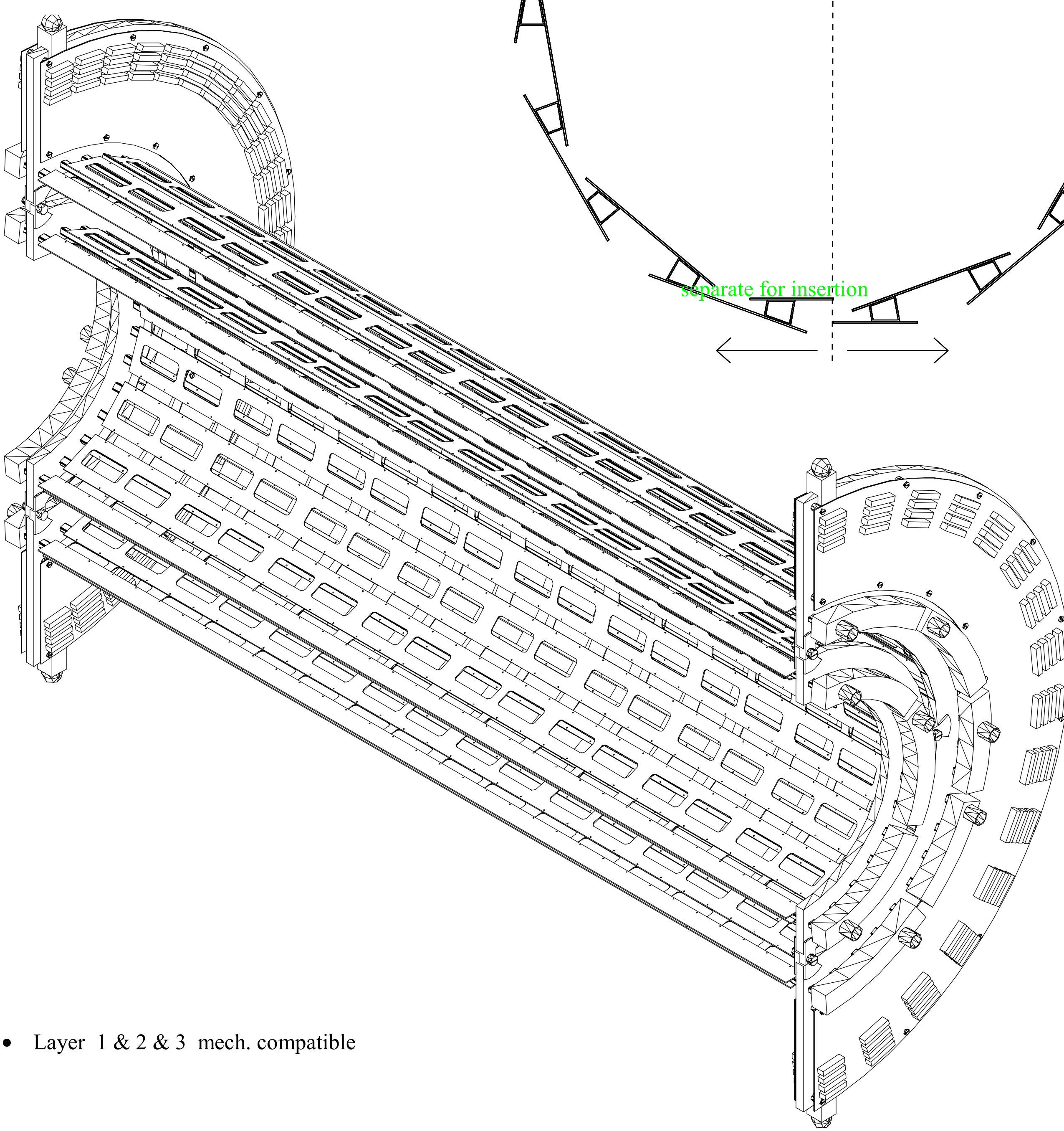
  Low Lumi high Lumi

- replace layers after 6 x 10^{14}/cm^2
- all 3 layers compatible

CMS PIXEL BARREL

Mech. & Cooling
0.6% X_0

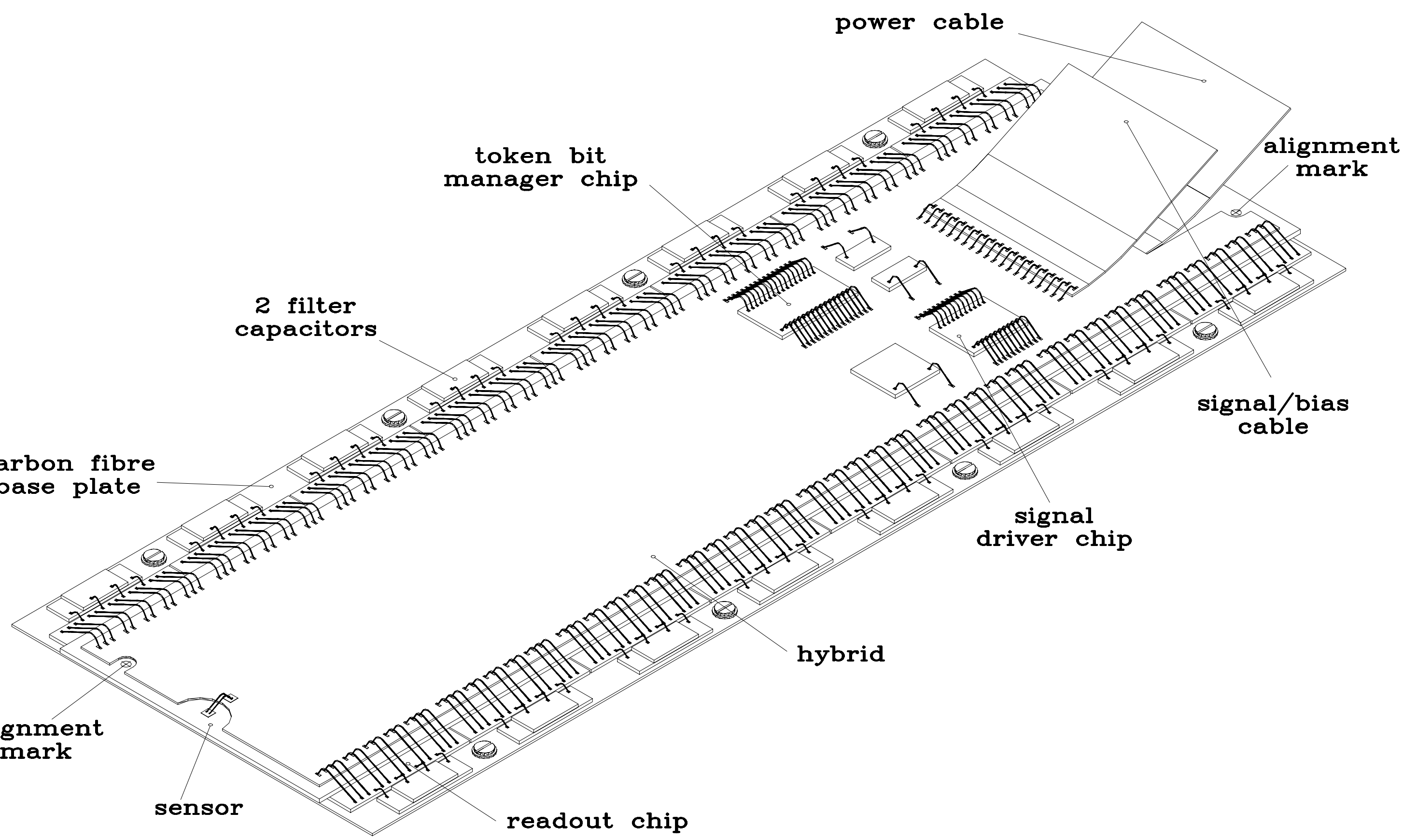


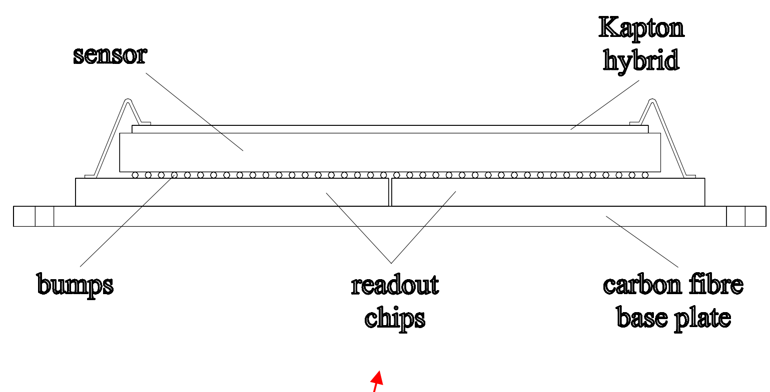


- Layer 1 & 2 & 3 mech. compatible

BARREL PIXEL MODULE

- Silicon sensor **16 x 64mm^2**, **250 µm** thick, **150µm** square pixels
- 16 Readout chips (52 x 53 pixel) ---> ~**44k** pixel ---> 2.4 Watt
- ~ **1 %** X_O





butting chips !

BARREL & FORWARD PIXEL

Table 1: Parameters of CMS Pixel Barrel

	Configuration	**Radius [mm]**	**Faces (∗)**	**full/half Modules**	**Chips**	**Pixels**	**Area [m^2]**
Layer 1	low lumi	41 - 45	18	128/32	2304	6.35×10^6	0.15
Layer 2	low & high lumi	70 - 74	30	224/32	3840	10.6×10^6	0.25
Layer 3	high lumi	107 - 112	46	352/32	5888	16.2×10^6	0.38

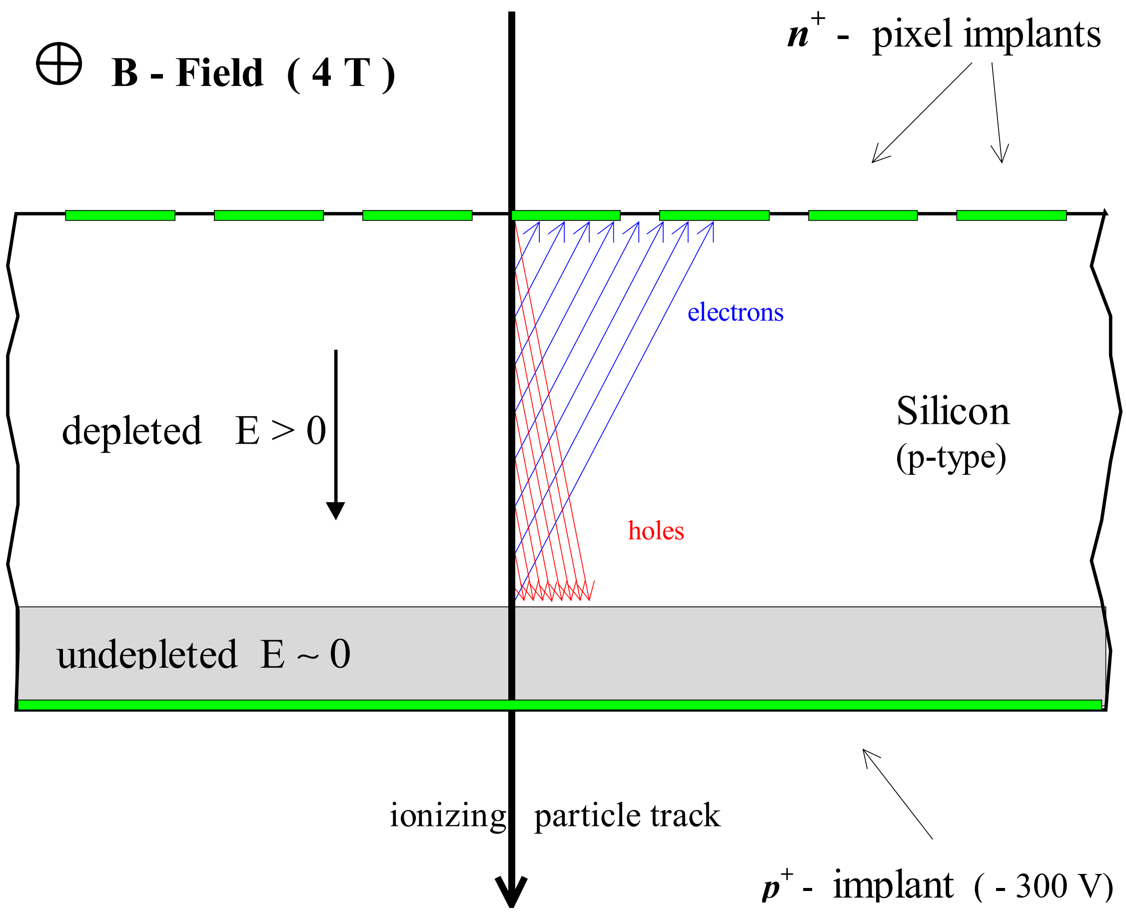
(∗) Two half faces are counted as one face

Table 2: Parameters of CMS Pixel End Disks

z cm	Radius mm	Blades	Sensor Modules	Chips	Pixels	Area m^2
± 32.5	60 - 150	24	7	1080	3.0×10^6	0.07
± 46.5	60 - 150	24	7	1080	3.0×10^6	0.07

CMS PIXEL SENSOR

- Charge sharing by Lorentz effect ---> position interpolation
- n^+- pixel on n-silicon (initial)
- Operate partial depleted up to 6 x $10^{14}/cm^2$



- natural rφ - pixel size ~ **150 µm**
- position interpolation by analog readout ---> **σ (rφ) ~ 10µm**
- need ~ 20000 μm^2 pixel area for pixel circuit (#transistors)
- defines z- pixel size ~ **150 µm** ---> good **σ (z) ~ 17µm**

PIXEL DATA RATES

LHC high luminosity

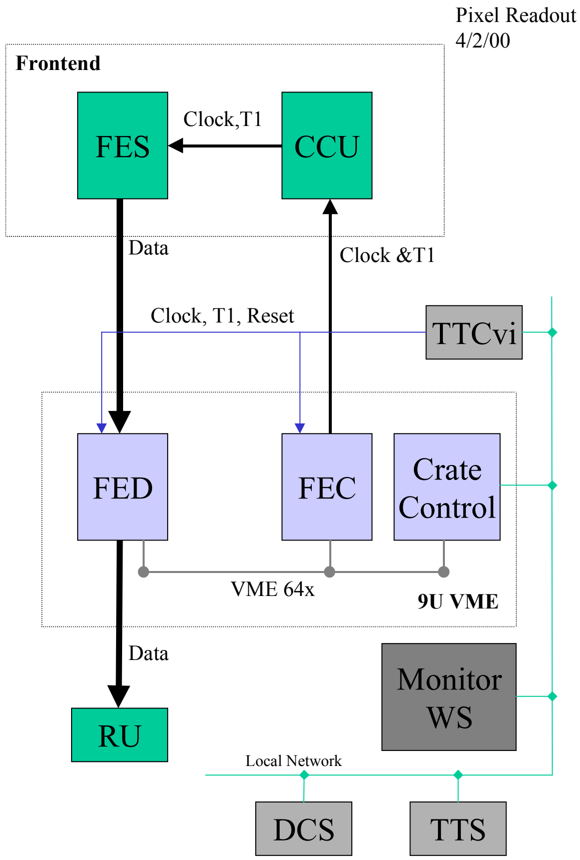
1. **Tracks :**
   800 ($\eta \leq 2$), ≤ 100 ($p_T > 1$ GeV).

2. **Pixels :**
   4.6 + 3.3 + 2.5 + 1. + 1. = 13 k pixels/event;
   e.g. @ 7 cm
   occupancy $\approx 3.3 \times 10^{-4}$;
   pixels/module $\approx$ 15 (1 from noise);
   pixels/ROC $\approx$ 1;
   single pixel rate $\approx$ 10 kHz.

3. **Data volume :**
   13 k pixels * 3 Bytes $\approx$ 39 kB/event;
   13 k pixels * 100 kHz $\approx$ 1.3 G pixels/s
   * 3(10) Bytes $\approx$ 3.9(13) GB/s

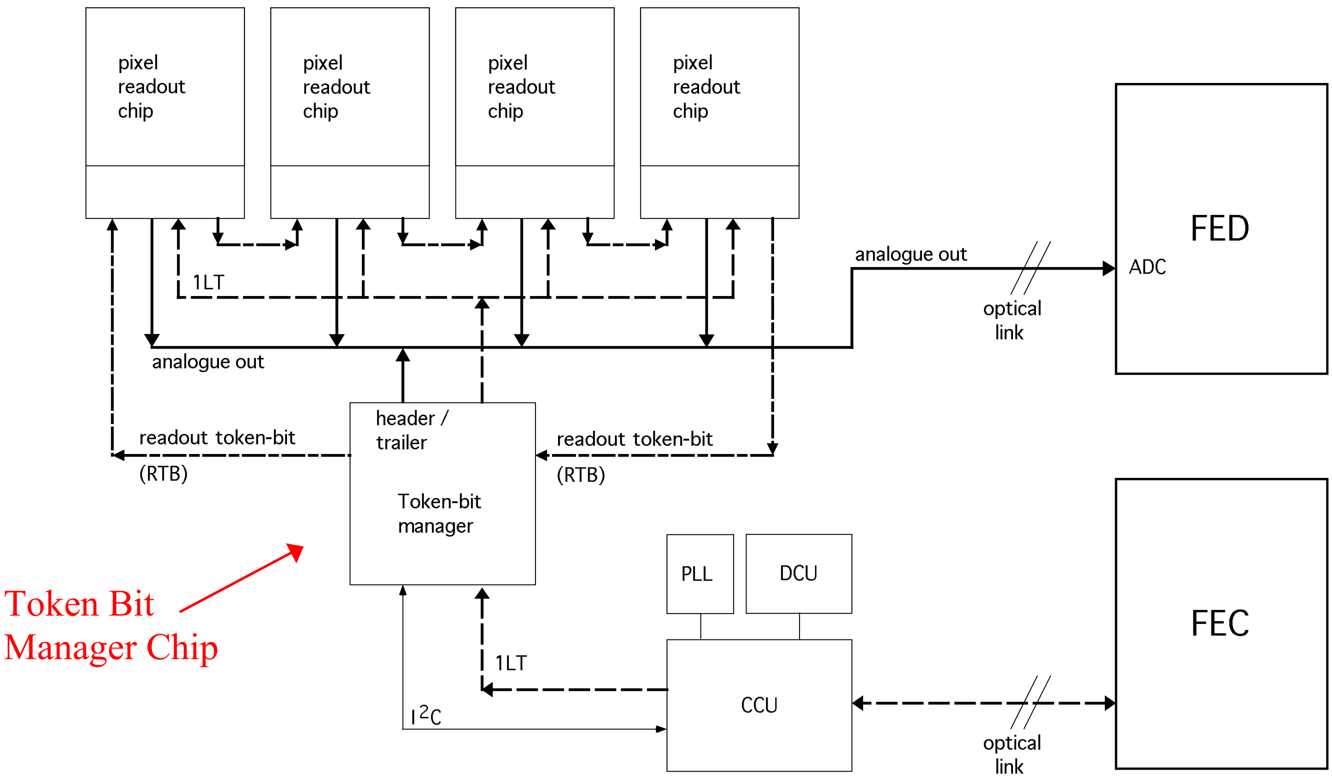
4. **Double column**
   occupancy $\approx$ 1.5% ;
   0.6 MHz column rate;
   2 pixels/column.

5. **Optical readout links** $\approx$ 3000.



Pixel Readout
4/2/00
Frontend
FES
Clock,T1
CCU
Data
Clock &T1
Clock, T1, Reset
TTCvi
FED
FEC
Crate Control
VME 64x
9U VME
Data
Monitor WS
RU
Local Network
DCS
TTS

READOUT OF TRIGGERED DATA



- Zero-suppression ----> data dependent readout time

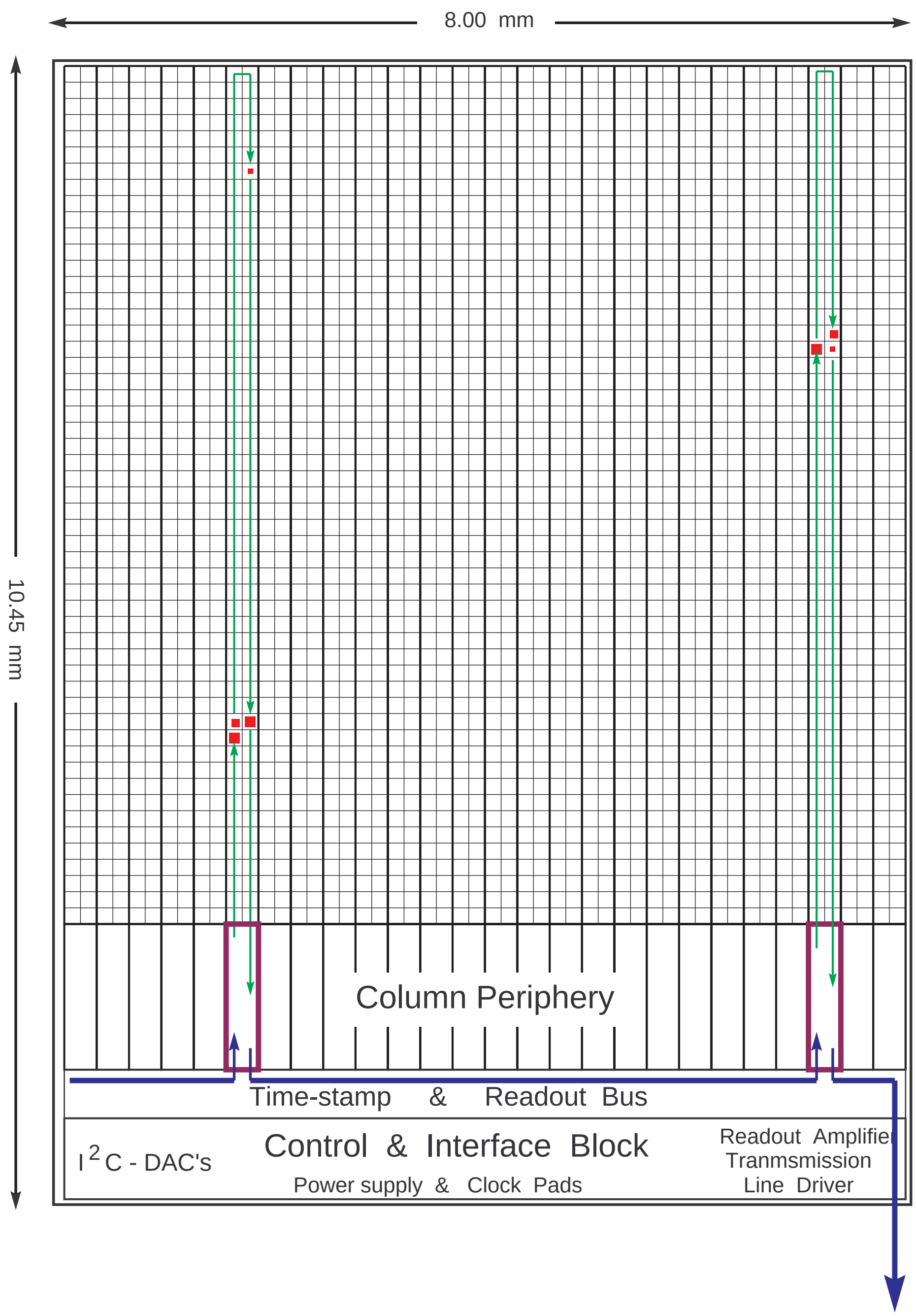
Readout Time

Radius /cm/	4	7	11
ROCs/link	8	16	16
<pixels>/link	16±11	15±9	8±6
<readout-time> /µs/	4	5	4
max. time /µs/	14	13	10
<wait-time> /µs/	1.4	2.4	1.1

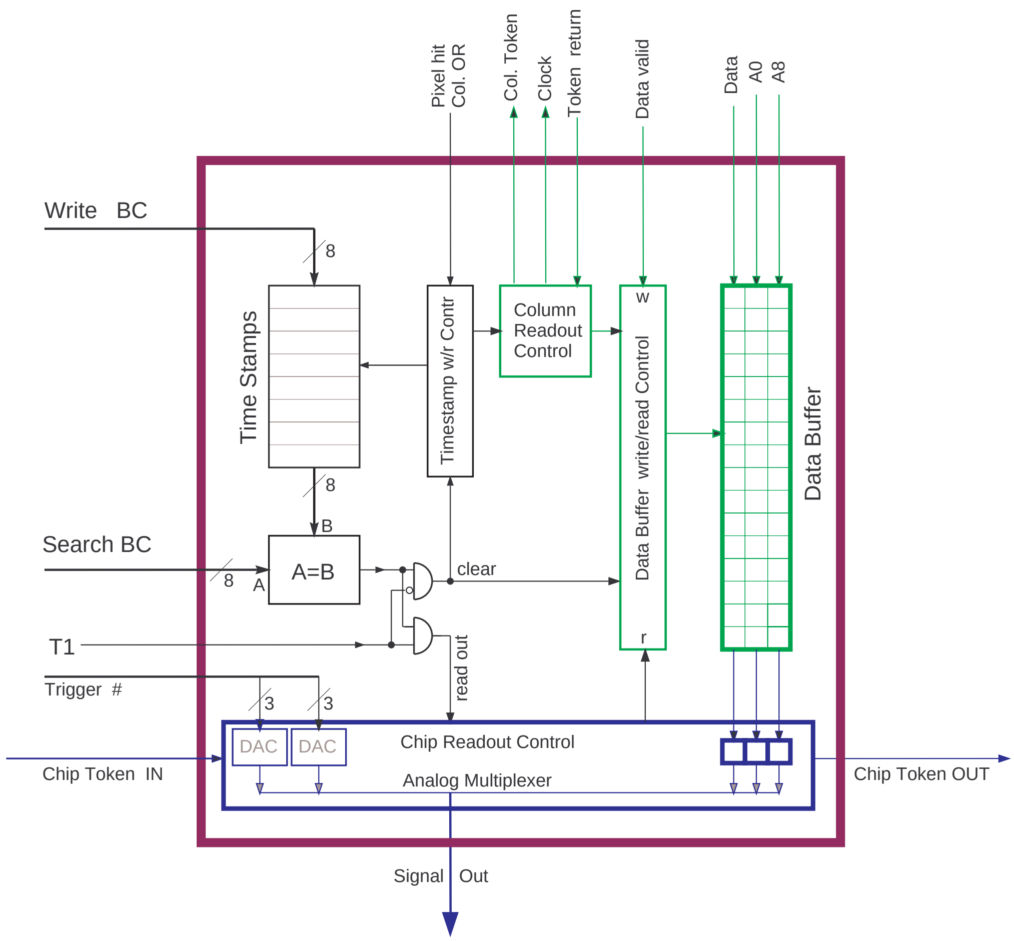
(High luminosity, 40MHz link, 100kHz L1T rate)

PIXEL READOUT CHIP

Data flow of pixel hits in **Column Drain Architecture**

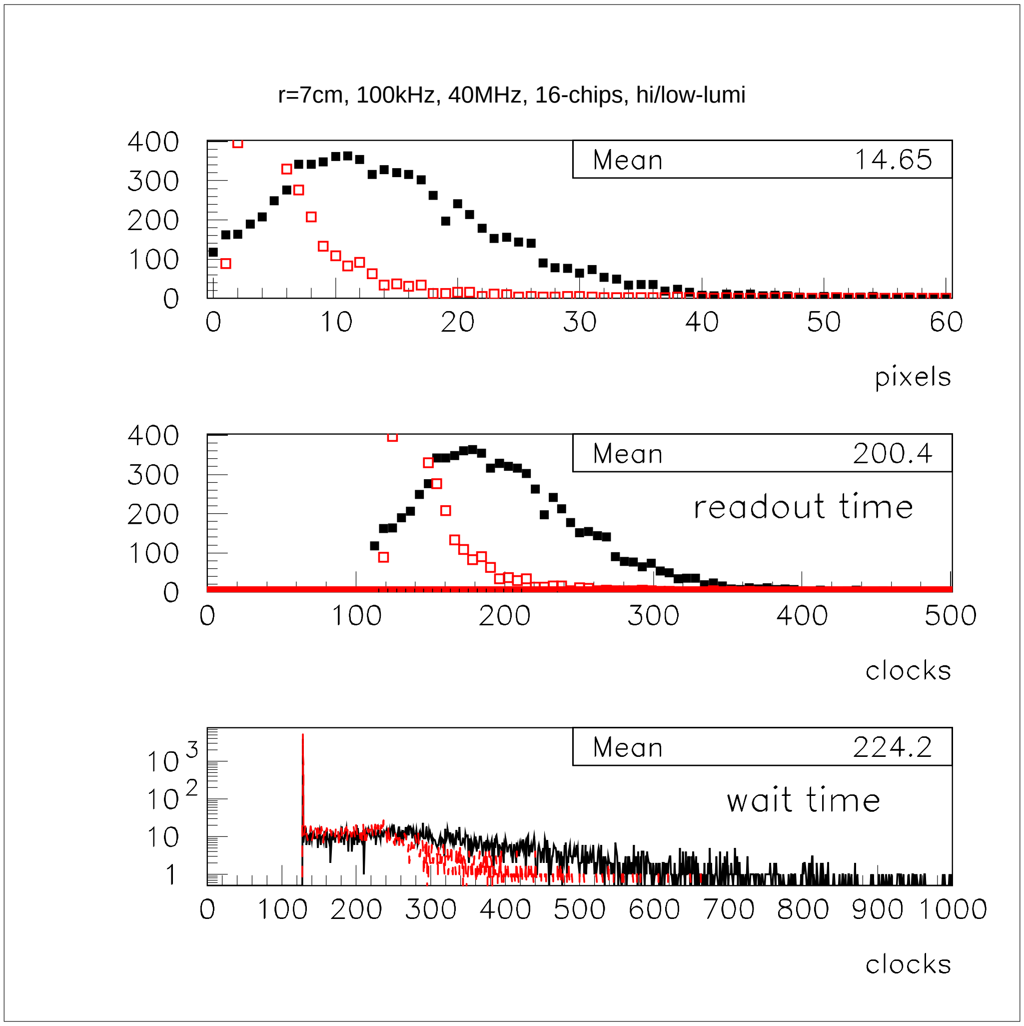


COLUMN PERIPHERY



- Dual-ported hit buffer (Column Drain <--> Chip Readout)
- Time-stamp verification with T1 trigger
- Data formatting and readout of T1-verified hits with analog coded pixel address header
- Prototype circuit : DM_PSI35 (DMILL) Dec. 98

READOUT TIME

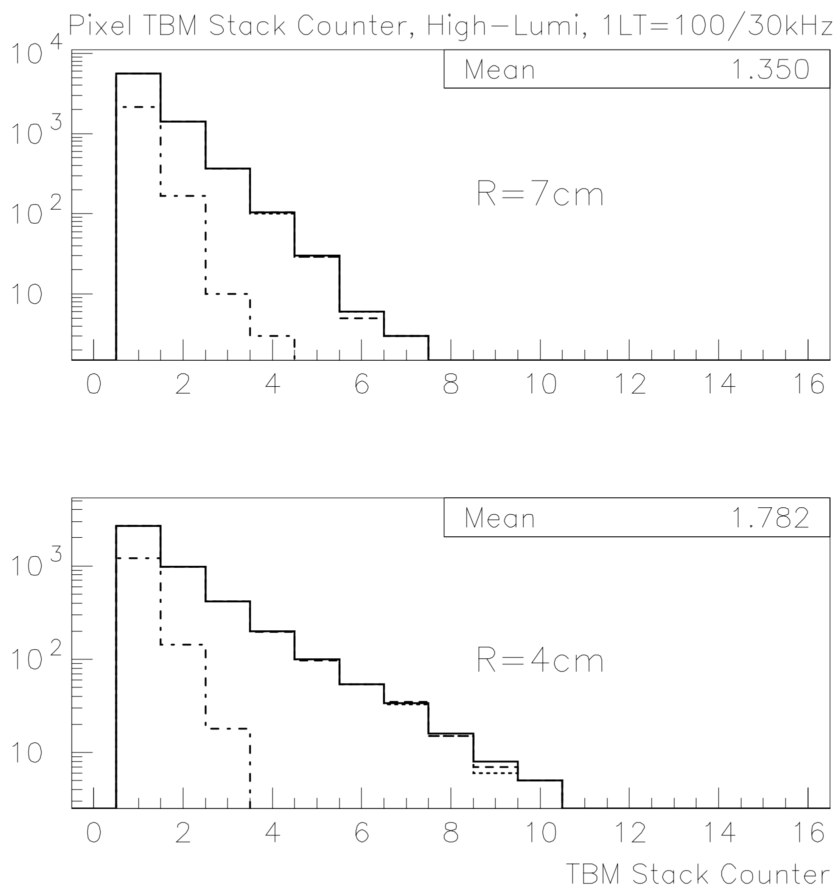


Number of pixels per data packet and the packet readout time for the 7cm pixel layer at high and low LHC luminosities.
Number of ROCs/link = 16, link speed = 40MHz,
L1T rate = 100kHz.

TBM Chip Stack Counter

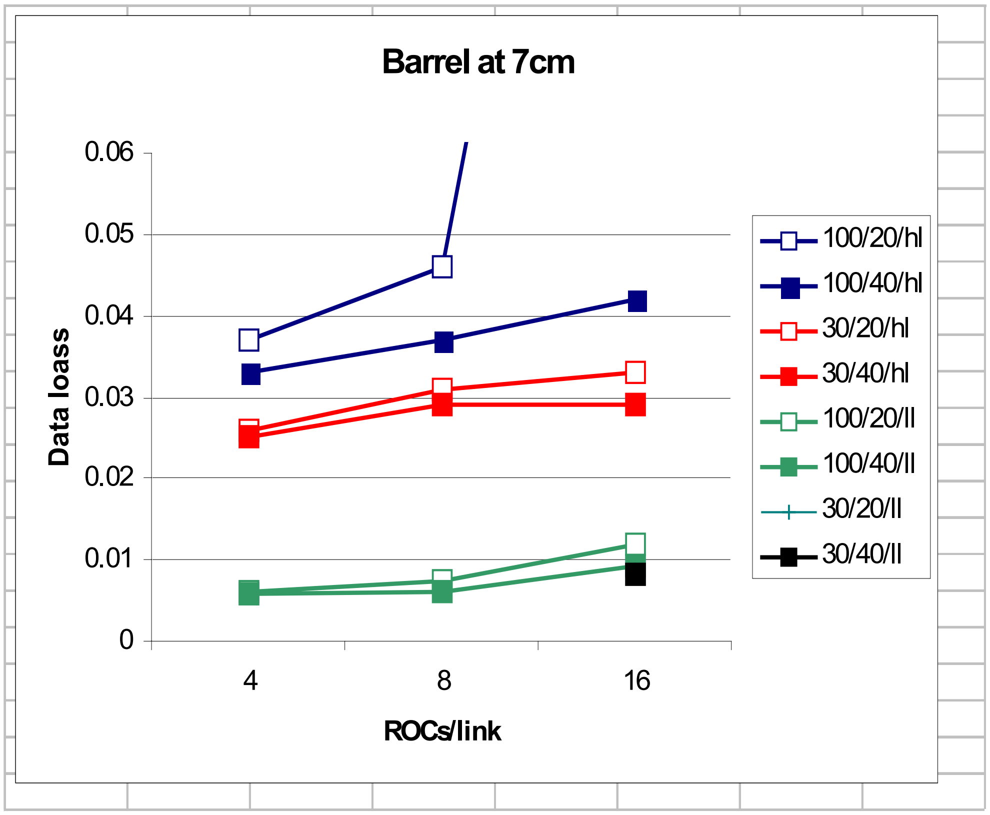
The Token-Bit-Manager (TBM) chip has to queue the incoming 1st level triggers.

Trigger stack for the pixel barrel at 4cm and 7cm, LHC high luminosity:



The TBM stack counter occupancy. The solid line is for 100kHz 1LT rate, the dashed line is for 30kHz.

Data loss for the pixel barrel at 7 cm



BLUE : high-lumi, 1LT 100kHz, 40/20MHz link.

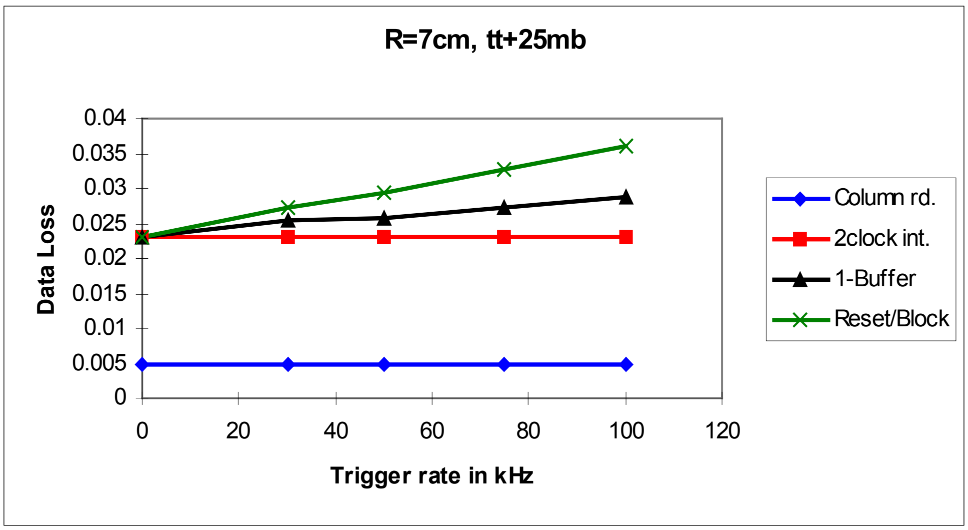
RED : high-lumi, 1LT 30kHz, 40/20MHz link.

GREEN : low-lumi, 1LT 100kHz, 40/20MHz.

BLACK : low-lumi, 1LT 30kHz, 40/20MHz.

READOUT DATA LOSS

Pixel Barrel Layer at 7cm, full LHC luminosity



Sources of data loss :

1. Column readout losses e.g. pixels overwritten, column busy, time-stamp and data buffers full.
2. Readout data buffer overflow, a column can store only one 1LT trigger confirmed time stamp.
3. After readout the column is reset, all time stamps are lost.
4. Dead time of 1 clock (25ns) to setup the column readout mechanism after this column was hit.

SEONSOR DEVELOPMENT

Status at the time of the CMS Tracker TDR :

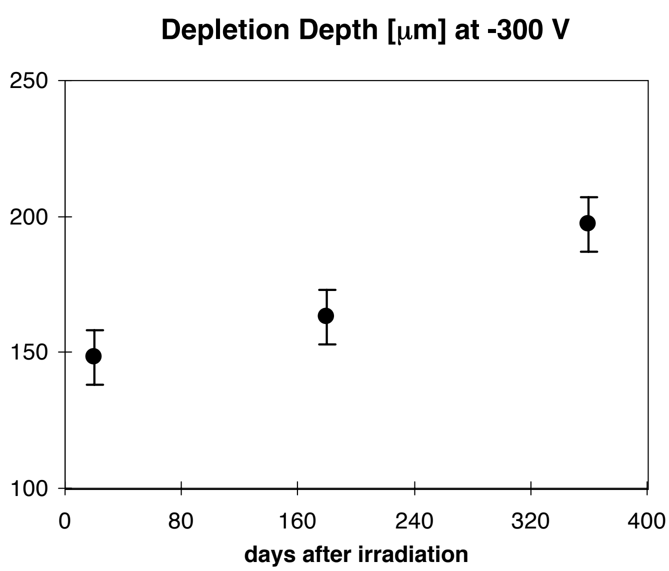
- Si sensors irradiated up to $6 * 10^{14}$ pion/cm^2 ,
- After some annealing time (~1 year) can be depleted to 200 μm at -300V bias voltage (14 ke signal).

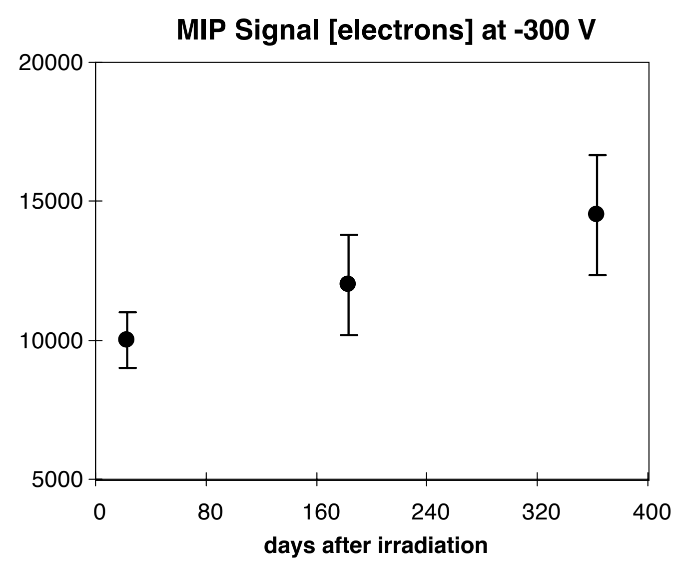
Recent progress, future plans :

- Test new sensors received from CSEM and SINTEF, low and high resistivity wafers, standard and oxygen enriched.
- Variations in:
  p-stop rings, n implant size, # of p-stop rings, guard-rings, ….
- Irradiation (April 2000 at CERN).
- Beam tests with bump-bonded detectors (fall 2000), overall optimization program.
- Summer-Fall 2001 selection of the final design.

SILICON SENSOR PERFORMANCE

after $6 \times 10^{14}/cm^2$ 300 MeV/c pions at PSI





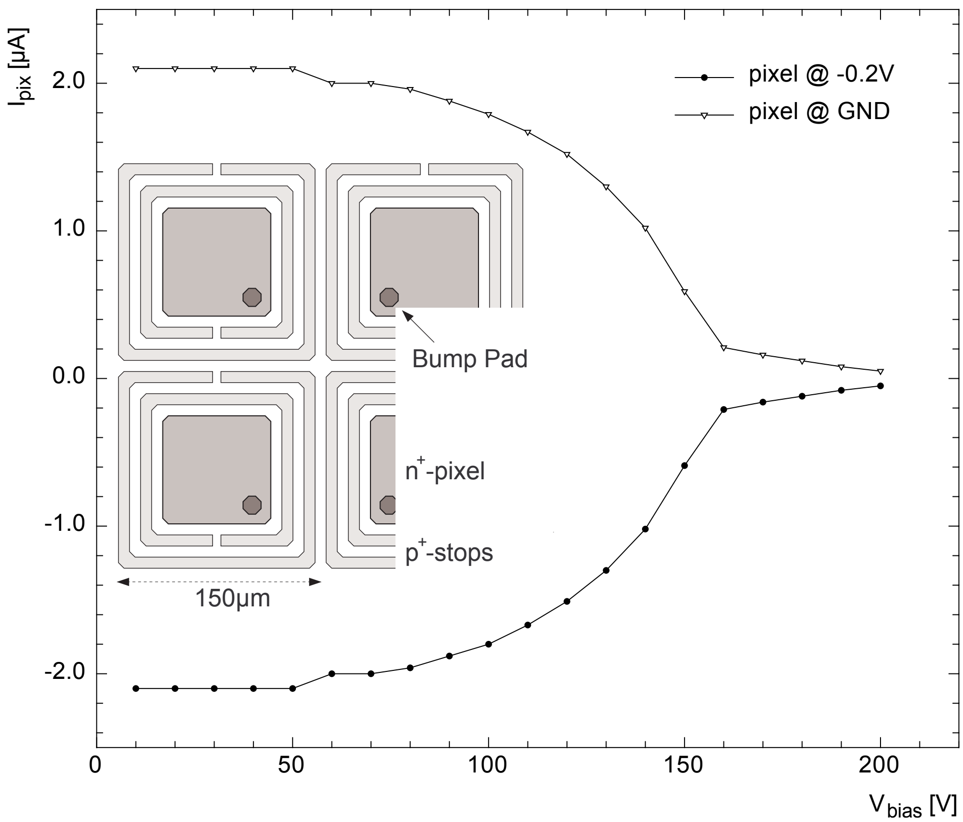
- expect at least **14000** electrons signal up to $6 \times 10^{14}/cm^3$
- need **2000 - 3000 e** pixel threshold for analog interpolation

Goal:

- run with **2500 e** pixel threshold
- **5σ** noise threshold ----> noise < **500 e**

also after irradiation !

SENSOR TESTS



Inter-pixel current as a function of bias voltage.

SOME COMMENTS ABOUT THE PERFORMANCE

Despite the somewhat different designs both detectors Atlas and CMS show very similar simulated performance.

→ See the LHC physics yellow report, e.g.
$Bs \rightarrow J/\Psi(\mu\mu)\ \Phi(KK)$

	ATLAS	*CMS*
Events	300000	300000
Time resolution	0.063 fs	0.063 fs
Background	15%	10%

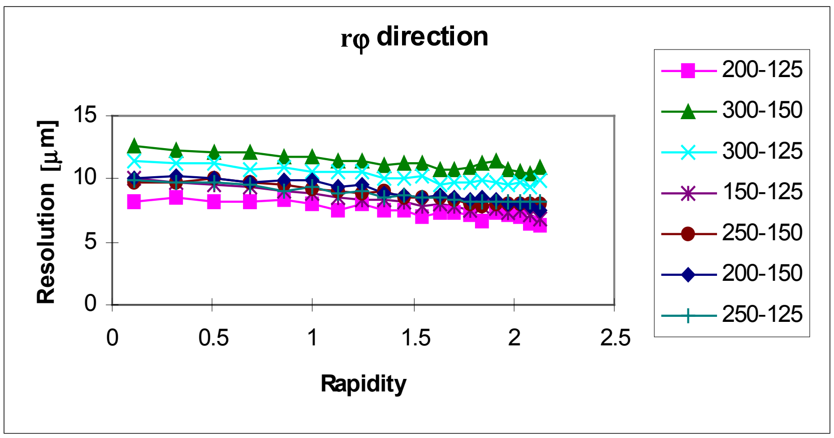
How could the pixel detector be used in triggering?

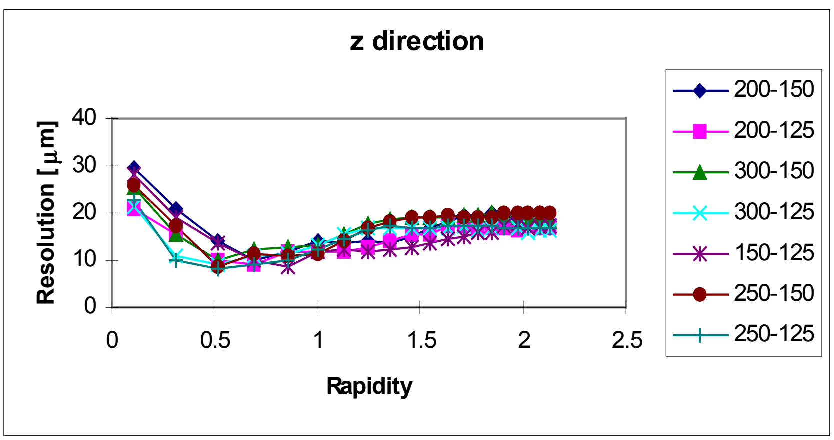
- 3rd level CMS trigger involves full event reconstruction and the pixel detector is fully included;
- Can one do something at the 2nd level with a "standalone" pixel detector information?

PIXEL HIT RESOLUTION

Pixel Barrel Layer at 7cm

Hits from 100 GeV μ tracks.



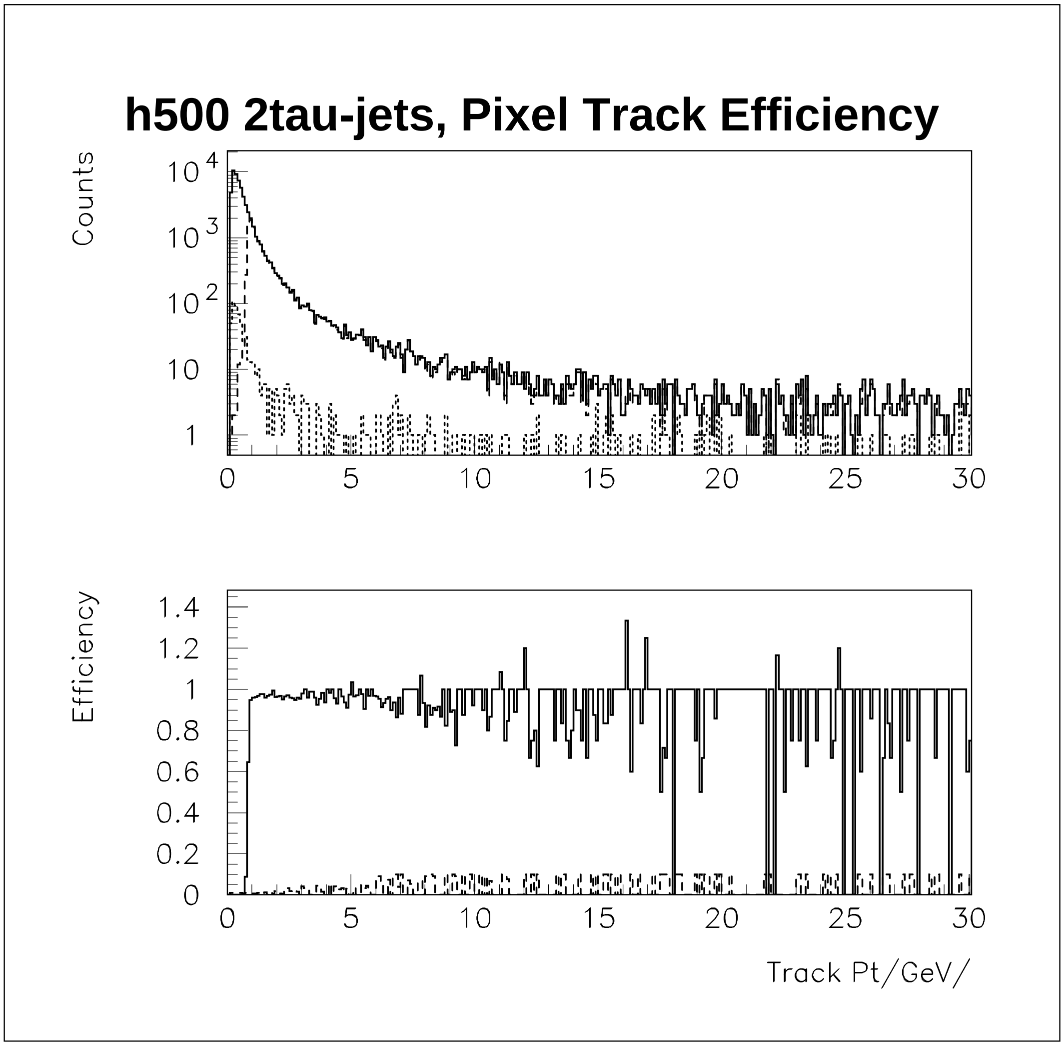


PIXEL HIGH LEVEL TRIGGERS

THE ALGORITHM

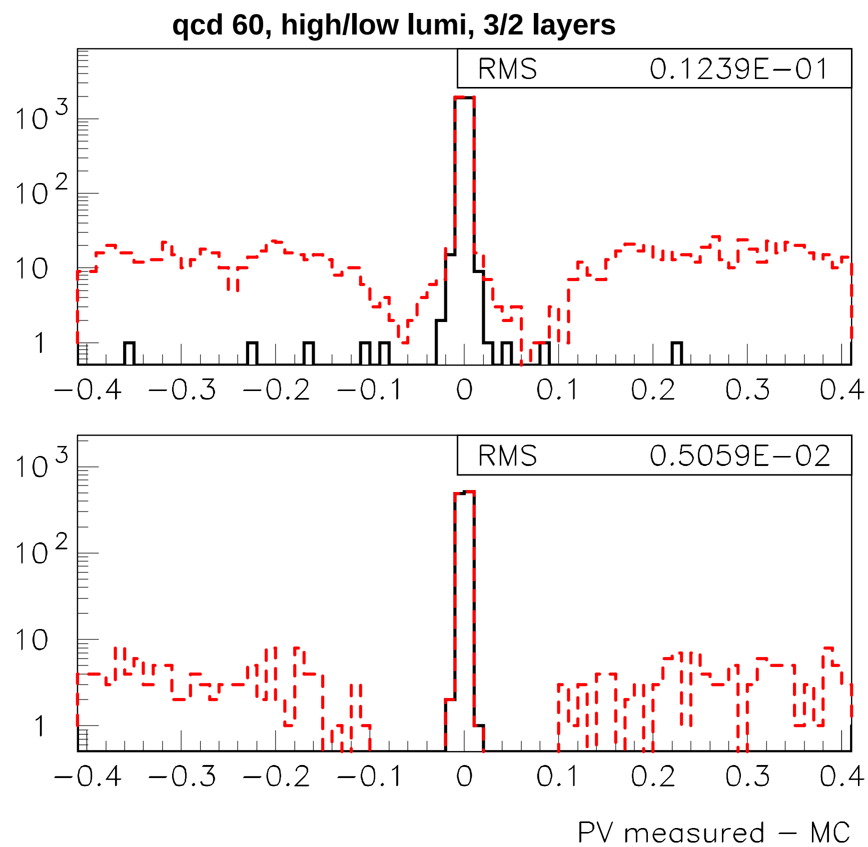
- Correlate hits in two pixel layers which point in φ and z to the interaction region.
- Match hits in φ and z in the 3^{rd} pixel layer.
- Find the PV (histogramming the z impact parameter) and eliminate track candidates which do not point to it.

PIXEL TRACK FINDER



Efficiency for track finding using the 3 pixel layers only.

PV Finding using Pixel Hits



The difference (in cm) between the z position of the Monte Carlo primary vertex and the reconstructed primary vertex. Only pixel hits are used in the vertex reconstruction. The upper plot is for qcd-jet events at high luminosity with the 3 layer pixel barrel. The lower plot is for same events at low luminosity and with a 2 layer pixel barrel. The dashed line shows all found vertices and the solid line is the main "signal" primary vertex as found by the algorithm.

SUMMARY

CMS pixel collaboration :

- **Readout chip :** PSI, RWTH Aachen, ETHZ,
- **Sensors :** PSI, Uni. Zuerich,
  Purdue Uni., Johns Hopkins Uni.,
- **TBM chip :** Rutgers Uni.,
- **Bump bonding :** PSI, ETHZ, UC Davis,
- **Trigger :** PSI, Uni. Basel,
- **Control :** PSI, Uni. Basel, Fremilab,
- **Mechanics, cooling :** PSI, Uni. Zuerich,
  Northwestern Uni., Uni. of Mississippi**,**
- **VME readout :** HEPHY Wien,