FRONT-IND ELECTRONICS FOR PIKEL SENSORS

P.F. Manfredi

Lawrence Berkeley National Laboratory
University of Pavia and INFN Pavia (Italy)
PFManfredi@lbl.gov

THE APPEARANCE OF PIXEL DETECTORS, THAT OPENED UP A BROAD PERSPECTIVE IN TRACKING AND IMAGING APPLICATIONS, HAS SET THE DEMAND FOR MIXED SIGNAL, HIGH DENSITY MONOLITHIC FRONT-END CHIPS TO ACQUIRE AND PROCESS THE INFORMATION FROM THE PIXELS.

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

TO ADOPT A QUITE GENERAL APPROACH TOWARD THE DESIGN OF FRONT-END SYSTEMS FOR PIXELS, IT IS WORTH POINTING OUT THAT SOME BASIC CRITERIA ARE COMMON TO A LARGE VARIETY OF SITUATIONS INVOLVING THE ACQUISITION AND PROCESSING OF SIGNALS FROM A MATRIX OF CHARGE-SENSING ELECTRODES.

IT IS NOT BY CHANCE THAT THE WORD **SENSOR** HAS BEEN PREFERRED IN THE TITLE TO THE WORD **DETECTOR**

THE PIXEL SENSORS CONSIDERED HERE WON'T BE LIMITED TO THE CLASSICAL MATRIX OF DIODES OBTAINED BY DIFFUSING OR IMPLANTING A PATTERN OF A GIVEN TYPE OF DOPING ONTO A SEMICONDUCTOR SUBSTRATE OF OPPOSITE TYPE

THE CONCEPT OF PIXEL SENSOR IS FAR MORE GENERAL.

THE VERY IMPORTANT POINT PIXEL SENSORS HAVE IN COMMON IS THAT THEY ALL BEHAVE, AS FAR AS THE DESIGN OF THE FRONT-END ELECTRONICS GOES, LIKE HIGH DENSITY MATRICES OF CAPACITIVE SIGNAL SOURCES.

THEREFORE, THE FRONT-END ELECTRONICS IS CALLED TO ACT UPON CHARGE INFORMATION

AN INTERESTING EXAMPLE OF A PIXEL SENSOR WHICH IS NOT A <u>SEMICONDUCTOR DETECTOR</u> IS PROVIDED BY A MATRIX OF ELECTRODES DEPOSITED ON AN INSULATING SUBSTRATE TO SENSE THE OUTPUT CHARGE DISTRIBUTION FROM A MICROCHANNEL PLATE (see next viewgraph)

THIS STRUCTURE IS AN EXTREMELY VERSATILE DETECTOR

BY A PROPER CHOICE OF ITS PHOTOCATHODE, IT MAY BE MADE SUITABLE TO DETECT PHOTONS IN A VERY BROAD ENERGY RANGE, FROM INFRARED TO LOW ENERGY X RAYS

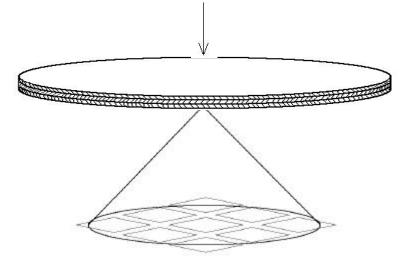


Figure 1.

Position estimation, 5
bit ADC, DNL 0.5 LSB,

100 \(\mu\) pixel pitch

4

2

4

4

4

4

4

-40 -20 0 20 40

Position, \(\mu\)

Figure 2.

Table 1. Specifications for MCP based multiparametric pixel readout

Rate per cm ²	Rate/column	Rate/pixel	Pixel counting losses, %	Unresolved clusters*
$2x10^8/s \text{ cm}^2$	$1x10^{6}/s$	$2x10^{4}/s$	$1x10^{-3}/s$	0.96%
$4x10^8/s \text{ cm}^2$	$2x10^{6}/s$	$4x10^{4}/s$	$2x10^{-3}/s$	1.92%

Minimum pixel size: 100^{μ} Spatial resolution: 25^{μ}

Time resolved application: time resolution β 0.5ns

High event rate applications

Maximum readout rate per column is 10⁷/s

* Cluster recognition in 10ns

A SECOND EXAMPLE OF A PIXEL SENSOR WHICH, AGAIN, IS NOT A SEMICONDUCTOR DETECTOR IS PROVIDED BY A MATRIX OF ELECTRODES DEPOSITED ON AN INSULATING LAYER, EACH ELECTRODE ACTING AS A SECONDARY EMISSION-BASED PHOTON DETECTOR.

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

THE FOLLOWING DESIGN ASPECTS ARE COMMON TO ALL FRONT-END SYSTEMS, REGARDLESS OF THE NATURE OF THE PIXEL SENSORS THEY ARE INTENDED FOR:

- COEXISTENCE OF LOW LEVEL ANALOG SIGNALS AND DIGITAL ACTIVITIES ON THE SAME CHIP which requires the adoption of special layout precautions
- *HIGH CURCUIT DENSITY ON THE CHIP* which results in the two following design constraints:
 - limitation in the area available to the pixel cell
 - limitation in the power allotted to the pixel cell

MOVING NOW TO THE DESIGN OF FRONT-END SYSTEMS FOR SEMICONDUCTOR PIXEL DETECTORS IN TRACKING AND IMAGING APPLICATIONS, MORE CONSTRAINTS ARE TO BE TAKEN INTO ACCOUNT.

RADIATION HARDNESS IS ONE OF THEM

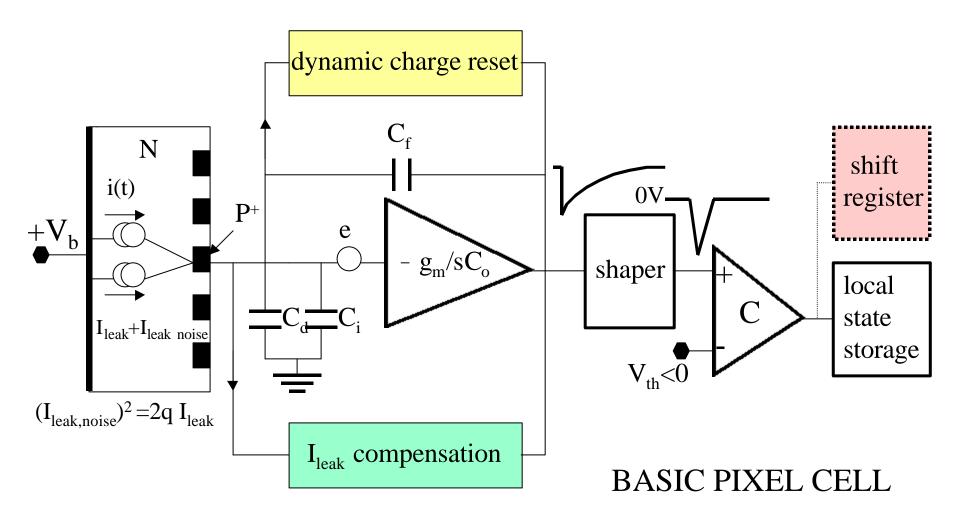
PIXEL DETECTORS EMPLOYED AS TRACKING ELEMENTS IN PARTICLE PHYSICS AT COLLIDING BEAM MACHINES ARE LOCATED CLOSE TO THE INTERACTION POINT AND BECAUSE OF THAT THEY MAY ACCUMULATE DURING THEIR LIFETIME VERY LARGE RADIATION DOSES.

IN A 10 YEAR OPERATION IN LHC EXPERIMENTS THE PIXEL DETECTORS AND ASSOCIATED FRONT-END ELECTRONICS ARE EXPECTED TO ABSORB GAMMA-RAY DOSES OF SEVERAL TENS OF Mrad AND NEUTRON FLUENCES OF UP TO 10¹⁵ cm⁻²

ONE MORE REQUIREMENT TO BE MET IN THE DESIGN OF A FRONT-END SYSTEM FOR A PIXEL DETECTOR OPERATING AT A SYNCHRONOUS MACHINE LIKE LHC IS

A TIME DEFINITION OF THE HIT COMPATIBLE WITH THE INTERBUNCH PERIOD

THAT IS, 25 ns IN THE LHC CASE



P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

THE CRUCIAL POINTS ARE:

- The desired noise behavior must be guaranteed under the constraint of a low power dissipation.
- The target noise behavior must be retained throughout the operational life of the front-end chip, upon absorption of the total doses of radiation specified in viewgraph 11.
- The preamplifier dc stabilizing network must be designed to be able to absorb the detector leakage current, which under the effect of radiation may reach values of up to 100 nA.
- The across-the-chip dispersion in the value of the threshold of comparator C is a very critical aspect

TO ACHIEVE ADEQUATELY SMALL VALUES OF ENC, THE EQUIVALENT NOISE CHARGE, AT THE LOW CURRENT LEVELS ALLOWED IN A PIXEL FRONT-END DESIGN, INPUT DEVICES FEATURING A LARGE TRANSCONDUCTANCE-TO-STANDING CURRENT RATIOS g_m/I_d AND A HIGH TRANSITION FREQUENCY AT LOW CURRENTS ARE AN ESSENTIAL REQUIREMENT.

IN MONOLITHIC PROCESSES THESE REQUIREMENTS ARE MET EITHER BY A BIPOLAR TRANSISTOR OF SMALL EMITTER PERIPHERY OR A SHORT CHANNEL MOSFET

SUBMICRON CMOS PROCESSES LOOK VERY ATTRACTIVE IN THE PIXEL FRONT-END DESIGN, SO THE ATTENTION WILL BE MOSTLY ON THEM. A RADHARD JFET-BICMOS PROCESS LIKE DMILL MAY HOWEVER SUGGEST TO USE IN THE PREAMPLIFIER DESIGN, IF NECESSARY, THE BIPOLAR TRANSISTOR OR JFET.

IN A MOSFET THE SPECTRAL POWER DENSITY OF THE VOLTAGE NOISE (labelled as **e** on page 12) INCLUDES TWO CONTRIBUTIONS:

- THE 1/f NOISE ASSOCIATED WITH THE DRAIN CURRENT
- A FREQUENCY-INDEPENDENT ONE (WHITE NOISE) WHOSE DOMINANT CONTRIBUTION IN AN IDEALLY DESIGNED DEVICE IS THE CHANNEL THERMAL NOISE

$$d\overline{e^2}/df = d\overline{(e_{1/f})^2}/df + d\overline{(e_{f^0})^2}/df$$

THE POWER DENSITY OF THE 1/F NOISE CAN BE EXPRESSED AS:

$$d(e_{1/f})^2/df = N_t q^2 t_{OX}/\alpha C_i f = K_a/C_{ox}^2 W L f = K_f/f$$

WHERE:

N_t is the volumetric trap density in the oxide

 t_{OX} is the gate oxide thickness

q is the electron charge

α is a constant

THE PRODUCT $H_f = C_i K_f = K_a/C_{ox}$ IS THE PROCESS PARAMETER WHICH CHARACTERIZES THE 1/f - NOISE

THE POWER DENSITY OF THE CHANNEL THERMAL NOISE IS INVERSELY PROPORTIONAL TO THE TRANSCONDUCTANCE OF THE DEVICE:

$$d(\overline{e_{f^0 \text{ THER}}})^2/df = 4kTn\gamma/g_m$$

WHERE:

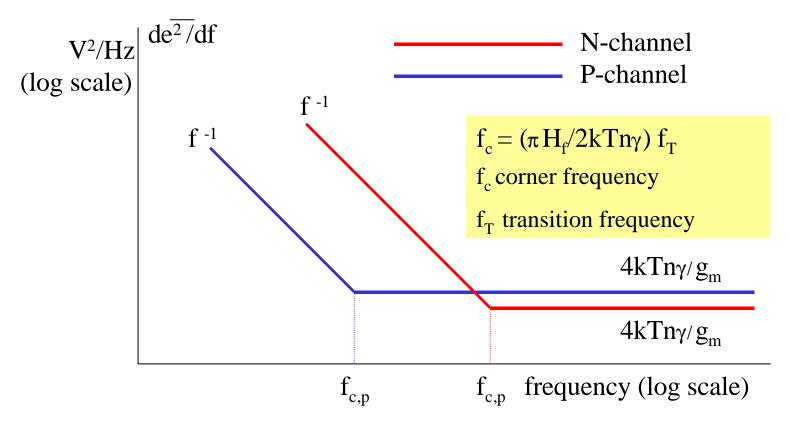
k is Boltzmann's constant

T is the absolute temperature

n is a parameter relevant to the subthreshold charcteristic

 γ is a coefficient which depends on the operating condition (weak, moderate or strong inversion)

THE POWER DENSITY OF THE SERIES NOISE IN MOSFETS HAS THE FREQUENCY DEPENDENCE QUALITATIVELY PLOTTED HERE



Piecewise linear noise representation in MOSFETS

TERMS THAT CONCUR TO INCREASE THE f O BEYOND THE CHANNEL THERMAL NOISE ARE:

- THE THERMAL NOISE DUE TO THE SPREADING RESISTANCES OF GATE AND BULK
- THE IMPACT IONIZATION NOISE

BESIDES, THE GATE COUPLING OF THE CHANNEL THERMAL NOISE IN THE INPUT DEVICE CONTRIBUTES WITH ONE MORE f O DENSITY TERM AT THE PREAMPLIFIER OUTPUT.

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

TWO ASPECTS MAKE THE MORE ADVANCED SUBMICRON AND DEEP SUBMICRON CMOS PROCESSES POTENTIALLY SUPERIOR FROM THE NOISE STANDPOINT TO THE ORDINARY ONES: (*)

- THE DECREASE IN GATE-OXIDE THICKNESS, 10 nm OR LESS, WHICH RESULTS IN A REDUCED 1/f NOISE. MEASURED $H_{\rm f}$ VALUES AROUND 3.5x10⁻²⁶J IN THE PMOS AND 2x10⁻²⁵J IN THE NMOS SUPPORT THIS STATEMENT.
- THE ENHANCED g_m/I_d RATIO RESULTING FROM THE SHRINKING IN THE CHANNEL LENGTH L WHOSE POTENTIAL EFFECT IS A REDUCTION IN THE CHANNEL THERMAL NOISE.

VELOCITY SATURATION, HOT ELECTRON EFFECTS AND A POSSIBLE INCREASE IN 1/f NOISE MAY, HOWEVER, MAKE THE REDUCTION OF L BELOW CERTAIN VALUES USELESS OR EVEN DETRIMENTAL.

^(*) A. Rivetti et al - Analog Design in Deep Submicron CMOS Processes for LHC

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

TAKING INTO ACCOUNT ALSO THE DETECTOR LEAKAGE CURRENT THE FOLLOWING EXPRESSION IS OBTAINED FOR THE SQUARE OF THE EQUIVALENT NOISE CHARGE:

 $ENC^{2} = (A_{1}/t_{p})(4kTng/g_{m})(Cd+Ci+C_{f})^{2} + 2p A_{2}(Cd+Ci+C_{f})^{2} H_{f}/C_{i} + (2qI_{leak} + N_{c})A_{3}t_{p}$

WHERE A_1 AND A_2 , ARE THE SHAPER COEFFICIENTS FOR THE f $^\circ$ AND f $^{-1}$ VOLTAGE NOISE TERMS, A_3 THE SHAPER COEFFICIENT FOR THE PARALLEL NOISE, t_p IS THE PEAKING TIME AND N_c THE PARALLEL NOISE DENSITY DUE TO THE FEEDBACK NETWORKS .

THE APPROACH TO THE CHOICE OF THE INPUT DEVICE SIZE **W** WHICH MINIMIZES ENC, DEPENDS ON HOW STRINGENT IS THE LIMITATION ON THE VALUE OF THE CURRENT IN THE INPUT DEVICE.

IF THE LIMITATION IS SOMEWHAT RELAXED, THE CURRENT DENSITY I_d/W IS FIXED AT A VALUE SUCH TO YIELD AN ADEQUATELY HIGH TRANSITION FREQUENCY f_T . W IS CHOSEN TO MEET THE CAPACITIVE MATCHING CONDITION $C_i = C_d + C_f$. THE RESULTING ENC IS:

 $ENC^2 = 16(A_1/t_p)(kTn\gamma/\omega_T)(C_d + C_f)^2 + 8\pi A_2(Cd + C_f)^2 H_f + (2q I_{leak} + N_c)A_3 t_p$

IF A STRINGENT LIMITATION ON THE DRAIN CURRENT I_d OF THE INPUT DEVICE IS TO BE MET, THE MINIMIZATION OF ENC IS DONE UNDER THE CONSTRAINT OF CONSTANT I_d . THE OPTIMUM W, WHOSE EXACT VALUE DEPENDS ON THE RELATIVE WEIGHT OF 1/f AND f^0 DENSITIES IS SUCH THAT $1/3(C_d+C_f) < C_i < (C_d+C_f)$.

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN

Numerical examples (*):

Assume the following detector and input device parameters before irradiation:

DETECTOR Cd = 250 fF Ileak = 1nA Ci = 100 fF

FE DEVICE N-CHANNEL W=30 μ m L=0.5 μ m t_{ox} = 5.5 nm (Ci = 100fF) I_d = 10 μ A, yielding g_m = 250 μ S

SHAPER: piecewise parabolic weighting function, $t_p = 10 \text{ ns}$

ENC² is built-up from the following contributions (*):

channel thermal noise: 3.9×10^4 (e rms)²

1/f noise: 3.5×10^3 (e rms)²

 I_{leak} : 50 (e rms)²

(*) based on information provided by G.Anelli, F. Faccio, S. Florian, P.Jarron

As a second example, consider the limiting case of a bipolar transistor with an extremely high f_T ENC² simplifies into:

$$ENC^{2} = 2[A_{1}(kT)^{2}(Cd+C_{f})^{2}/qI_{c}t_{p} + qI_{c}t_{p}A_{3}/h_{FE}] + (2qI_{leak}+N_{c})A_{3}t_{p}$$

where h_{FE} is the dc base-to-collector current gain and the terms in square brackets are the noise contribution due to the active element. The first term is the contribution due to the shot noise in the collector current, the second one comes from the shot noise in the base current.

At $I_d = 10\mu A$ and $h_{FE}=100$ the relevant values are: values are:

contribution due to the shot noise in the collector current $1x10^4$ (e rms)²

contribution due to the shot noise in the base current $4.4 \times 10^3 \, (e \, rms)^2$

Comparison between the ENC contributions due only to the active devices gives:

$$ENC_{NMOS} = 200 \text{ e rms}$$
 $ENC_{BIPOLAR\ TRANS} = 120 \text{ e rms}$

DMILL OFFERS ONE MORE INTERESTING ALTERNATIVE TO THE FRONT-END DESIGN, THE P-CHANNEL JFET. DMILL JFETS HAVE BEEN EXHAUSTIVELY TESTED IN LOW NOISE APPLICATIONS (*).

THEY WERE PROVEN TO FEATURE AN OUTSTANDING NOISE BEHAVIOR IN DETECTOR APPLICATIONS ON A BROAD RANGE OF PEAKING TIME VALUES.

HOWEVER, IN THIS SPECIFIC CASE WHERE LOW NOISE CHARACTERISTICS MUST BE ACHIEVED AT VALUES OF t_p IN THE 10 NS REGION, UNDER THE CONSTRAINTS OF STANDING CURRENTS IN THE LOWER 10 μ A REGION AND SMALL AREA, PROBABLY THE DEEP SUBMICRON MOSFETS ARE THE BEST AVENUE TO PURSUE.

(*)P.F.Manfredi et al- Noise Behavior of DMILL JFETs - NIM 409, 336 (1998)

EFFECTS CAUSED BY THE ABSORBED RADIATION

The effects related to the exposure to radiation are a dominant issue in a pixel front-end. They can be classified as (*):

- effects related to the total dose
- effects of the SEL type (single event LATCH-UP)
- effects of the SEU type (single event UPSET)

TOTAL DOSE EFFECTS AFFECT THE FOLLOWING ASPECTS IN THE ANALOG SECTION :

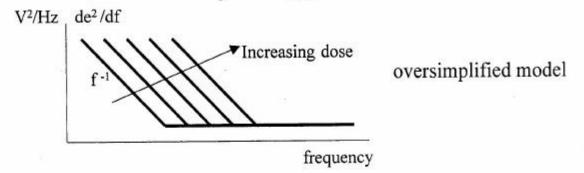
- drift in the operating point of the active devices
- variation in the small signal parameters
- increase in noise
- (*) F. Faccio et al Total Dose and Single Event Effects (SEE) in a 0.25 µm CMOS Technology
- P.F. Manfredi BERKELEY Lab & PAVIA University and INFN

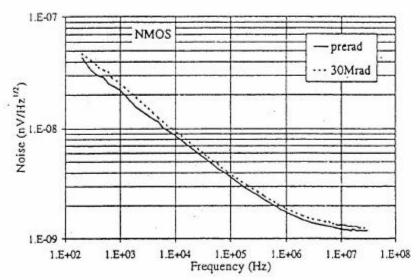
SPECIFICALLY IN MOSFETS THE TOTAL DOSE EFFECTS INDUCED BY IONIZING RADIATION HAVE AS CONSEQUENCES:

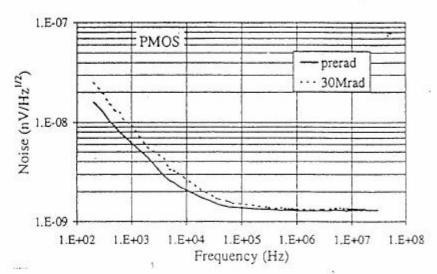
- threshold variations
- variations in the carrier mobility
- increase in noise
- turning-ON of normally OFF N-channel devices

THE THREE EFFECTS ARE RELATED TO THE DEFECTS CREATED BY THE IONIZING RADIATION IN THE GATE OXIDE AND AT THE INTERFACE OXIDE-SILICON. DECREASING THE OXIDE THICKNESS RESULTS IN REDUCED THRESHOLD VARIATIONS AND IN A SMALLER DENSITY OF 1/f NOISE.

THE NEXT VIEWGRAPH COMPARES AN OVERSIMPLIFIED MODEL WHICH EXPLAINS THE NOISE INCREASE IN MOS OF THICKER OXIDE WITH THE ACTUAL BEHAVIOR OF SUBMICRON, THIN OXIDE MOSFETS.







NOISE SPECTRA OF NMOS AND PMOS TRANSISTORS (*)

(*) F. Faccio et al: Total Dose and Single Event Effects (SEE) in a 0.25μm CMOS Technology (1998)

THE REDUCED THICKNESS OF THE GATE OXIDE ALONE DOES NOT REMOVE ALL THE TOTAL DOSE EFFECTS IN A CMOS PROCESS. THE LEKAGE CURRENT PATHS BETWEEN DEVICES AND EFFECTS RELATED TO THE FIELD OXIDE, LIKE THE TURNING ON OF NORMALLY OFF N-CHANNEL MOSFETS ARE STILL PRESENT.

A SOLUTION TO THESE PROBLEMS IS PROVIDED BY ADOPTING ENCLOSED STRUCTURES FOR THE N-CHANNEL MOSFETS AND THE USE OF GUARD RINGS AROUND THEM.

THE INTRODUCTION OF THESE DEVICE LAYOUT TECHNIQUES INTO A DEEP SUBMICRON PROCESS FEATURING AN ULTRA THIN GATE OXIDE HAS LED TO A CMOS TECHNOLOGY OF OUTSTANDING RADIATION TOLERANCE FEATURES (*).

^(*) W. Snoeys et al. Radiation Tolerance beyond 10 Mrad for a pixel readout chip in standard submicron CMOS

JFET BASED MONOLITHIC PREAMPLIFIERS WERE PROVEN TO BE FULLY FUNCTIONAL AFTER EXPOSURE TO 100 Mrad OF GAMMA RAYS AND TO NEUTRON FLUENCES BEYOND 5x10¹⁴ cm⁻².

UPON ABSORPTION OF THE FIRST Mrad OF GAMMA, THE GATE LEAKAGE CURRENT UNDERGOES A SHARP INCREASE, FROM THE pA TO THE nA REGION, WHERE IT LEVELS OFF.

RADIATION AFFECTS MAINLY THE LOW-FREQUENCY REGION OF THE NOISE SPECTRUM.

THE CHANNEL THERMAL NOISE SEEMS TO BE VIRTUALLY UNAFFECTED BY RADIATION, WHICH MEANS THAT AT VALUES OF THE PEAKING TIME FROM A FEW TENS OF ns DOWN, THE JFET IS TO BE CONSIDERED, FROM THE NOISE STANDPOINT HIGHLY RADIATION TOLERANT.

BIPOLAR TECHNOLOGIES HAVE INTRINSICALLY SOME DEGREE OF TOLERANCE TO TOTAL DOSE EFFECTS. EXPOSURE TO RADIATION RESULTS IN A DEGRADATION OF THE $h_{\rm FE}$. THE MAIN IMPLICATION OF THIS EFFECT IS ON NOISE, ALTHOUGH SOME CONSEQUENCES MAY ALSO APPEAR IN THE OPERTAING POINT OF THE ANALOG CIRCUITS.

REDUCTIONS IN THE VALUES OF $h_{\rm FE}$ OF UP A FACTOR 2 HAVE BEEN OBSERVED. THIS RESULTS IN A CONTRIBUTION OF THE PARALLEL NOISE TO THE TOTAL ENC WHICH CAN BE SIZABLE ALSO AT PEAKING TIMES IN THE 10 ns REGION.

FOR INSTANCE, THE BIPOLAR TRANSISTOR OPERATING AT I_c =10 mA WITH h_{FE} =100 BEFORE IRRADIATION, UPON A FACTOR 2 REDUCTION IN ITS h_{FE} AFTER IRRADIATION WOULD CONTRIBUTE TO TOTAL ENC WITH ABOUT100 RMS ELECTRONS ARISING FROM PARALLEL NOISE.

SINGLE EVENT EFFECTS

Single Event Latch-Up (SEL): the charge ,made available by an ionizing event may trigger a parasitic thyristor in a bulk CMOS or bipolar process. It may turn out to be destructive.

Among the radhard technologies DMILL, (where all active devices reside on individual insulating layers) is immune from this problem

Deep submicron processes, with enclosed N-MOS structures and guard rings have also been proven to feature a good degree of immunity from SEL

Single Event Upset (SEU): affects the operation of the digital section and consists in a change of bit or state in a logic circuit. The only way to avoid it is by circuit design techniques.

BOTH SEL AND SEU OCCUR WHEN CERTAIN THRESHOLDS IN THE CHARGE CREATED BY THE IONIZING EVENT ARE EXCEEDED

ONE MORE CRUCIAL DESIGN POINT: THE COMPARATOR

The comparator which appears in the schematic of the basic cell is a crucial circuit. It fulfills a twofold function:

- sets the acceptance threshold to the charge associated with the hit
- defines the hit timing

The two functions may be actually assigned to two different circuits(*).

The threshold dispersion across the chip is a serious issue. Its reduction based on the increase in the areas of the matched devices that constitute the comparator may not comply with the cell area restrictions of the pixel readout.

Solutions based on the correction of the individual comparator offset are in use.

A high charge sensitivity of the linear section helps to reduce the input-referred threshold dispersion.

K. Einsweiler et al. IEEE Transactions on Nuclear Science, 46, 792 (1999)

STRUCTURES OF THE ANALOG SECTION OF A PIXEL FRONT-END

The basic pixel cell described at page 12 detects the hit and attributes it to the pixel where it occurred.

Such a readout system, associated with a histogramming memory becomes the basic unit of a pixel imager.

In some applications, *RETENTION OF THE INFORMATION ON THE CHARGE INDUCED ON THE PIXEL* is required.

The solution based on the Time-over-Threshold approach, for instance, suits this purpose very well (*).

NEW APPLICATION-DRIVEN CONCEPTS ARE NOW ADDRESSING THE DESIGN OF PIXEL READOUT SYSTEMS

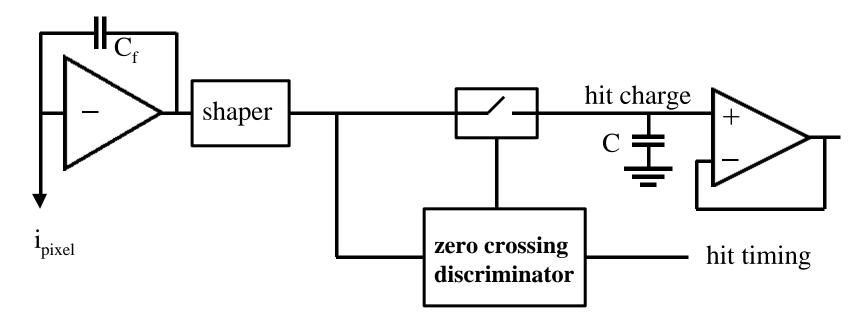
(*) L. Blanquart et al: MAREBO, A Full Radhard Pixel Detector Prototype for ATLAS

THE FUTURE TREND IN THE DESIGN OF PIXEL SYSTEMS WILL BE TOWARD A MULTIPARAMETRIC READOUT APPROACH.

A VERY SIMPLE EXAMPLE IN THIS SENSE IS THE PIXEL CELL WHOSE DESIGN IS PRESENTLY UNDERWAY AT BERKELEY LAB. THE CELL IS INTENDED FOR APPLICATIONS REQUIRING:

- high accuracy position sensing based on charge interpolation to achieve a high spatial resolution
- high accuracy timing, to perform time-resolved or time-correlated imaging

THE BLOCK DIAGRAM OF THE PIXEL CELL IS SHOWN BELOW



the goal in the timing channel is a dispersion of less than 0.5 ns as required in some time-resolved imaging applications

Acknowledgements

The information provided by G. Anelli, L. Blanquart, F. Faccio, W. Snoeys has been instrumental to the preparation of this talk.

Some of the ideas presented have are the rsult of discussions J. Millaud.

The contribution by V.V. Souchkov is also acknowledged

The excellent job done by L. Fabris in reviewing and criticizing this material is gratefully acknowledged

P.F. Manfredi - BERKELEY Lab & PAVIA University and INFN