

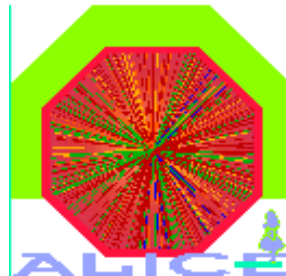
PIXEL2000, June 5-8, 2000

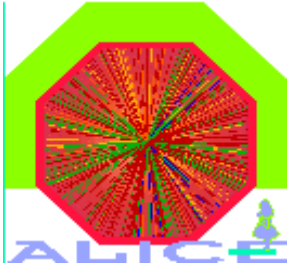
STATUS OF THE ALICE PIXEL DEVELOPMENTS

FRANCO MEDDI

CERN-ALICE / University of Rome & INFN, Italy

For the ALICE Collaboration





CONTENTS:

➡ Introduction:

Physics Requirements

Design Considerations

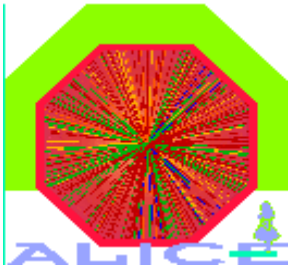
➡ Present development status and related issues:

Front-end chip

Ladder & stave layout

Read-out & control

Global layout



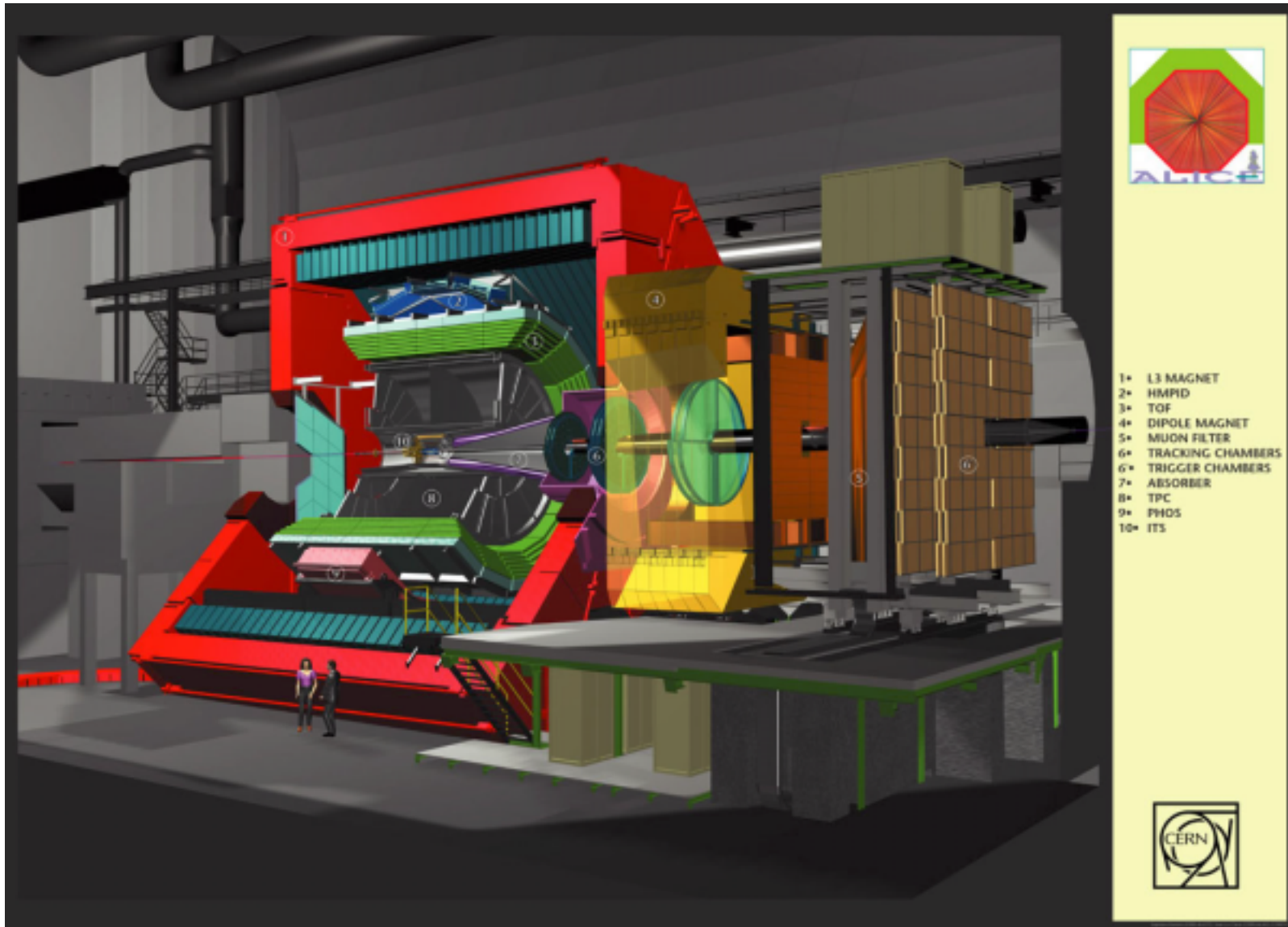
Institutes that will construct and operate the ALICE-ITS-PIXEL

- CERN
- ITALY

Bari (INFN, University and Politecnico)
Catania (INFN and University)
Legnaro (LNL-INFN)
Padova (INFN and University)
Roma (INFN and University)
Salerno (INFN and University)

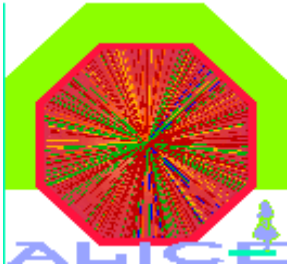
- SLOVAKIA

Kosice (Institute of Experimental Physics,
Slovak Academy of Sciences and
Faculty of Science P.J. Safarik University)



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ALICE SPD AS PART OF CENTRAL TRACKING SYSTEM: REQUIREMENTS

- Determination of **secondary vertices**:

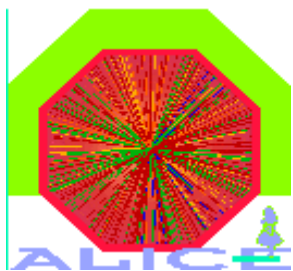
Charm & Beauty decays study

➡ Impact parameter resolution needed $\sigma(r\phi) \sim 50 \mu\text{m}$ @ $p_t \sim 1 \text{ GeV}/c$

- Central Pb-Pb collisions: **High track densities** ($> 50 \text{ cm}^{-2}$)

➡ Need high resolution & high granularity:

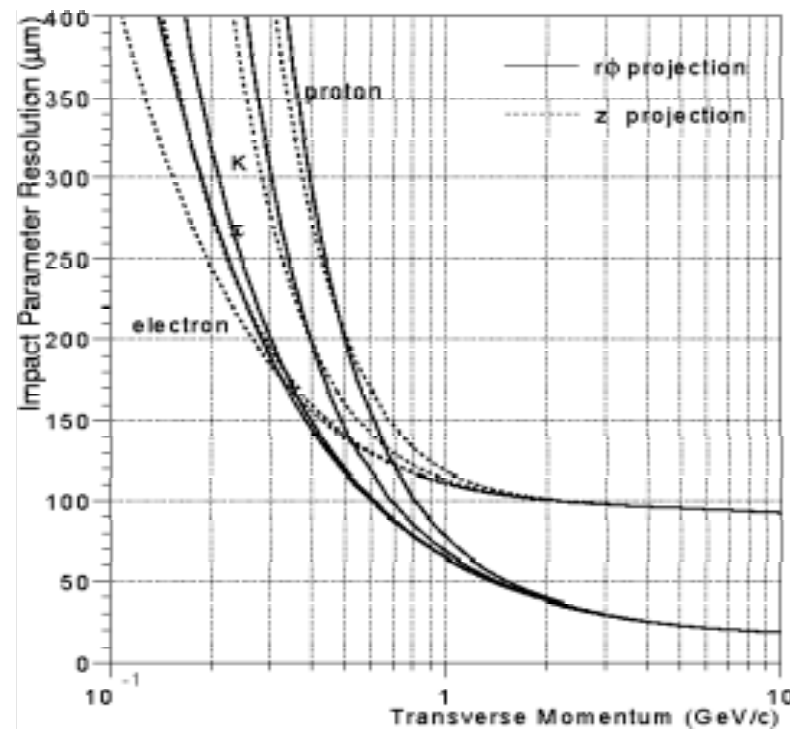
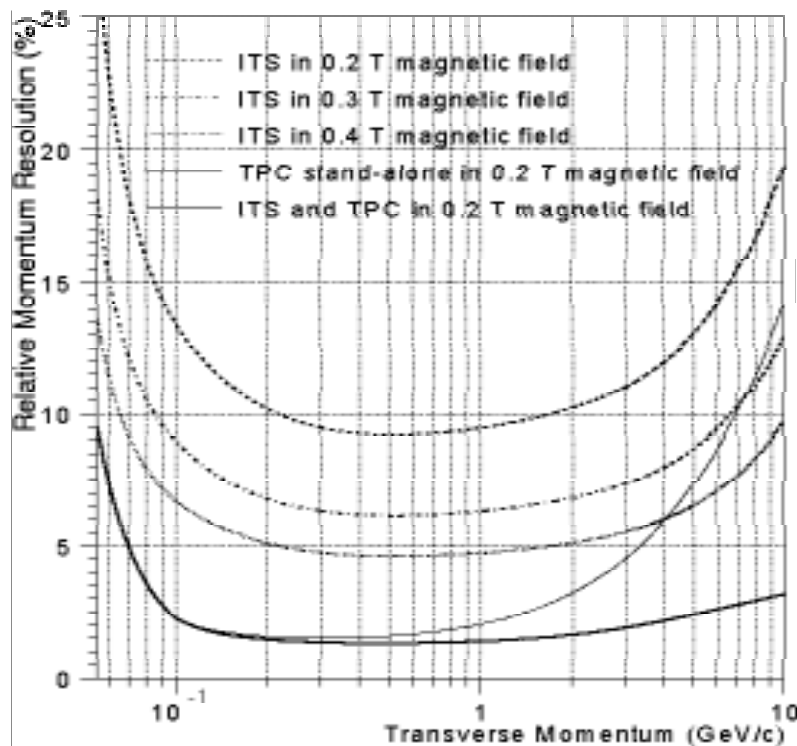
Two SPD Layers at 4 cm & 7 cm from beams
with acceptance of $\pm 45^\circ(\theta)$ [$|\eta| < 0.88$]
for vertices within $\pm 1\sigma$ length of the interaction diamond
SPD with cell size: $50 \mu\text{m}$ ($r\phi$) & $425 \mu\text{m}$ (z)



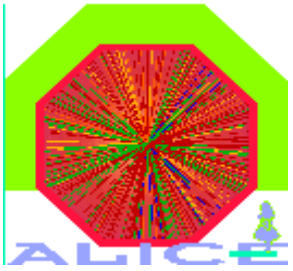
ALICE: WHOLE ITS & TPC SIMULATION

Tracking precision: $12 \mu\text{m}$ ($r\phi$) & $100 \mu\text{m}$ (z)

Two tracks separation: $100 \mu\text{m}$ ($r\phi$) & $850 \mu\text{m}$ (z)



Impact parameter resolution:
 $50 \mu\text{m}$ ($r\phi$) @ $p_t = 1.3 \text{ GeV/c}$



ALICE SPD: PRIMARY VERTEXING

- The determination of **primary vertices** is necessary both for the **dimuon physics** and for **good tracking**:

Vertex position in the vertex diamond

Size of the bunch: $\sigma_x = \sigma_y = 15 \mu\text{m}$ & $\sigma_z = 5.3 \text{cm}$

➡ Primary vertex resolution needed: few $\sim 10 \mu\text{m}$

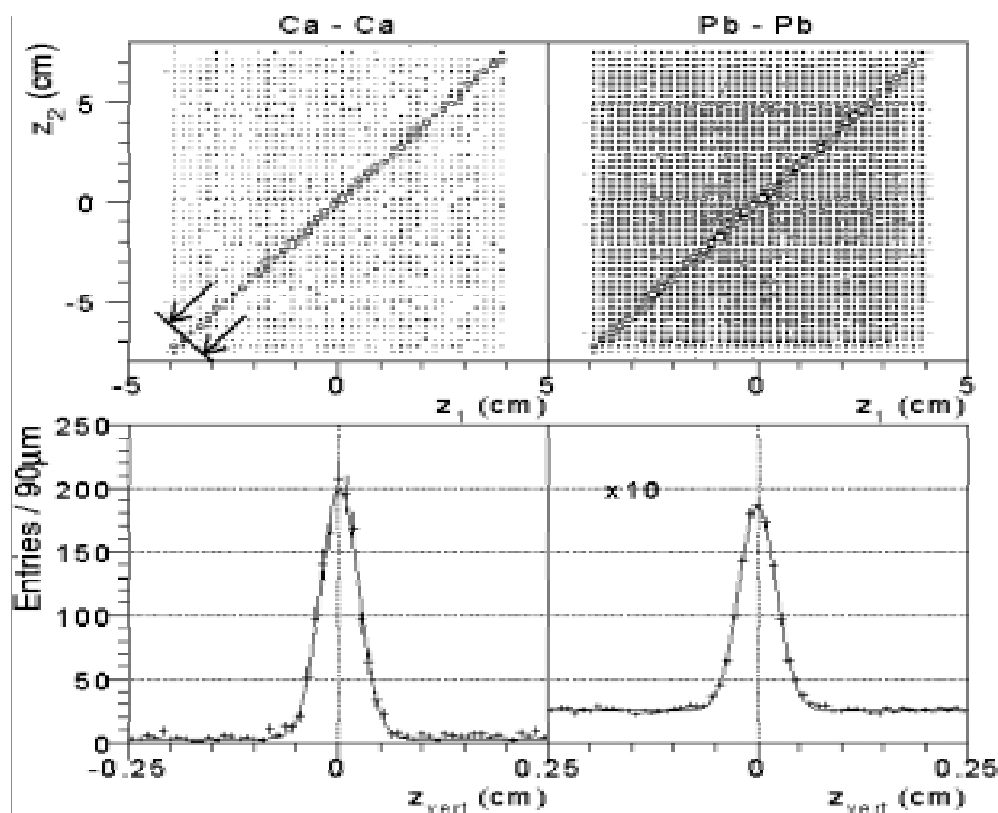
- Read-out capability during **high-L run** with dimuon spectrometer

➡ SPD highest rate central tracking device

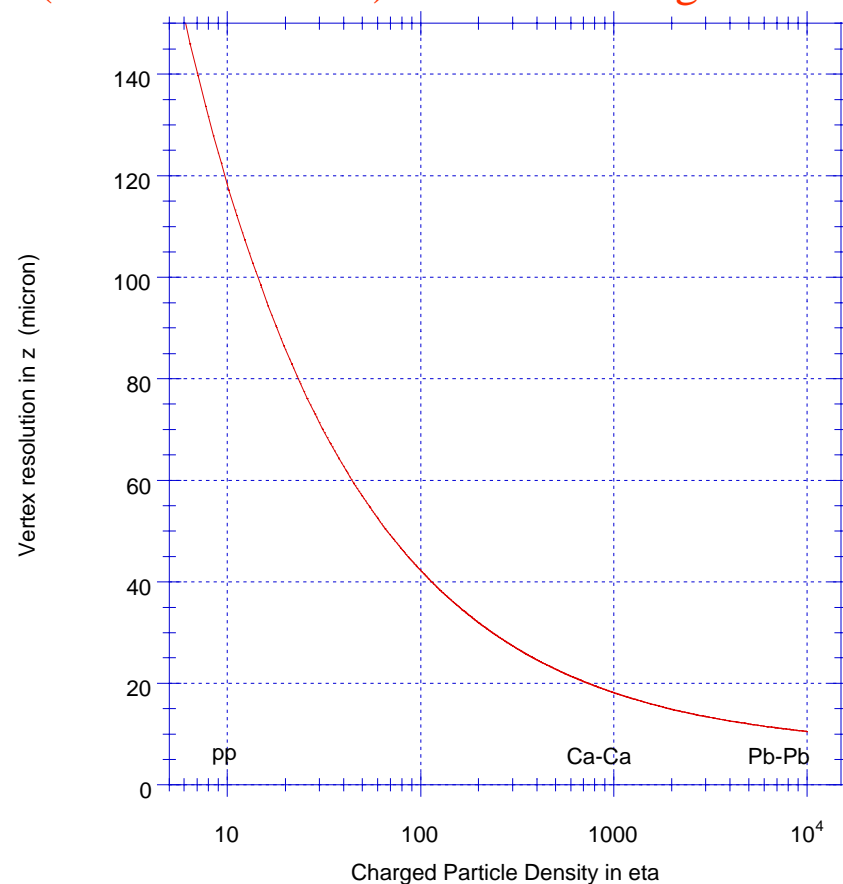


ALICE SPD STANDALONE PRIMARY VERTEX RESOLUTION (Z): **SIMULATION**

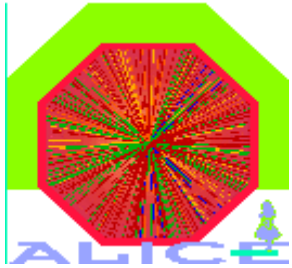
$\sigma(r\phi) < 10 \mu\text{m}$ & $\sigma(z) < 15 \mu\text{m}$ (low MLT events)....better for high MLT (!)



Correlation of the hits in the two pixel layers



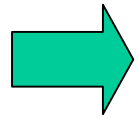
Resolution of the vertex along z-axis



ALICE SPD RADIATION TOLERANCE REQUIREMENTS

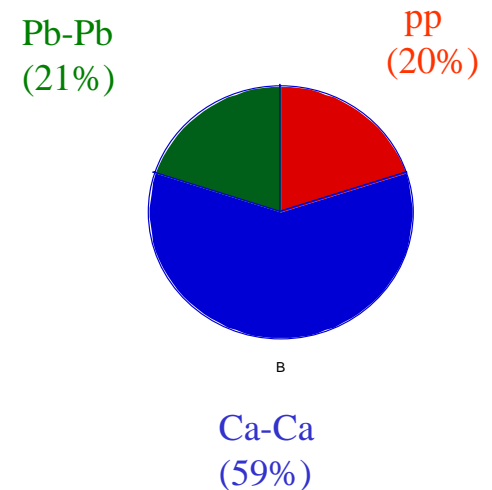
- At $r \sim 4\text{cm}$ during a running period of 10 years:

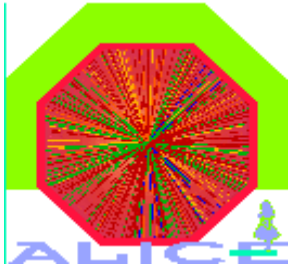
Total DOSE = 130Krad (1,3KGy)



Specification: $\sim 500\text{Krad}$ (50KGy)

Total neutron flux $< 10^{12} \text{ cm}^{-2}$





ALICE SPD: The **ALICE1** chip

FRONT-END CELL: “EDGELESS” DESIGN in 0.25 μm CMOS technology

Chip size $\sim 15\text{ mm} \times 14\text{ mm}$ & Total # transistors ~ 13 Million

RADIATION TOLERANCE issue:

tests done by X, γ rays & protons on Alice2Test chip done with final technology



It survives up to 30 Mrad

Main specifications:

Cell size	$50\text{ }\mu\text{m} (r\phi) \times 425\text{ }\mu\text{m} (z)$
Number of cells	$256 (r\phi) \times 32 (z)$
Minimum threshold	below 2000 e-
Threshold uniformity	200 e-
Strobe (LVL1) latency	up to 10 μs
Strobe duration	200 ns
Clock frequency	10 MHz

Robustness:

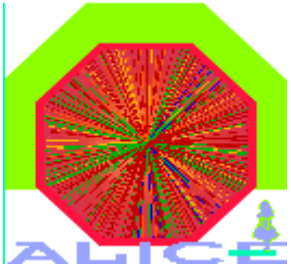
Individual cell threshold adjust (3bits)
Individual cell mask
Digital bias adjust
JTAG controls

Status:

Submitted to IBM



Expected back in July



ALICE SPD: **ASSEMBLY** OF R-O CHIPS

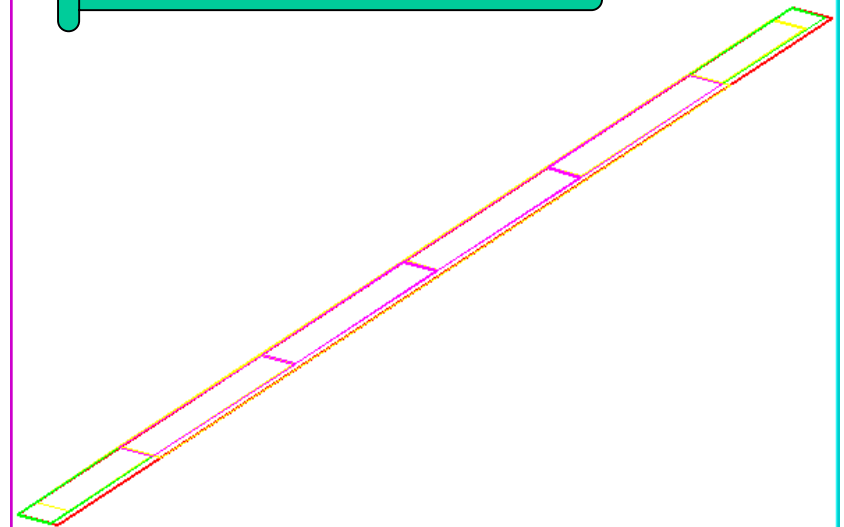
one-LADDER:

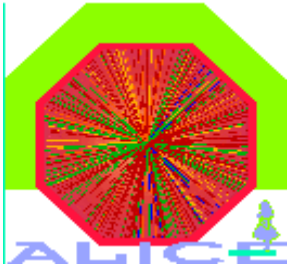
high resistivity silicon matrix
bump bonded to 5 read-out chips
("hybrid" technique)

half-STAVE:

two ladders
(10 r-o chips ~ 82k pixels)
+ one pilot chip
+ one optical link
+ timing & control interface

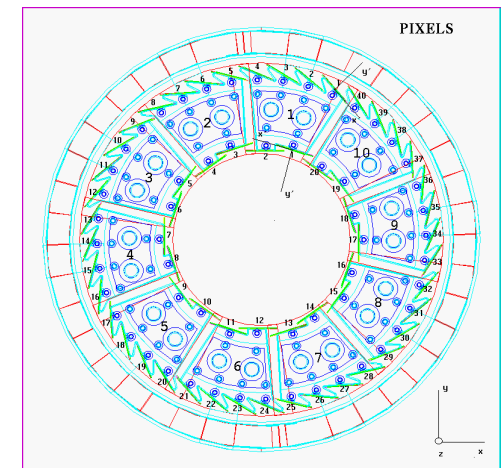
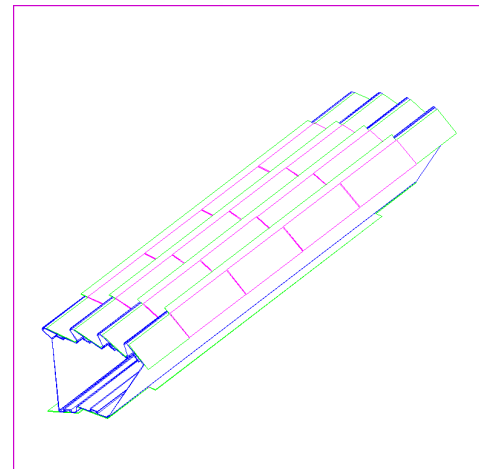
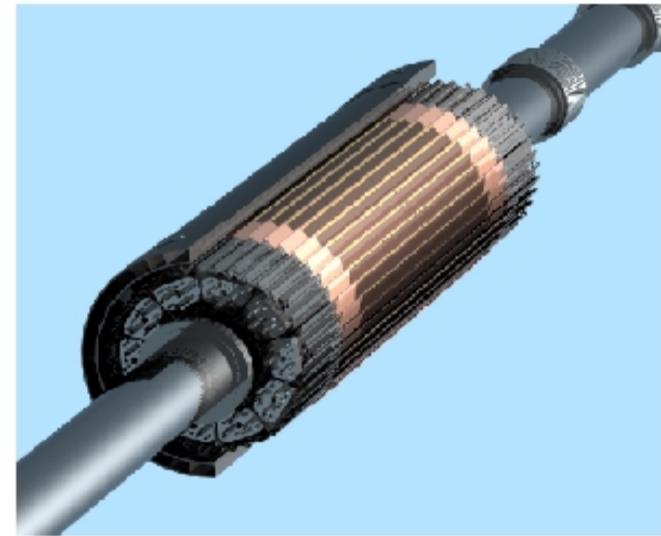
ONE STAVE

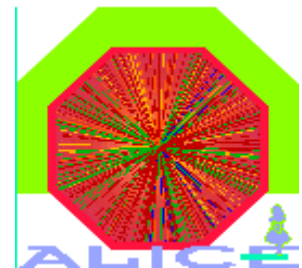




ALICE SPD: GLOBAL LAYOUT

10 carbon-fibre support sectors
 6 staves per sector
 (2 from inner
 4 from outer layer)
 In total:
 60 staves
 240 ladders
 1200 chips
 9.8 M pixel cells

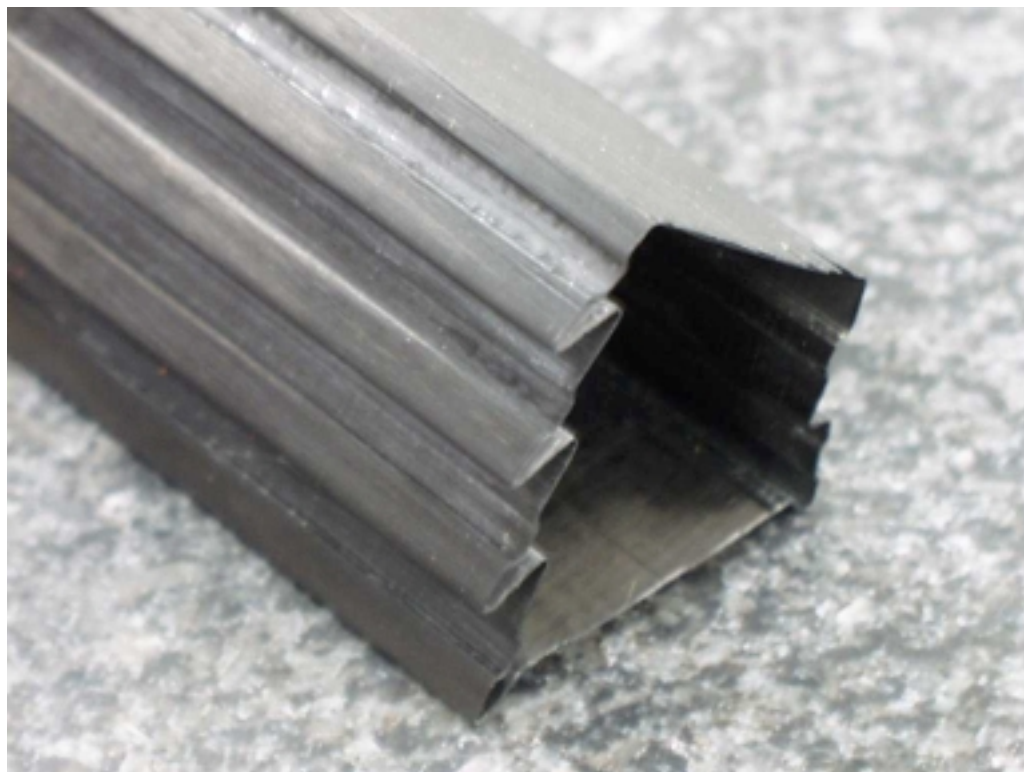




ALICE SPD: CARBON FIBER SECTOR PROTOTYPE

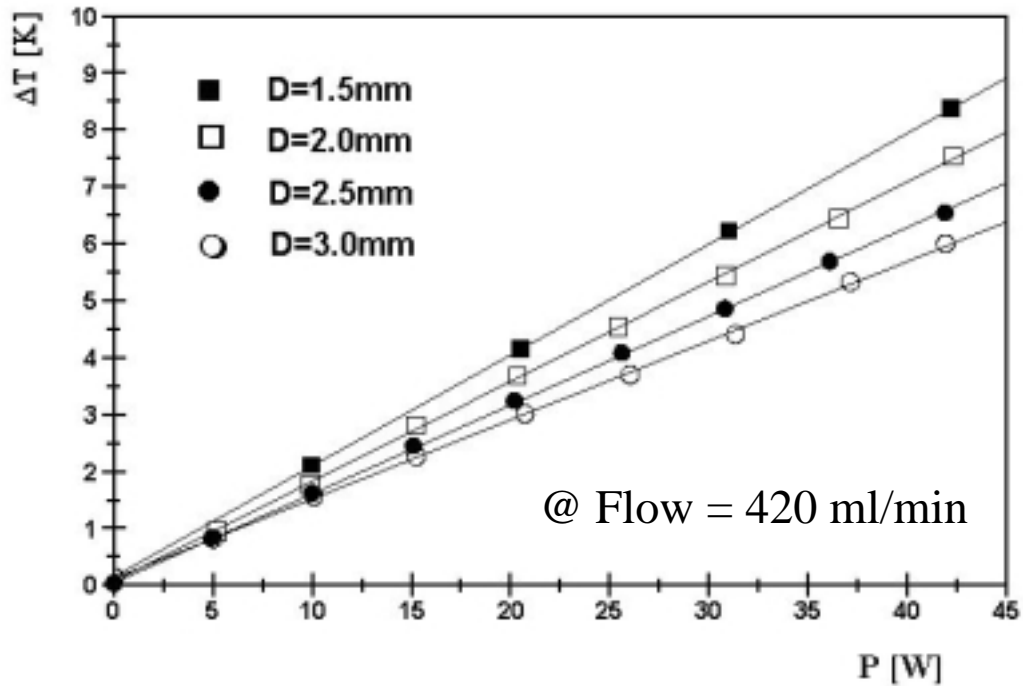
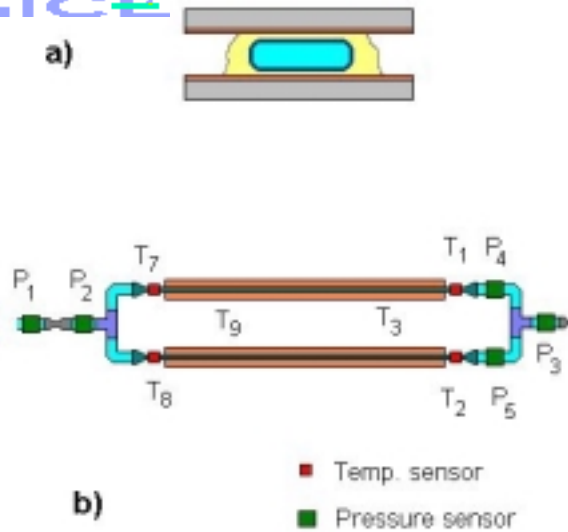
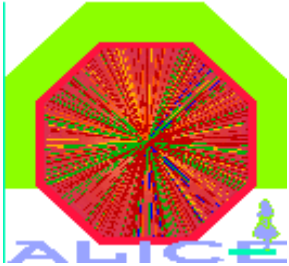


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ALICE SPD: COOLING SYSTEM



- **Efficiency** (within the allowed material budget $\sim 0.6 \% X_0$)
 - **Stability**
 - **Reliability**
- On the long term.

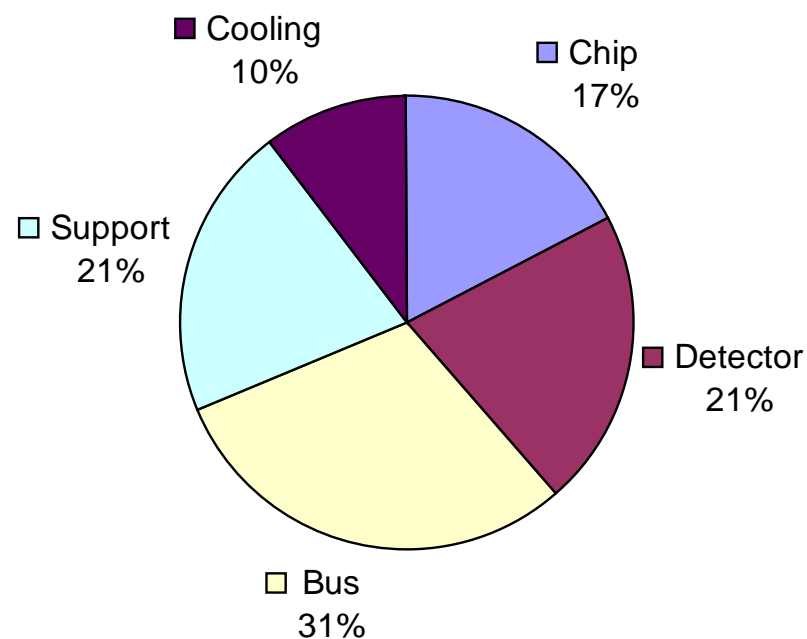
Inert coolant: C_6F_{14}
FLUOROCARBON ($P > 1 \text{ bar}$)

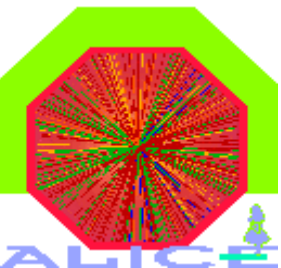


ALICE SPD: AMOUNT OF MATERIAL

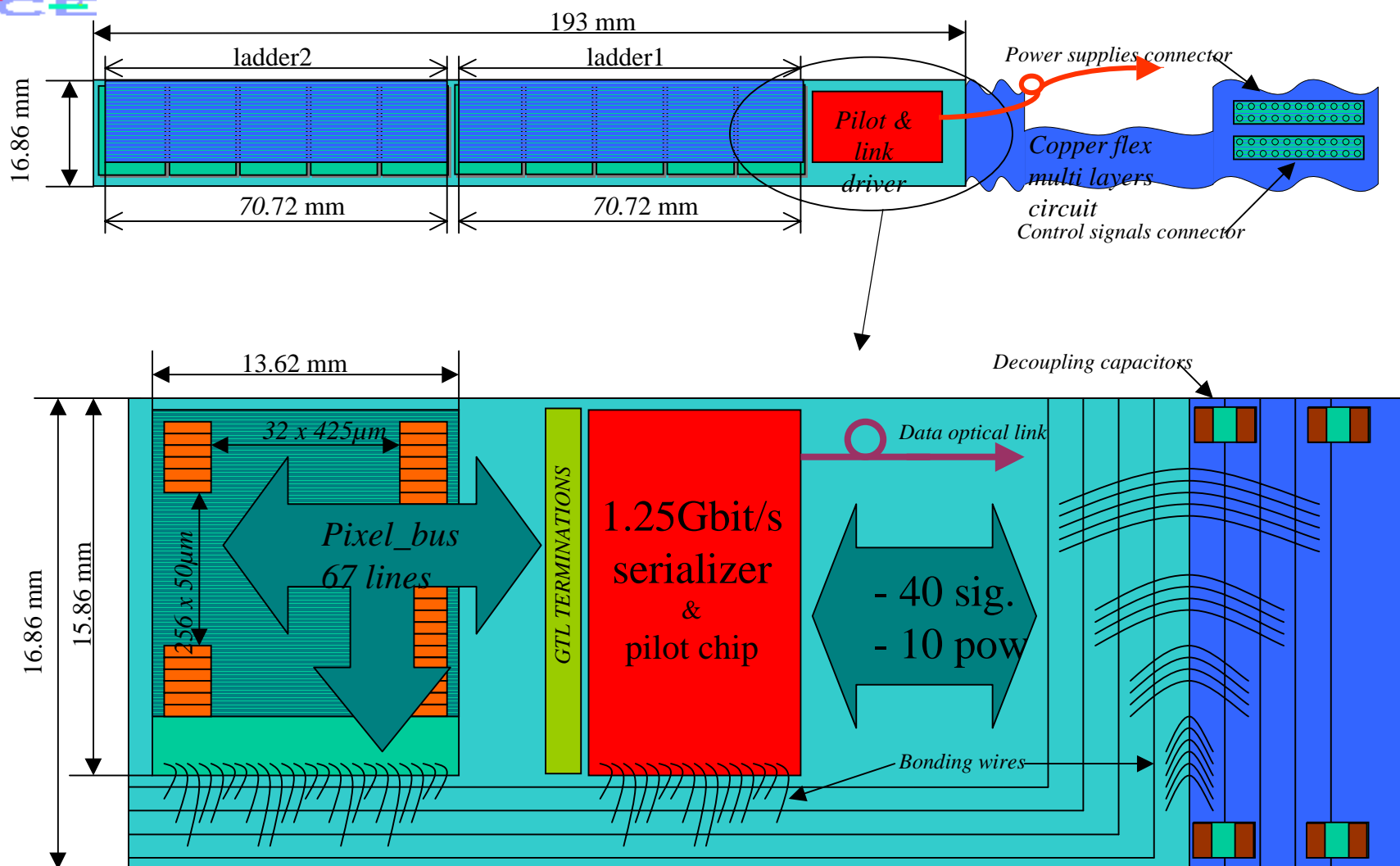
- A **straight track** perpendicular to the beam line crossing both layers sees on average $1.7 \% X_0$
- The **external shield** contributes an additional $0.25 \% X_0$

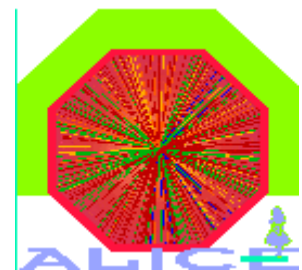
Material breakdown



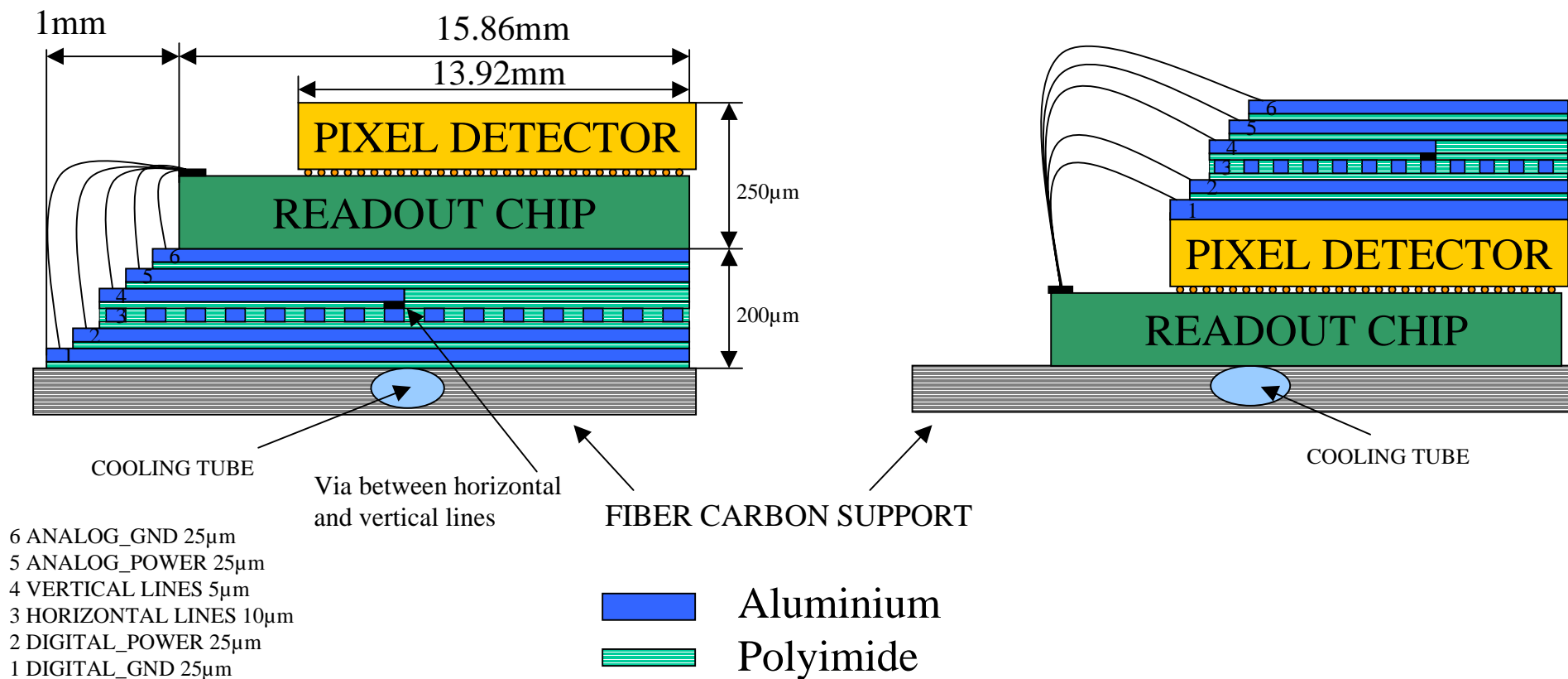


ALICE SPD: **PIXEL BUS** ISSUE





ALICE SPD: TWO **PIXEL BUS** HYPOTHESIS



Solution A

Solution B

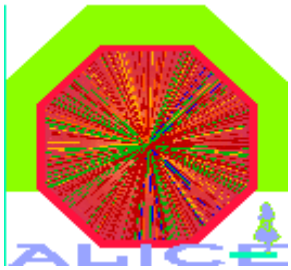


Each one has **pros** and **cons**: more studies are needed to decide

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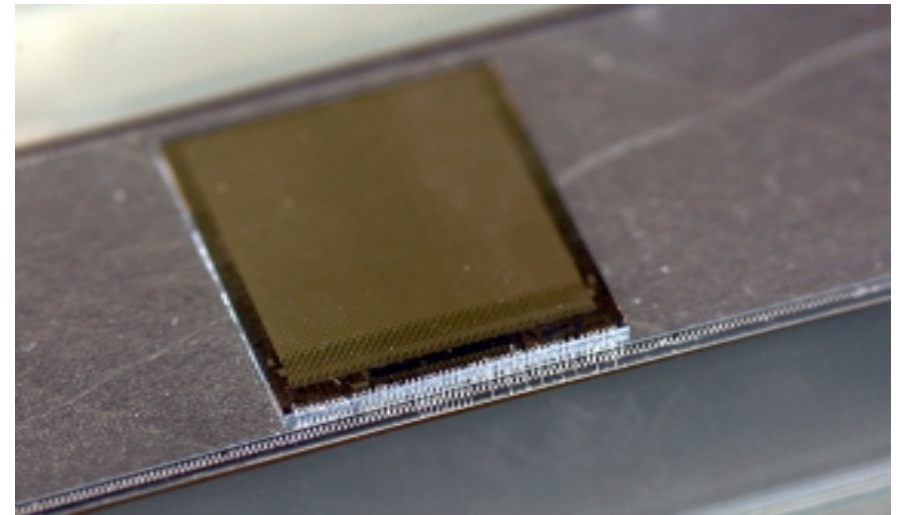
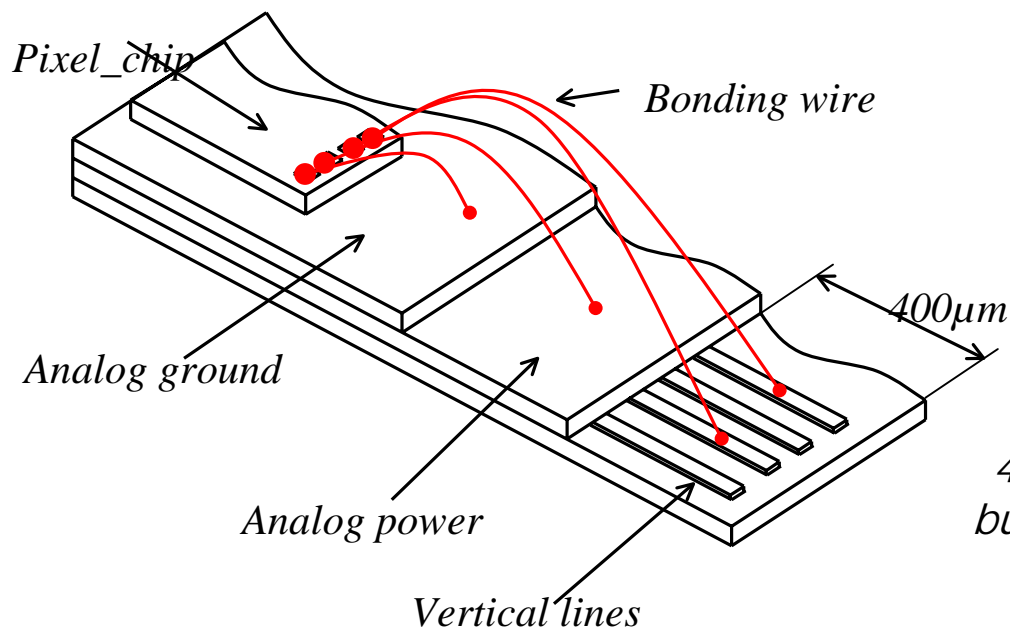
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ALICE SPD: MULTI LAYERS BONDING CONNECTIONS ISSUE

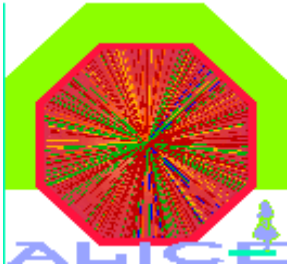
1-st essay



200mm x 17mm
4 aluminium layers
bus = 81 lines 100µm

Aluminium: 15µm
Kapton: 50µm
Glue: 10µm
Total thickness: 300µm

...mechanically it's feasible! → Next step: 200µm & 6 Al layers



ALICE SPD: HALF STAVE R/O & CONTROL

PILOT CHIP: same technology as for front-end chip (0.25 μm “rad.tol.”)

→ **SLOW CONTROL:**

boundary scan, parameter loading (JTAG standard)

→ **TRIGGER DISTRIBUTION:**

LVL1 (5.5 μs) , BUSY

LVL2Y (100 μs), LVL2N (< 100 μs)

10 chips x 256 clock cycles @ 10 MHz (256 μs)

→ **READOUT CONTROL OF FRONT-END CHIPS**

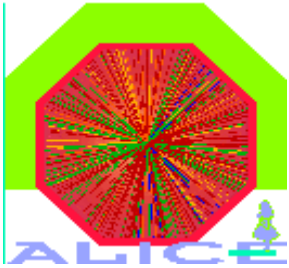
ROW DATA SERIALIZATION AND TRANSMISSION OFF-BARREL

zero-suppression & hit encoding done on ROUTER VME board (located in c.r.)

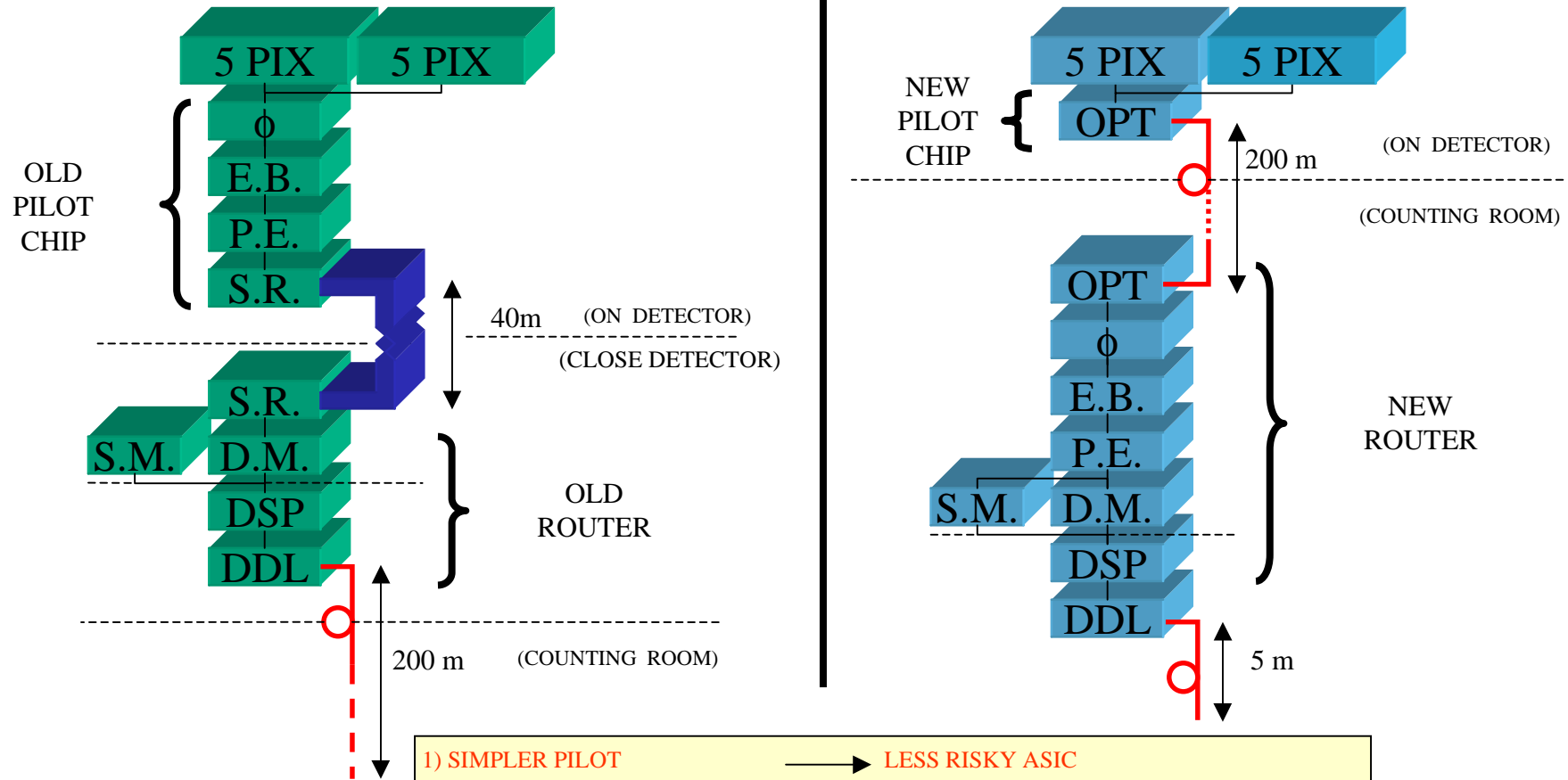
→ **CENTRAL Pb-Pb EVENT DATA SIZE:**

~ 400kbyte/event

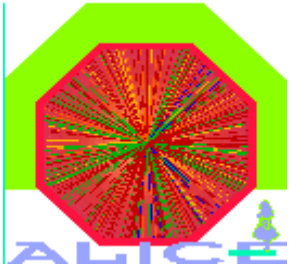
(50% data reduction possible formatting data, but with loss of redundancy!)



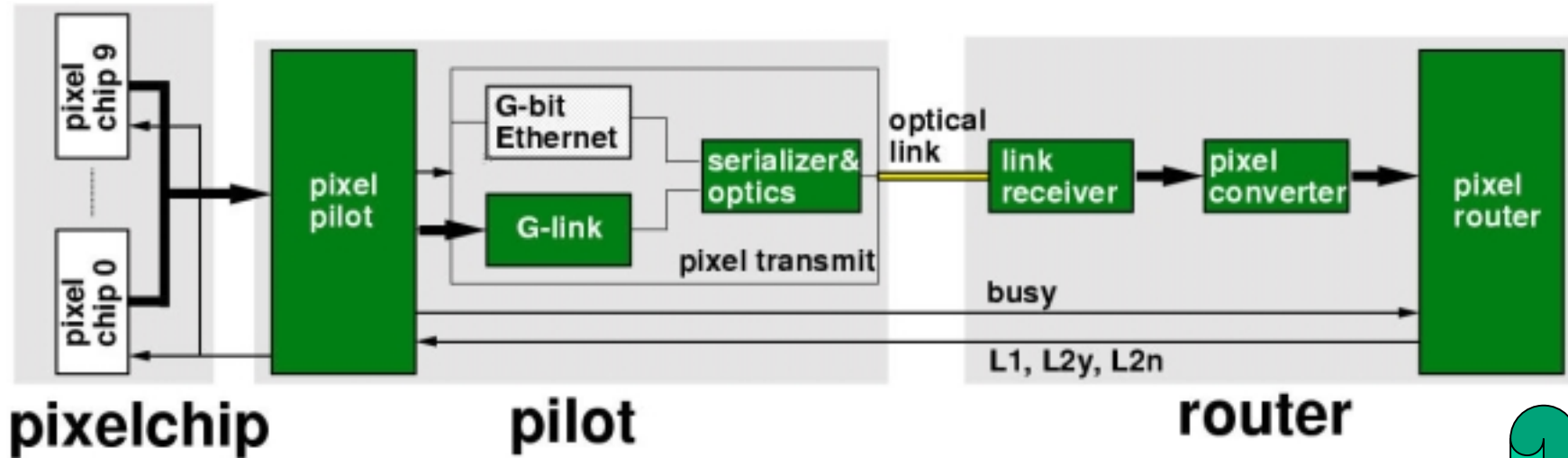
ALICE SPD: GLOBAL READ-OUT ARCHITECTURE (BLOCK DIAGRAM)



- | | | |
|----------------------------|---|-------------------------------------|
| 1) SIMPLER PILOT | → | LESS RISKY ASIC |
| 2) AVAIBLE F.E. OPT. LINK | → | LESS MAN POWER |
| 3) 200 m LINK | → | ROUTER ACCESSIBLE |
| 4) FPGA + MEM + DSP ROUTER | → | FLEXIBILITY FOR FUTURE "UPGRADINGS" |
| 5) RAW DATA TRANSMITTED | → | OCCUPANCY INDEPENDANCE |

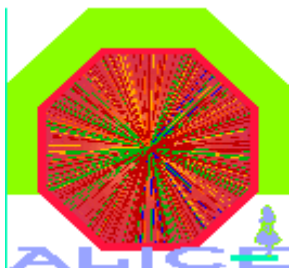


ALICE SPD: NEW PILOT CHIP ARCHITECTURE



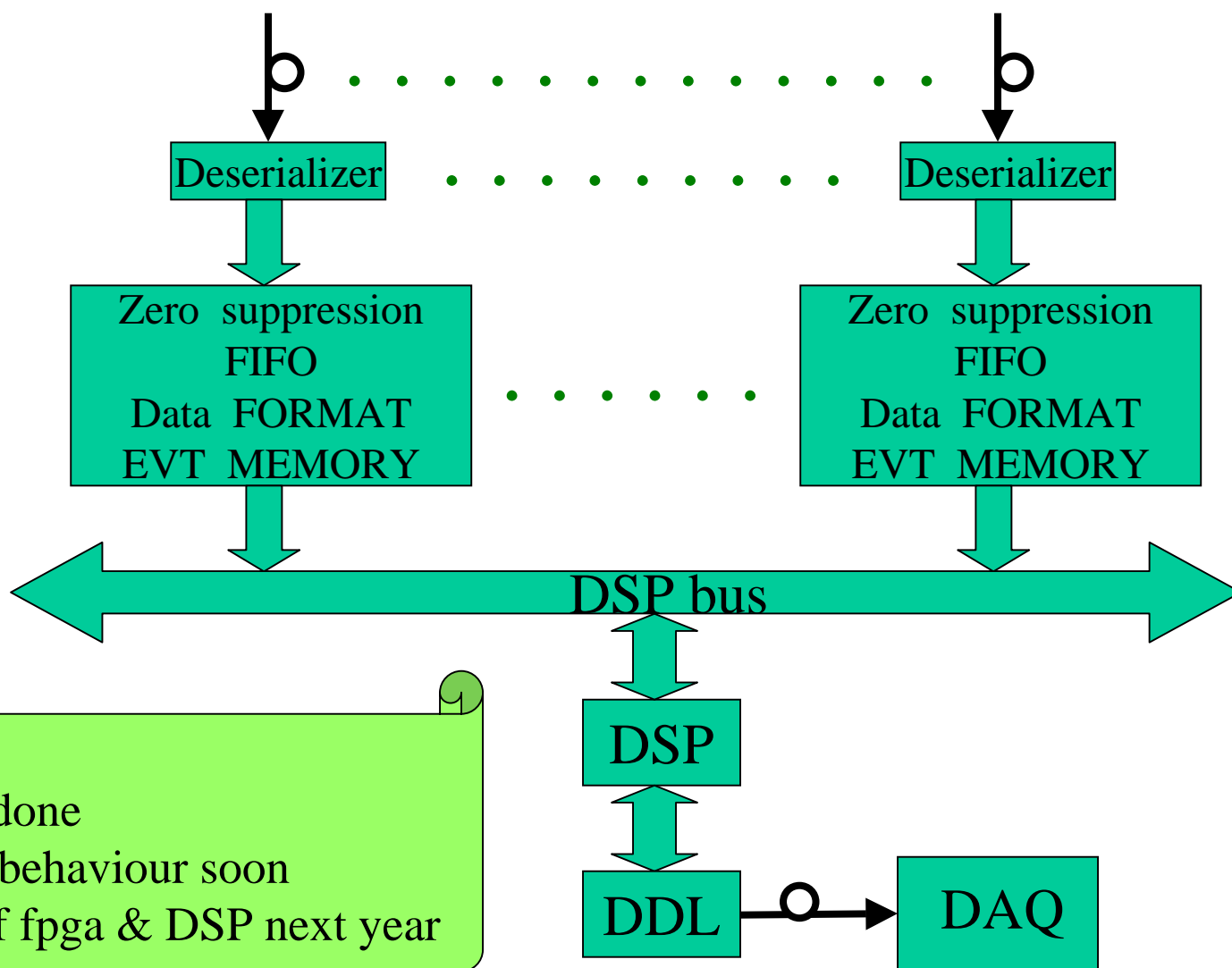
STATUS:

- Chip with **serializer & opto-amplifier** for the led-laser submitted last year
- Chip with **serializer & Glink encoder** ready to be submitted this year
- **Pixel pilot chip** will be submitted by the end of this year
- Chip with **all functionality** foreseen for next year



ALICE SPD: NEW ROUTER ARCHITECTURE

A VME board version
exists **now** !

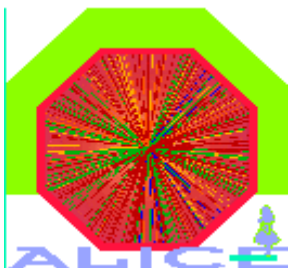


STATUS:

- HDL description done
- Simulation of the behaviour soon
- Implementation of fpga & DSP next year

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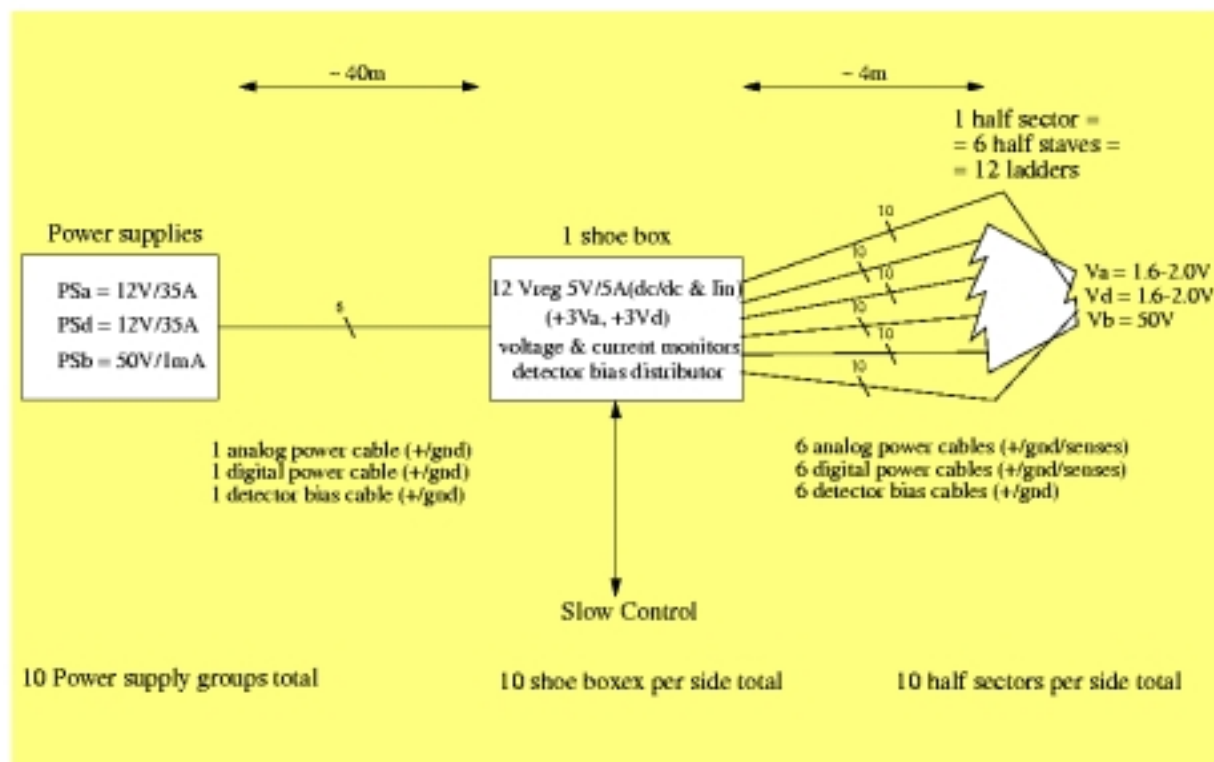
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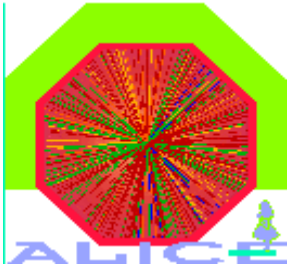


ALICE SPD: SERVICES ISSUES

Power distribution:

- Power supplies location in “safe area” ($\sim 40\text{m}$) outside L3 magnet
- Voltage regulation located on the shoe boxes: ($\sim 4\text{m}$) endcaps of the TPC?
or far ($\sim 20\text{m}$) for fast and easy access?
- V & I monitoring done at the level of shoe box



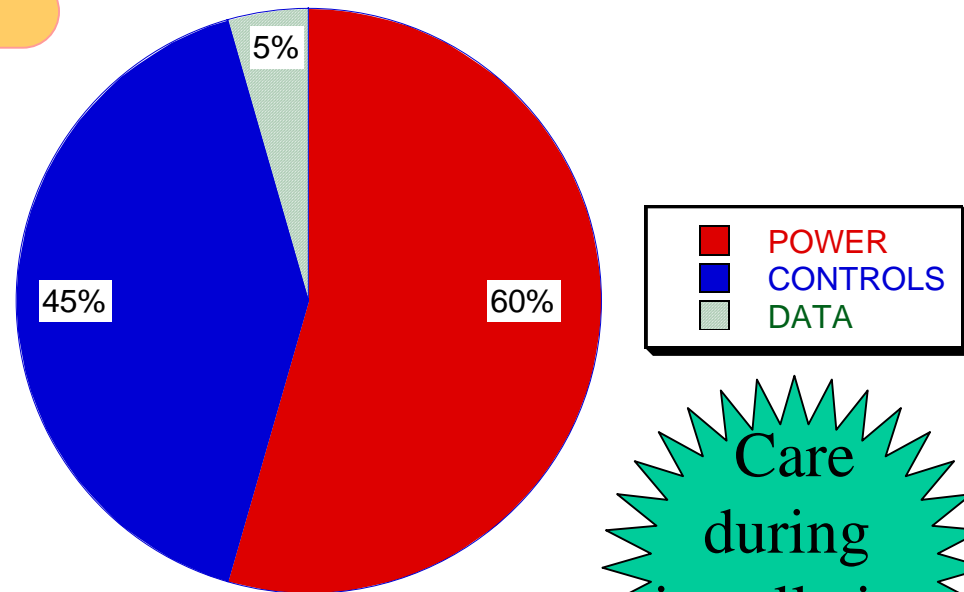


ALICE SPD: WEIGHT of the SERVICES

Cabling between patch panels (endcap) and pixel half-staves

Options:

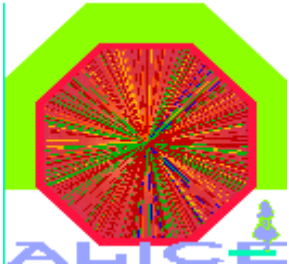
- kapton foil power cables or multiwires ribbon p.c.
- kapton foil signals cables or multiwires ribbon s.c. or multishielded twisted pair s.c.
- optical fiber



→ { ~ 110-140 g/half-stave & ~ 1m long cables system
Total weight for each side ~ 7-8 kg

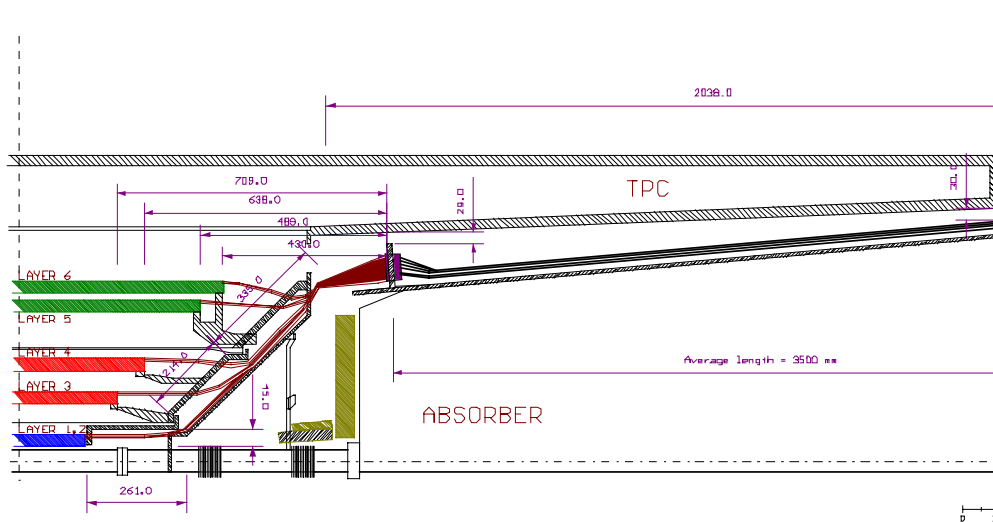
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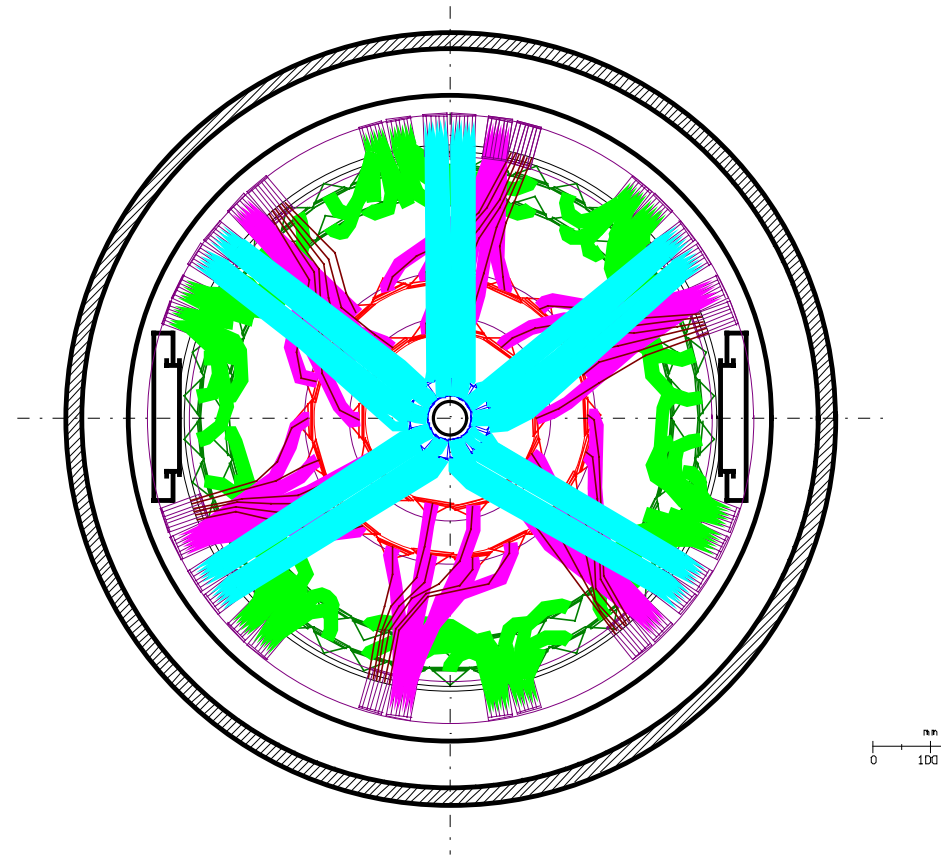
ALICE SPD: CABLING ISSUE

ITS CABLING LAYOUT PROPOSAL



Installation sequence issue:

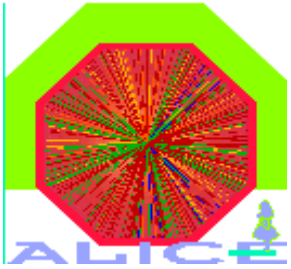
- Beam pipe
- SPD (two half shell)
- SDD+SST
- TPC



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ALICE SPD: CONCLUSIONS

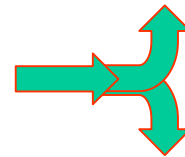
System architecture



Radiation damage



Technological aspects



Infrastructure

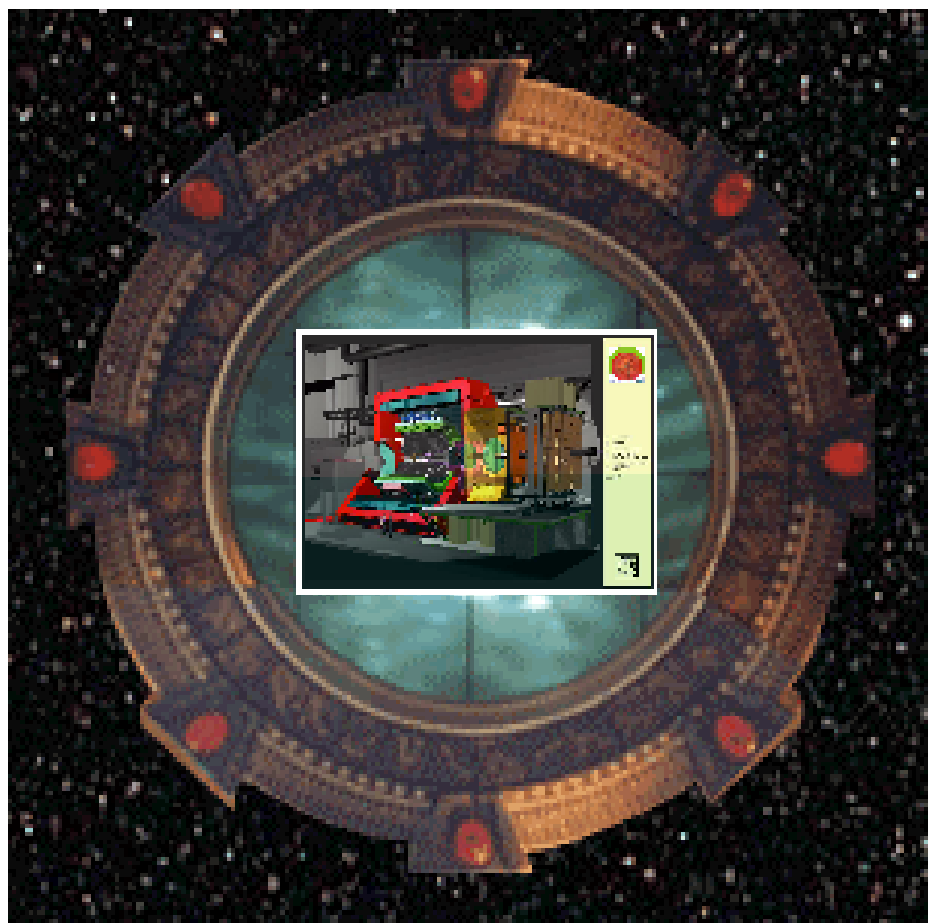


Installation





ALICE SPD is our QGP gate...



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