

Overview of the BTeV Pixel Detector

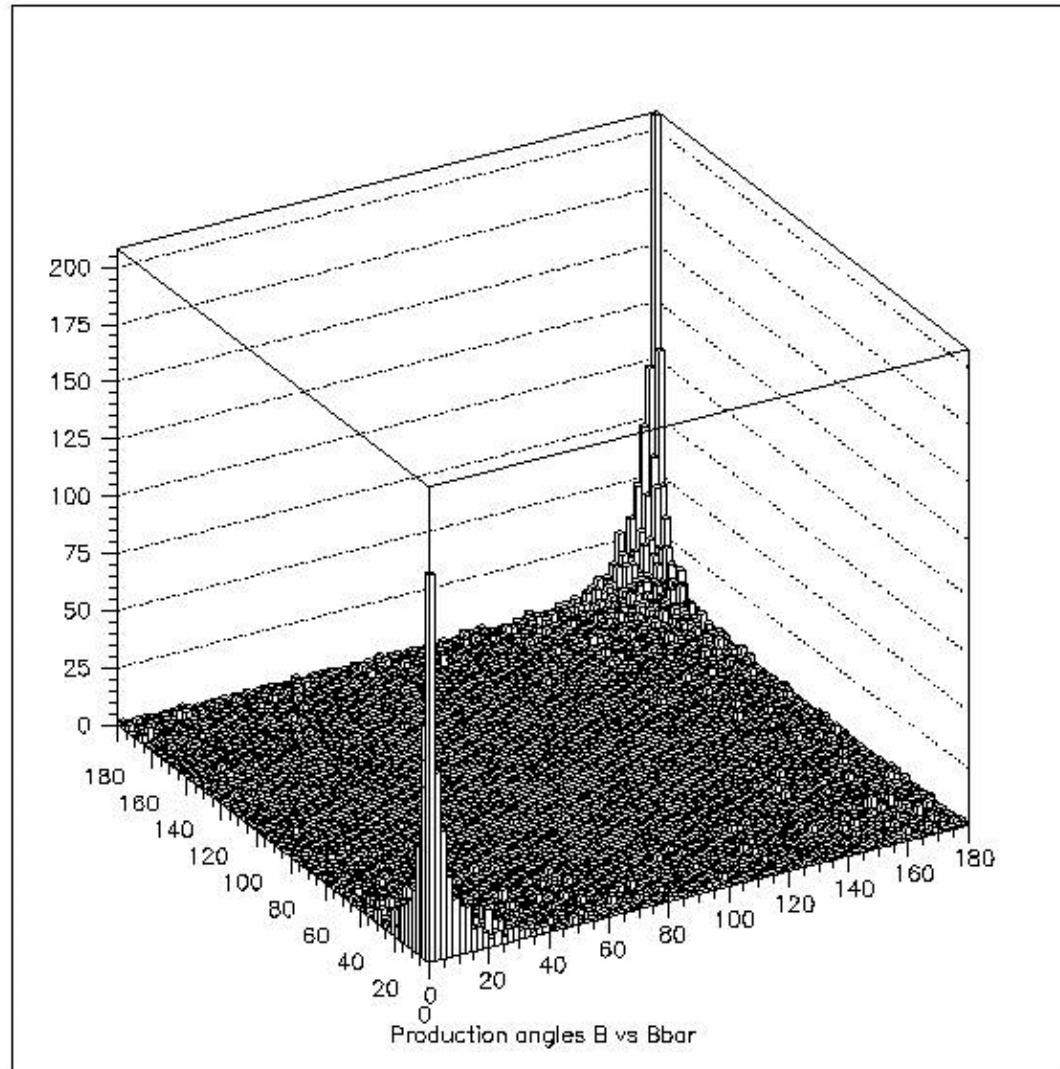
Charles Ray Newsom
University of Iowa
for the BTeV collaboration

Outline

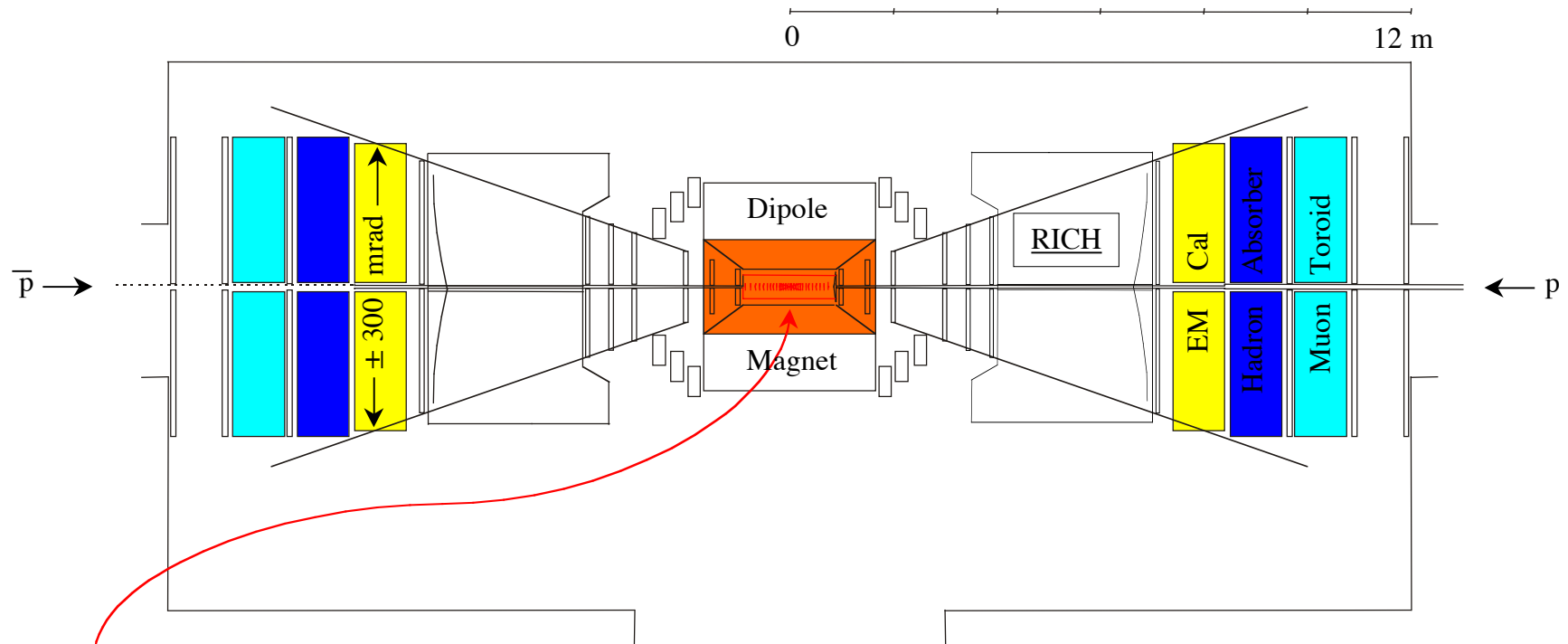
- BTeV-A Brief Summary
- Experimental Layout
- Pixel Layout
- Level 1 Vertex Trigger
- Pixel Readout Chip Development
- Fermilab Test Beam Measurements
- Summary and Conclusions



Forward Detector Maximizes Acceptance for Both B's



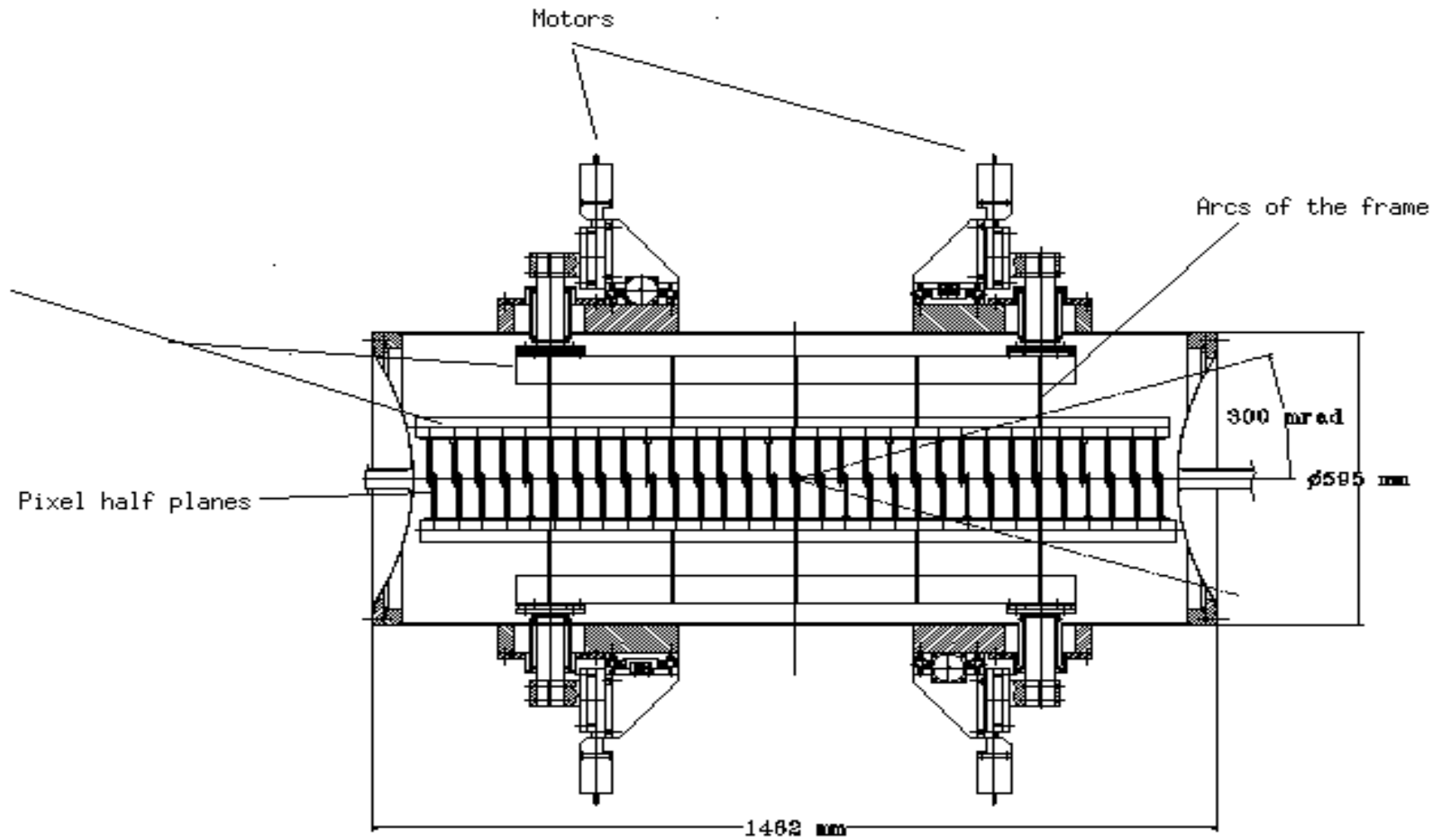
Plan View of the BTeV Detector



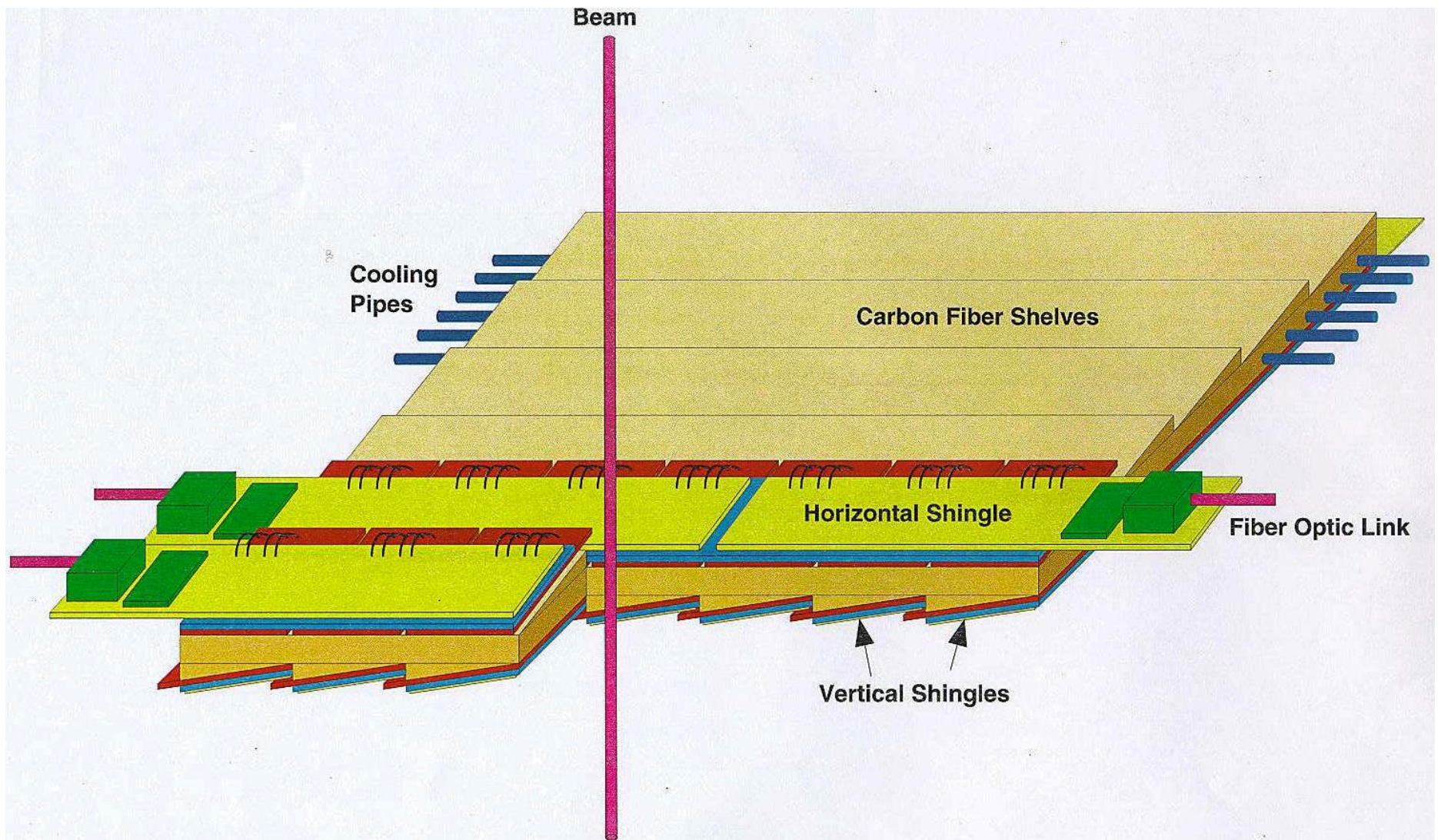
Pixel System (in vacuum):

- 31 stations distributed over 128 cm (± 64 cm)
- Each station has 2 planes arranged in “views” (y,x)
- Each plane has 500,000 pixels in a 10 x 10 cm area (square beam hole)
- Each pixel is $50\mu \times 400\mu$ in size (pulse height measurement for each pixel)

Side View of the Pixel Detector



Sectional View of a Pixel Half Plane



Pixel Based Vertex Trigger

- A key design feature of the system is that the pixel information will be used in the level 1 (lowest level) trigger.
- A fast data driven readout is required.
- Pixel planes are close to the beam, and in vacuum
 - Radiation level comparable to ATLAS/CMS
 $\sim 10^{14}$ particles/cm²/year.
- Retractable upper and lower assemblies

Level 1 Vertex Trigger using Pixel Data

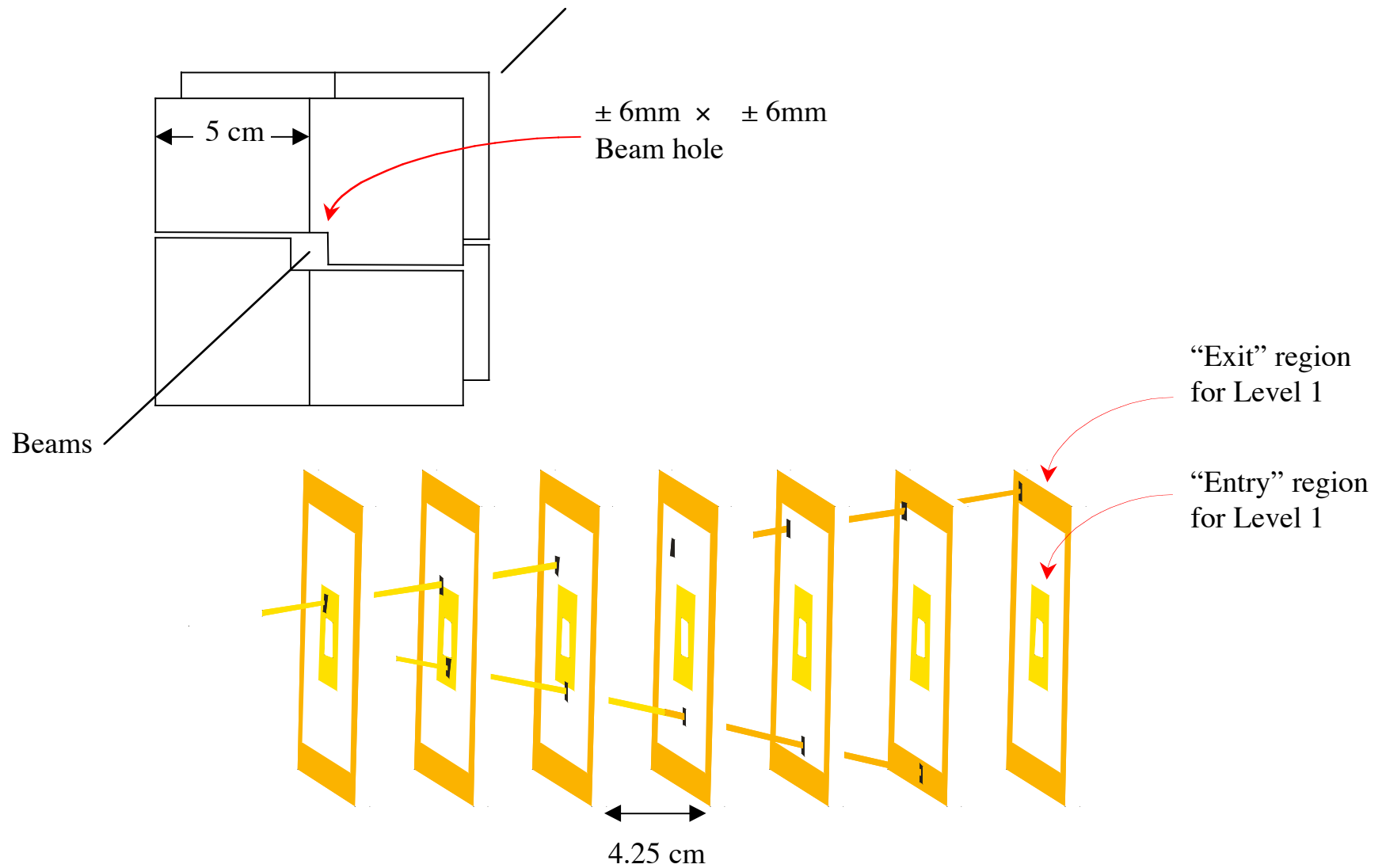
The Level 1 trigger performs 4 analysis steps:

- Track segment finding
- Track segment matching and extrapolation to the beam region
- Primary vertex reconstruction and impact parameter calculation for detached tracks
- Trigger decision based on the number of tracks with large impact parameter

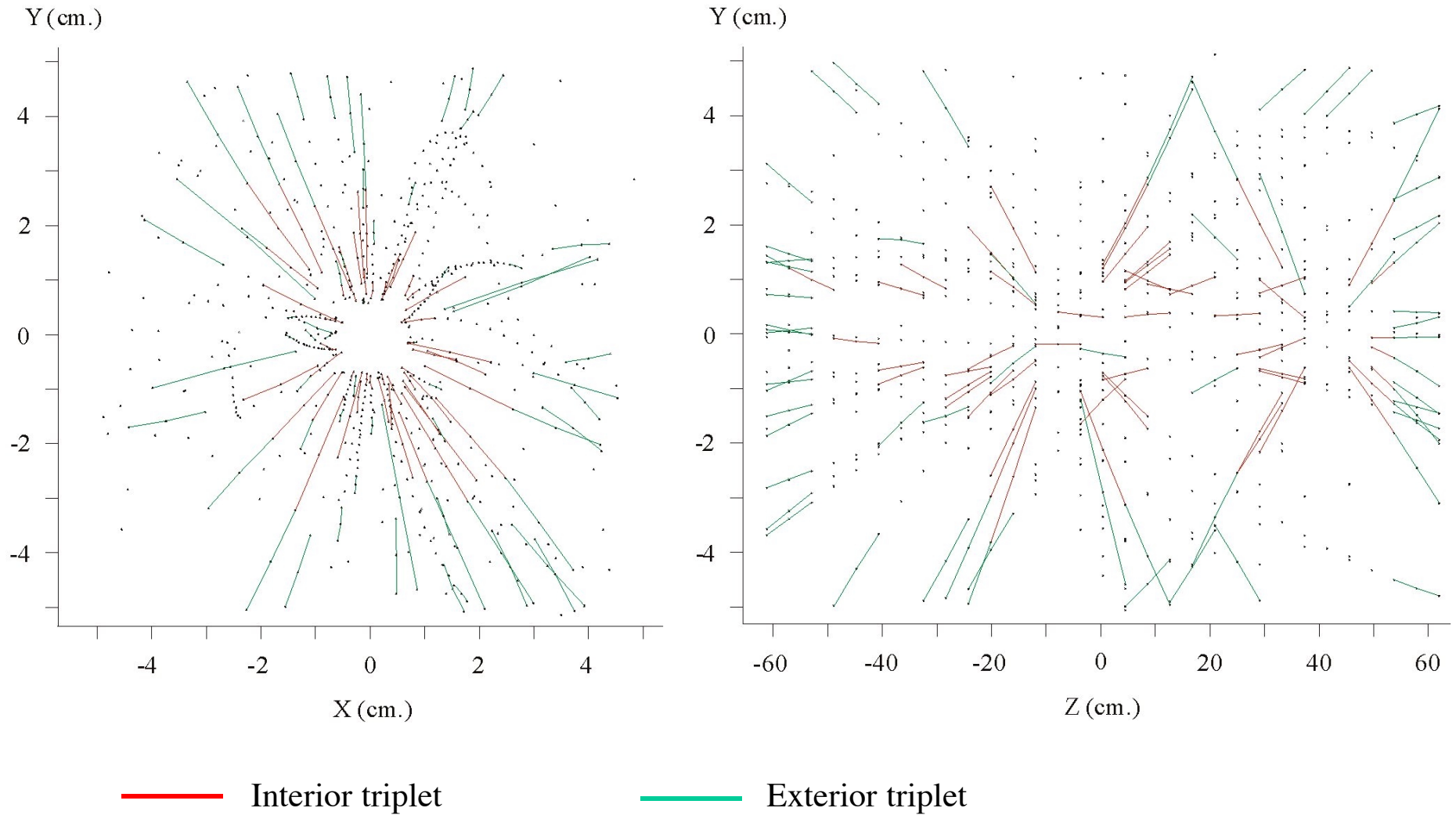
Key features of the baseline trigger:

- finds track segments as particles **enter** and **exit** the pixel detector
- simple and draconian removal of fake tracks (kill tracks that share hits)

Close-up View of the Pixel System



Pattern Recognition for a Generic B Event



FPIX0 characteristics

- HP 0.8 μ m technology
- Established front end concept
- Demonstrated analog/digital isolation
- Analog output from chip
- Bonded to ATLAS sensors
(50 μ m x 400 μ m pixels)
- 12 columns by 64 rows

FPIX1 characteristics

- HP 0.5 μm technology
- High Speed readout (132ns bunch crossing with multiple interactions per crossing)
- 2 bit FADC in each readout pixel
- Bonded to ATLAS sensors (50 μm x 400 μm pixels)
- 18 columns by 160 rows

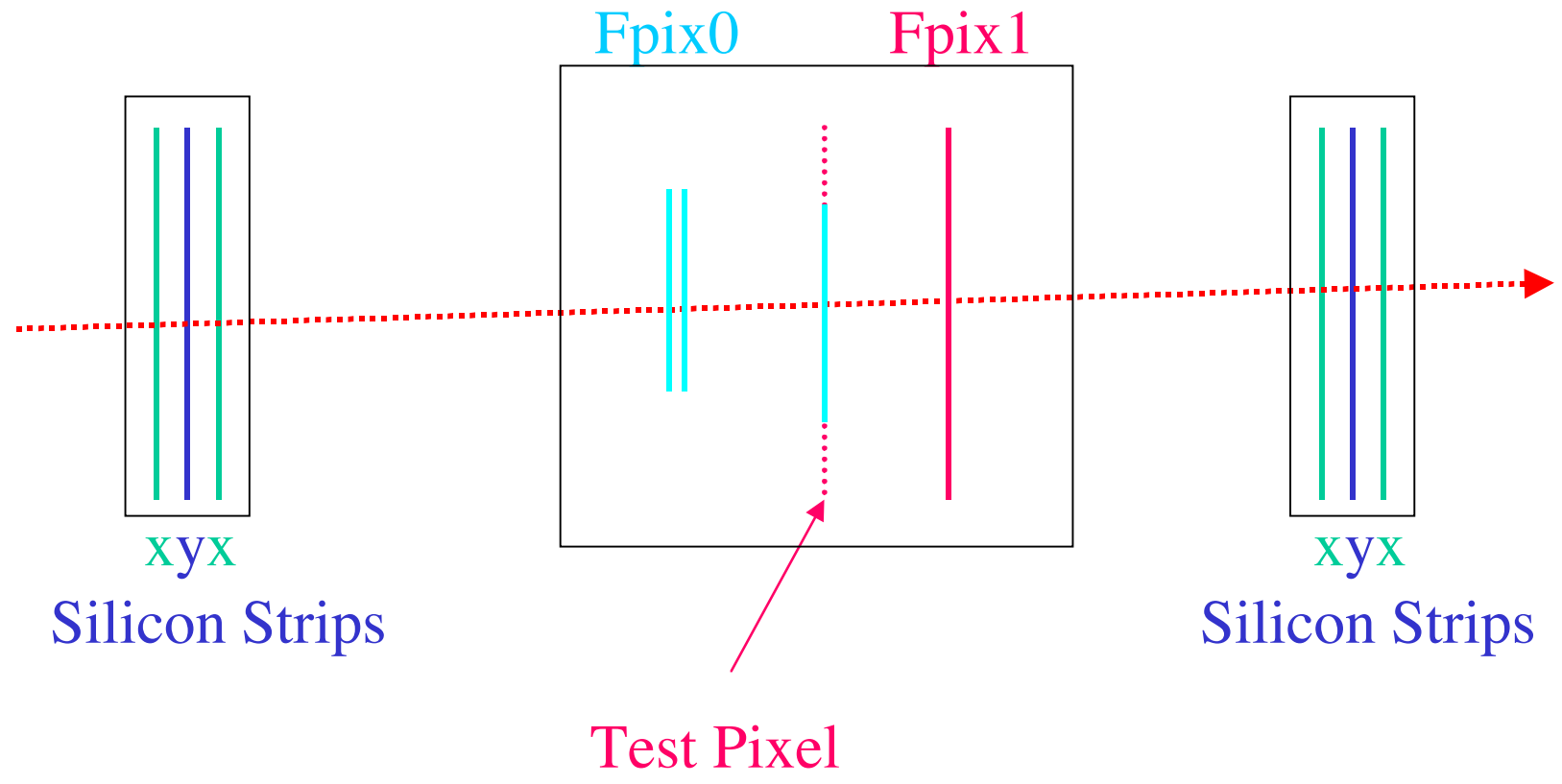
FPIX2 characteristics

- Commercial 0.25 μm CMOS technology
- 50 μm x 400 μm pixels
- Significant modifications from FPIX1
 - Analog front end (feedback and leakage compensation)
 - Digital sections (simplified EOC logic, reference currents and thresholds generated on chip)
- 3 bit FADC in each readout pixel
- Radiation hard!

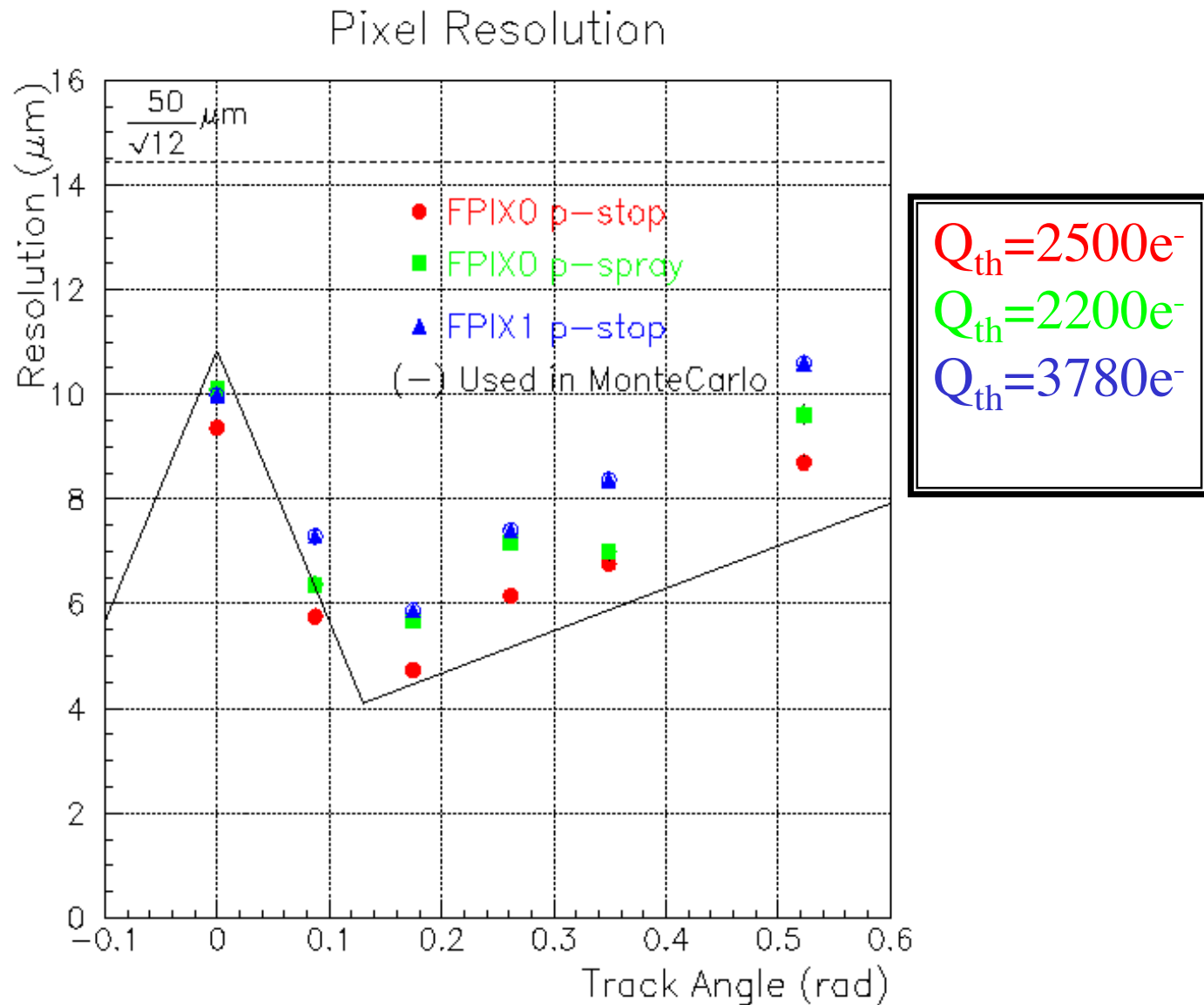
Pixel Beam Tests

- 227 GeV pion beam
 - 6 plane (in 2 stations) silicon strip telescope
 - 1 to 4 plane pixel telescope
 - Resolution studies
 - Incident angle
 - Threshold
 - Bias voltage
 - Number of digitization bits
 - Study P-stop and p-spray sensors
 - Magnetic field effects
-

Pixel Beam Test Telescope



Readout Chip and Detector comparisons



Future Work

- FPIX2
- Continue Mechanical, Electrical and Cooling Structure Research and Development
- Get Approved!
Proposal* Submitted May 15, 2000
- Build the Experiment!

*http://www-btev.fnal.gov/public_documents/btev_proposal/index.html



BTeV Pixel 2000 Talks

- Gabriele Chiodini: “1999 (BTeV) beam test results”
June 6, 11:20-11:40
- Abder Mekkaoui: “BTeV Front End Electronics”
June 6, 16:10-16:35
- Marina Artuso: "Study of the spatial resolution achievable with the BTeV pixel detector"
June 7, 10:15-10:30
- Sergio Zimmermann: "Development of high data readout rate pixel module and detector hybridization at Fermilab"
June 7, 14:55-15:15



Data Flow in the Level 1 Trigger

