

# Pixel readout electronics development for ALICE PIXEL VERTEX and LHCb RICH

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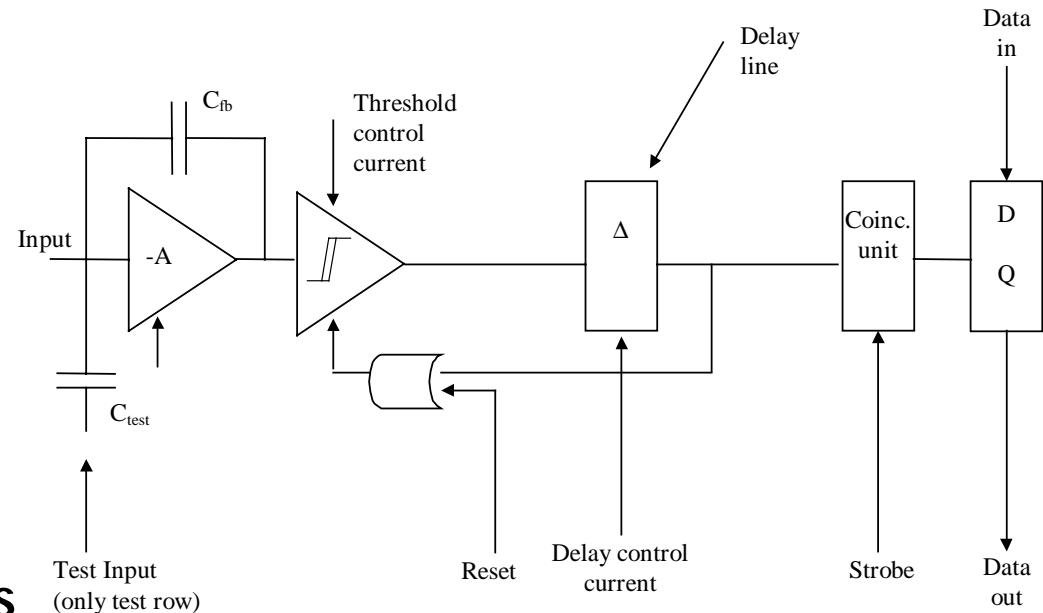
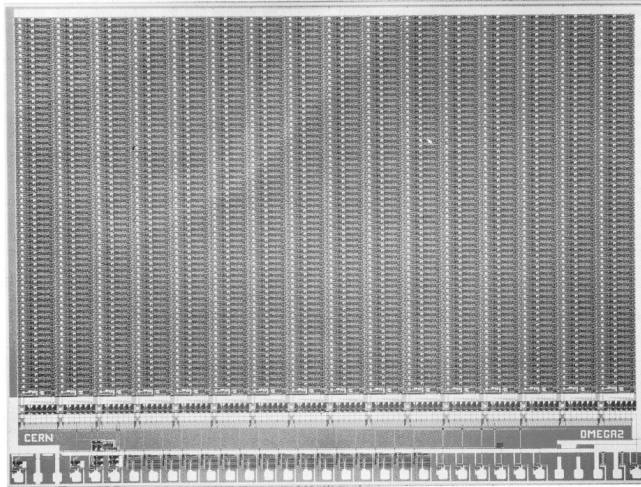
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# Outline

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- ◆ Previous full readout chips
  - Omega2
  - Omega3/LHC1
- ◆ Two testchips
  - 0.5  $\mu\text{m}$  CMOS
  - 0.25  $\mu\text{m}$  CMOS
- ◆ New chip for ALICE pixel and LHCb RICH
  - Chip description
  - Design for radiation tolerance
  - Design for testability
  - Design for uniformity
- ◆ Special issues
- ◆ Conclusions

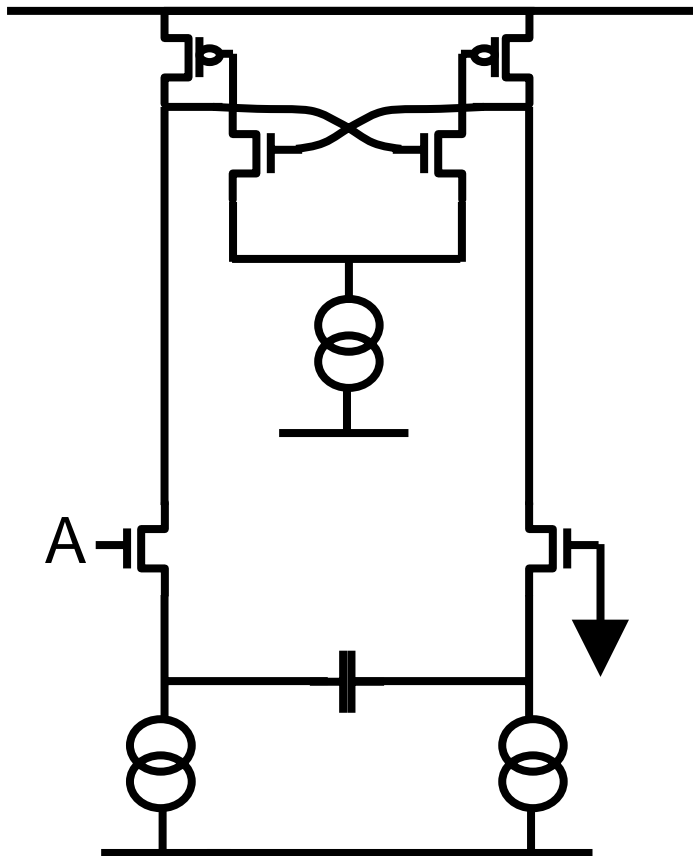
# Omega2



- ◆ Binary position information
- ◆ Pixel  $75 \times 500 \mu\text{m}^2$ , 64 rows by 16 columns
- ◆ Leakage current sensing cell at the bottom of each column
- ◆ Internal delay per pixel (current deprived invertors), dead for twice the trigger delay
- ◆ Shift register readout after level 1 trigger
- ◆ Limited testability : only one test row at the top
- ◆ Two metal layers only : no shielding between electronics and detector
- ◆ ~ 80 transistors/pixel (Self Aligned Contact  $3 \mu\text{m}$  technology)
- ◆ Dies at  $< 50\text{krad}$

# Omega3/LHC1

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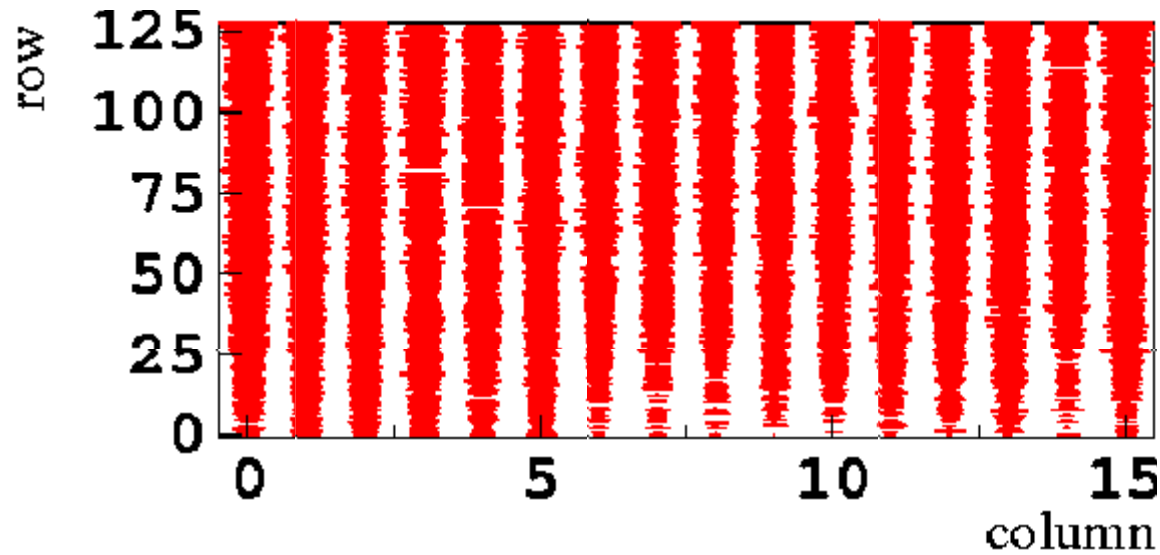


**Discriminator**

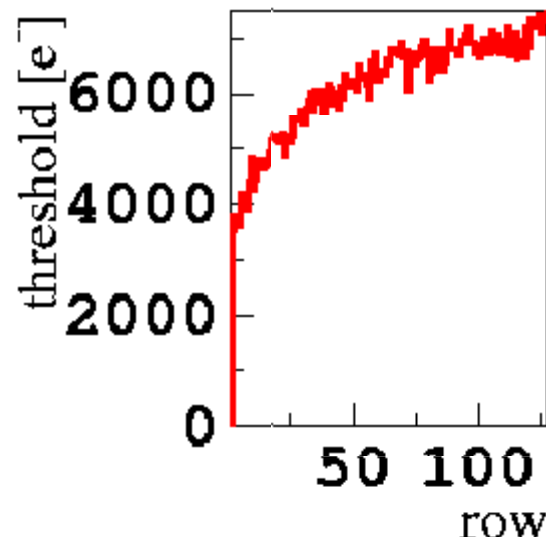
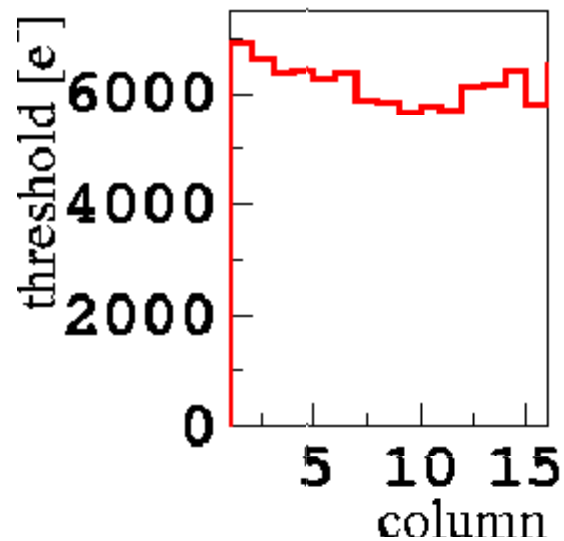
- ◆ Pixel  $50 \times 500 \mu\text{m}^2$ , 128 rows by 16 columns
- ◆ Internal delay per pixel (current deprived invertors), front end reset after small fraction of the trigger delay
- ◆ Shift register readout after level 1 trigger
- ◆ All pixels can be tested electrically
- ◆ Third metal shield
- ◆ ~ 380 transistors/pixel (Self Aligned Contact  $1 \mu\text{m}$  technology)
- ◆ Dies at  $< 50\text{krad}$
- ◆ Discriminator (see left) trade-off between threshold uniformity and speed
- ◆ Preampifier feedback

# Omega3 testability gave a wealth of information

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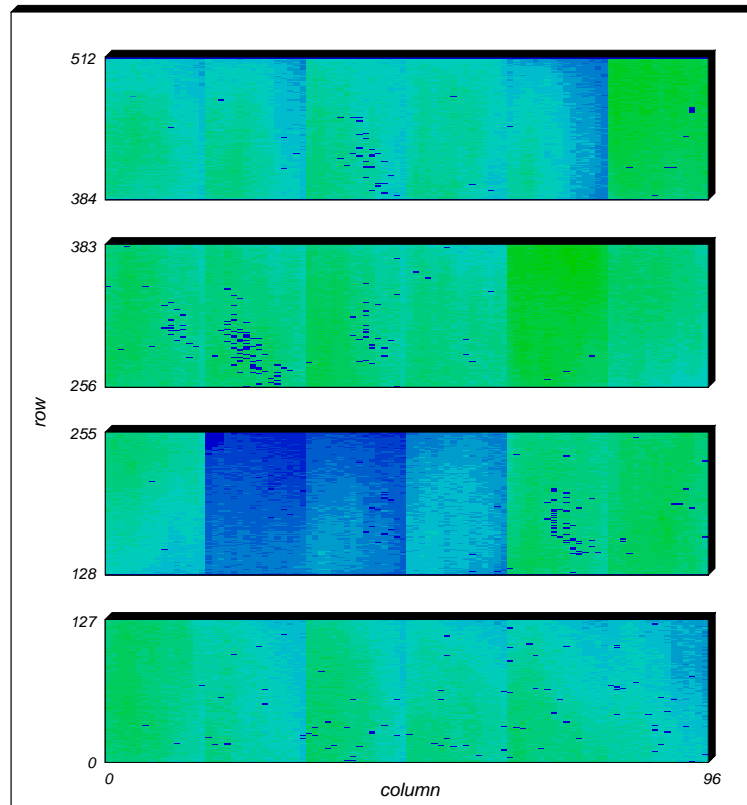


Top-down threshold  
variation due to  
resistive drop

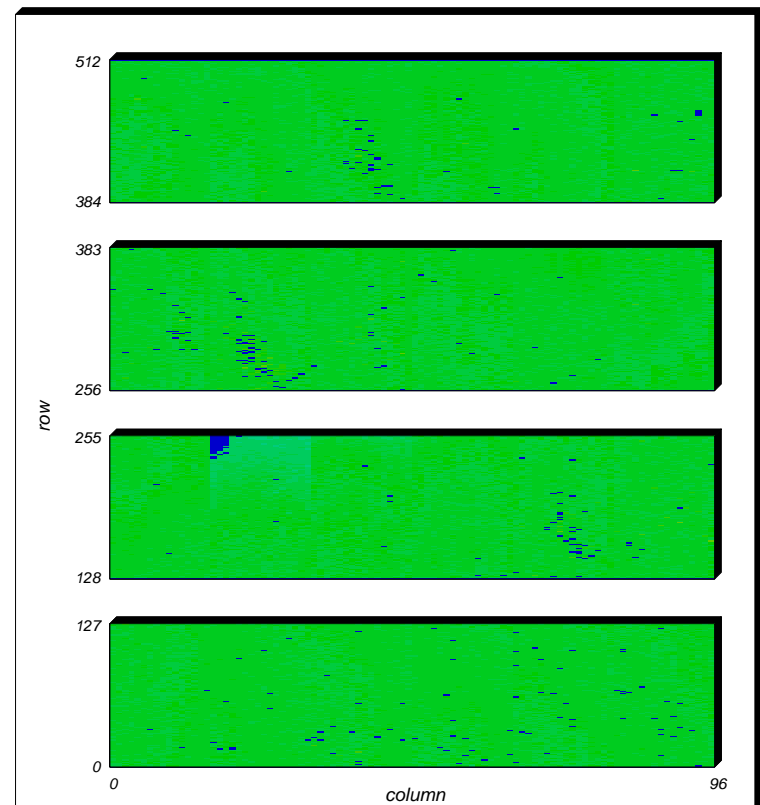


fixed in correction run

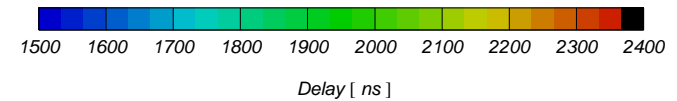
# 3 bit delay adjust on half plane (~ 50 000 channels)



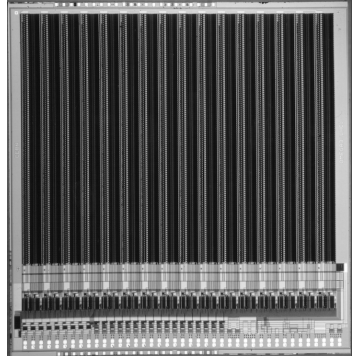
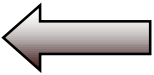
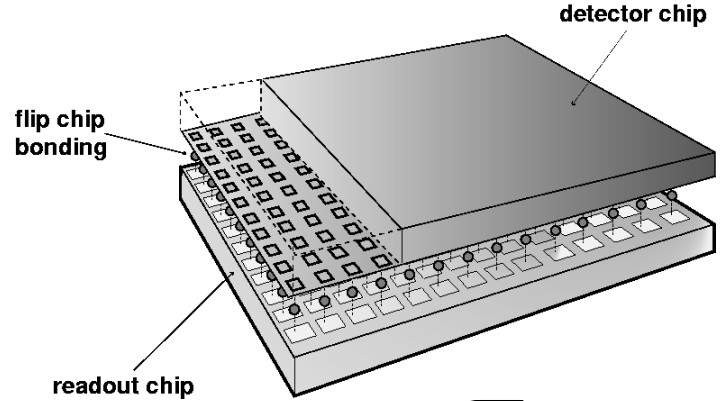
Before



After

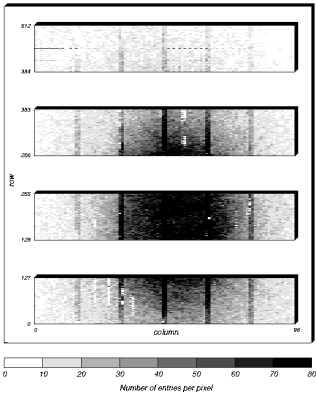
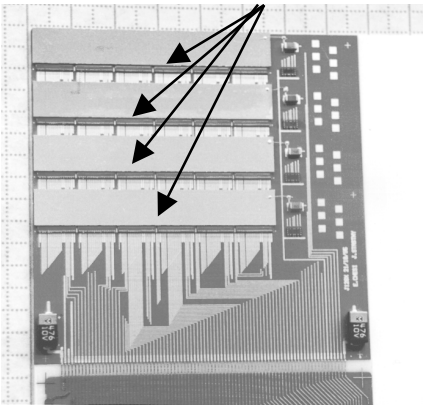
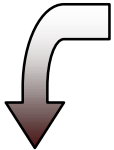


# Omega2 and Omega3 worked well (CERN RD-19, WA97 and NA57)

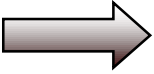
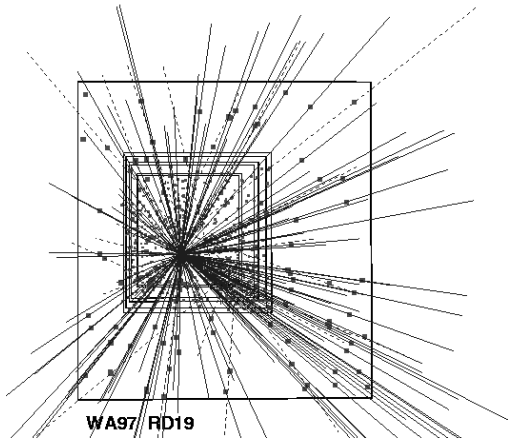


**LHC1 : 2000 CMOS readout channels**

**Pixel Ladders  
(6 chips)**



153 tracks through the Si Pixel Telescope

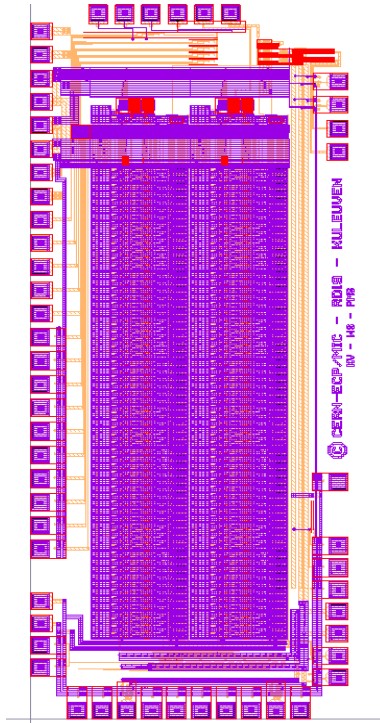


**Half plane ~ 50 000 sensing elements**

**WA97 NA57 Experiment  
1.2 M channels**

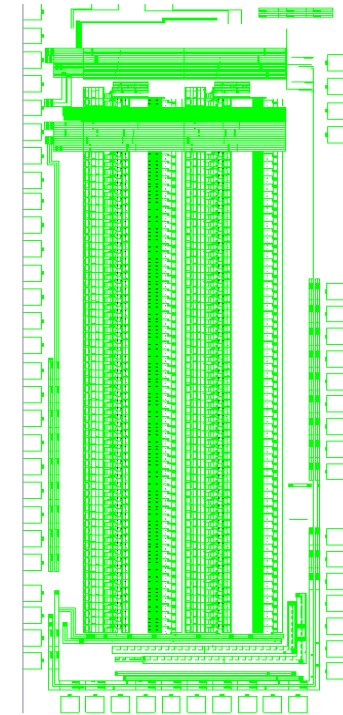
# Two test chips in commercial submicron CMOS

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- ◆ 2 columns of 64 pixels + 1 test pixel with analog outputs
- ◆ radiation tolerant layout
- ◆ 2 by 5 mm<sup>2</sup>
- ◆ full mixed mode circuit

LHC2TEST/ALICE1TEST  
0.5 μm CMOS  
25000 transistors

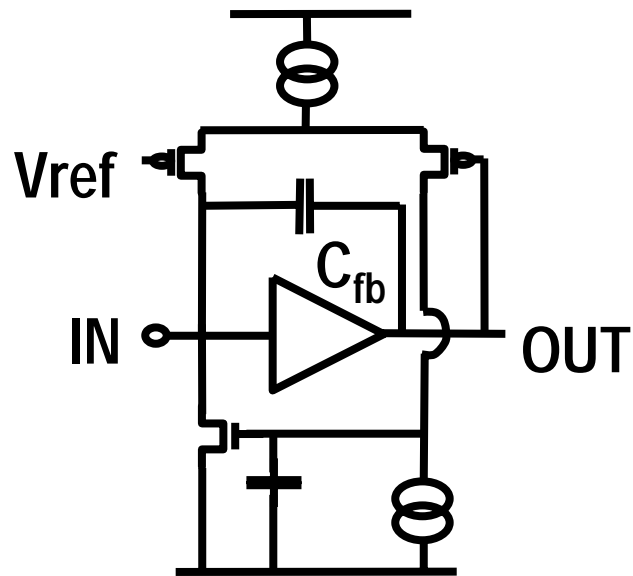


ALICE2TEST  
0.25 μm CMOS  
50000 transistors



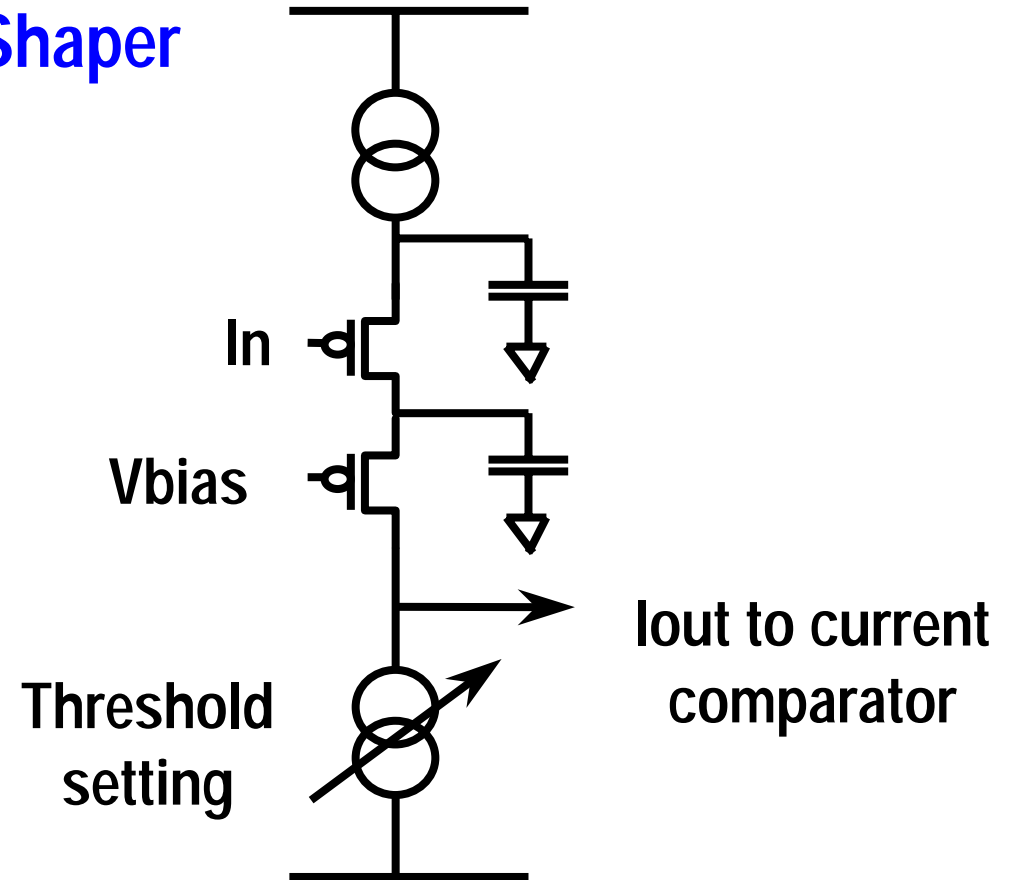
## Changes in front end

### Preamplifier



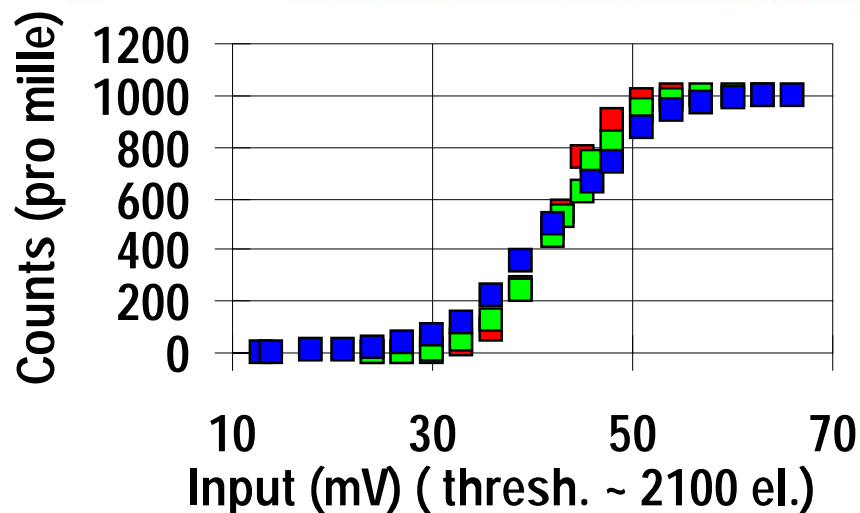
- ◆ DC level of input and output no longer coupled
- ◆ Leakage current compensation
- ◆ ref : F. Krummenacher, Nucl. Instr. and Meth., Vol. A305 (1991) 527-532

### Shaper



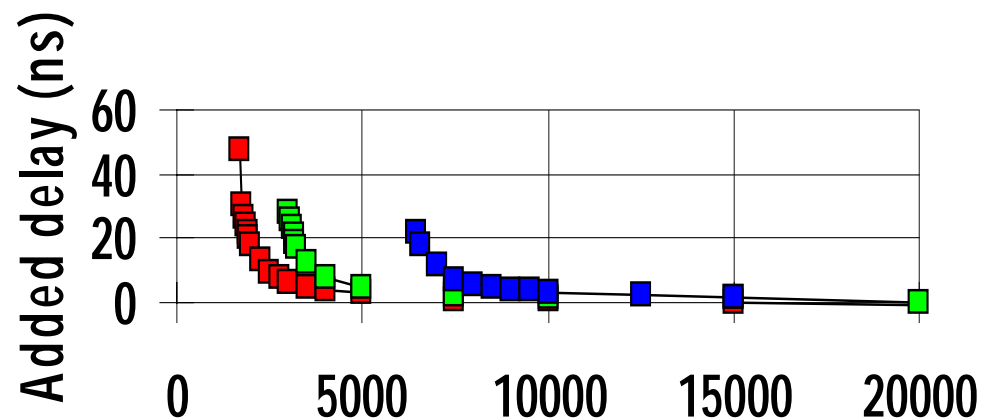
- ◆ Change in discriminator for speed, went to current comparator

# 0.5 $\mu\text{m}$ test chip



- $I_{\text{leak}} = 1.4$  nA, noise  $\sim$  180 e rms
- $I_{\text{leak}} = 16$  nA, noise  $\sim$  210 e rms
- $I_{\text{leak}} = 100$  nA, noise  $\sim$  330 e rms

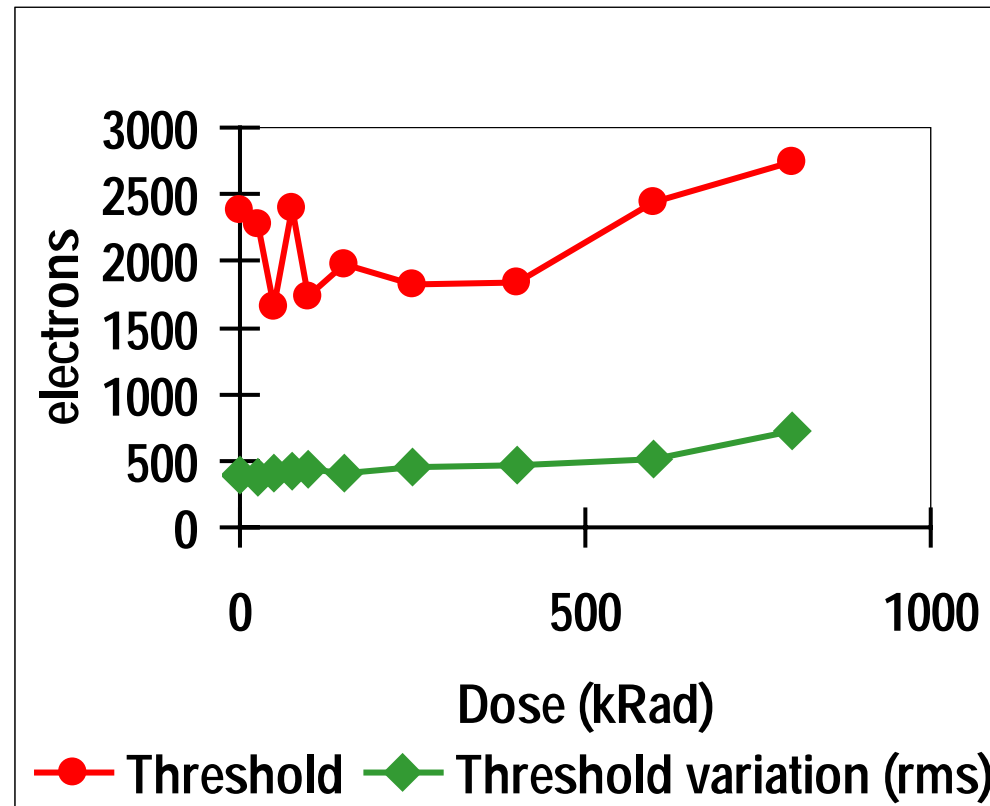
Leakage current compensation works  
(for both signs of leakage)



- threshold = 1650 el. ■ threshold = 2000 el.
- threshold = 6400 el.

Timewalk LHC compatible

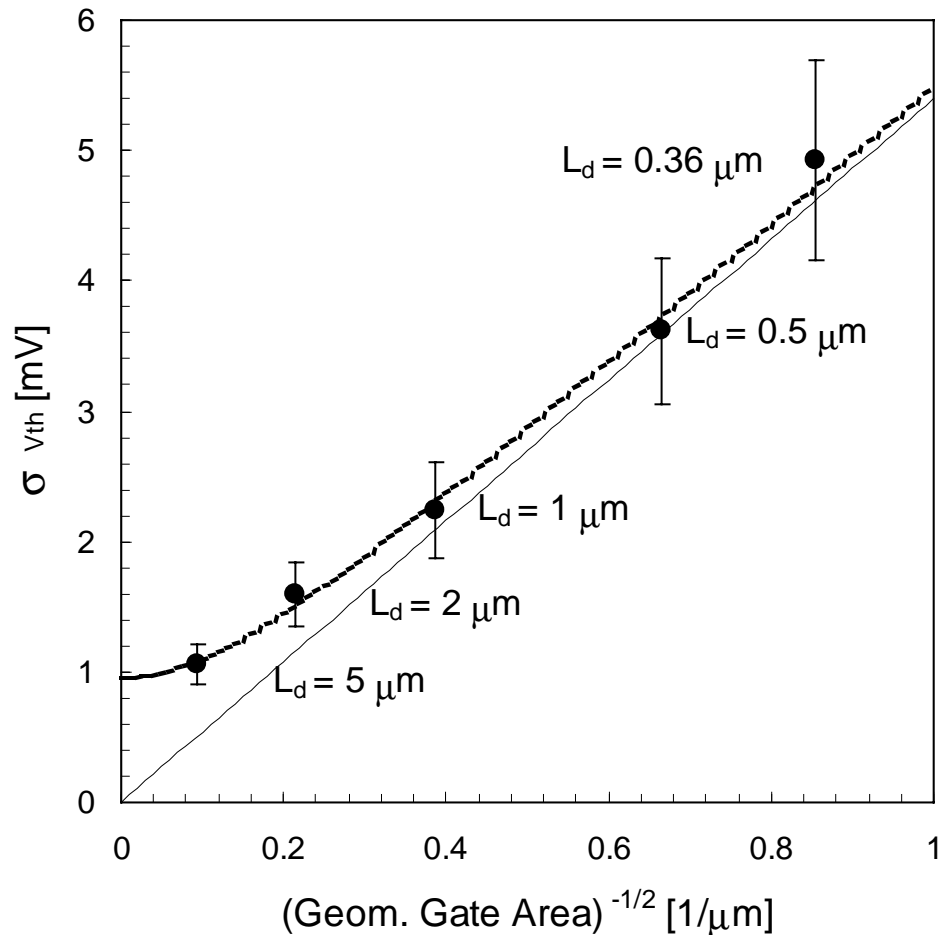
## 0.5 $\mu\text{m}$ test chip : evolution of Threshold and Threshold Variation with Xray Dose



**Supply currents virtually unaffected during the irradiation !  
Circuit dies around 1 Mrad because of transistor  $V_t$ -shifts  
which are still non-negligible in 0.5  $\mu\text{m}$**

**Confirmed for electrons, and for (cfr. F. Meddi et al.) gamma-rays and protons**

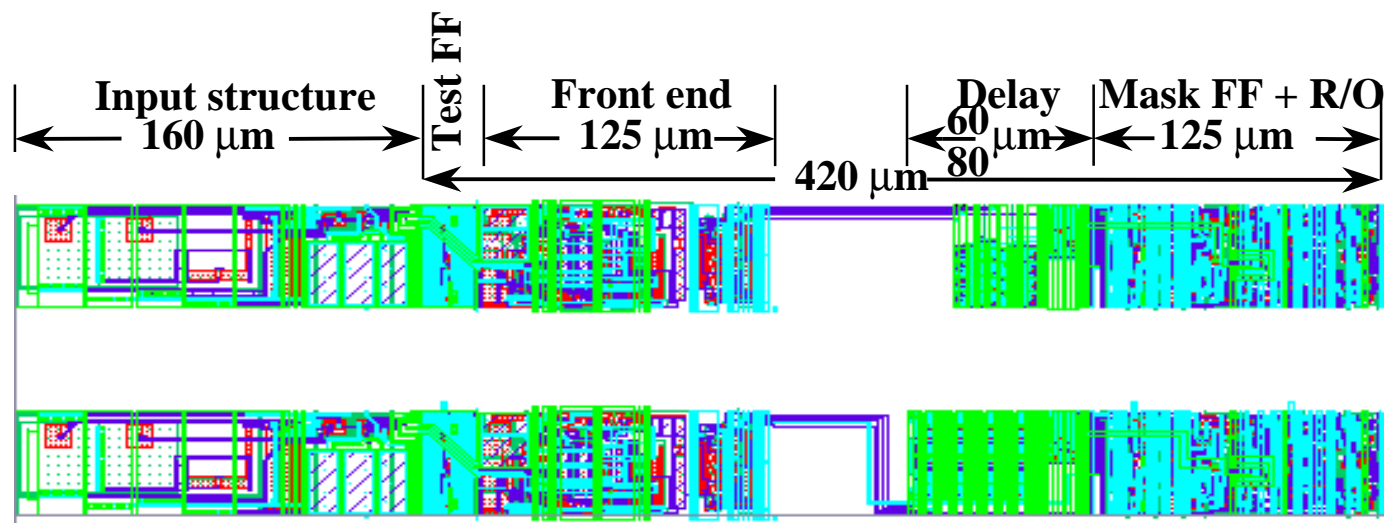
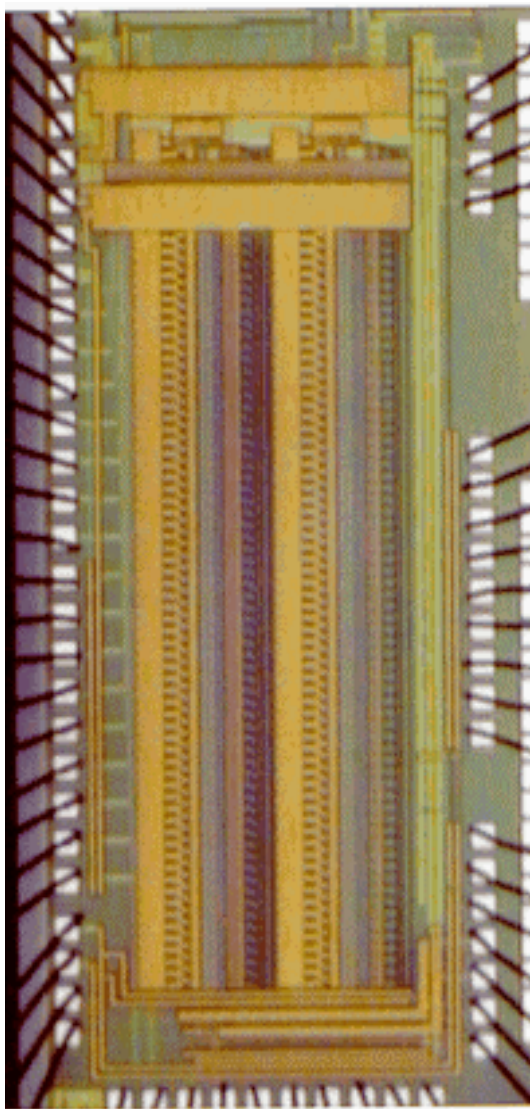
## 0.5 $\mu\text{m}$ test chip : conclusions



**Mismatch for edgeless transistors**  
cfr. G. Anelli et al.

- ◆ Threshold dispersion too large : edgeless transistor show much larger mismatch (see left)
- ◆ => need other front end topology
- ◆ Motivations to go deeper submicron :
  - Need more density
  - Will get even higher radiation tolerance
- ◆ Need for further modeling of edgeless transistors

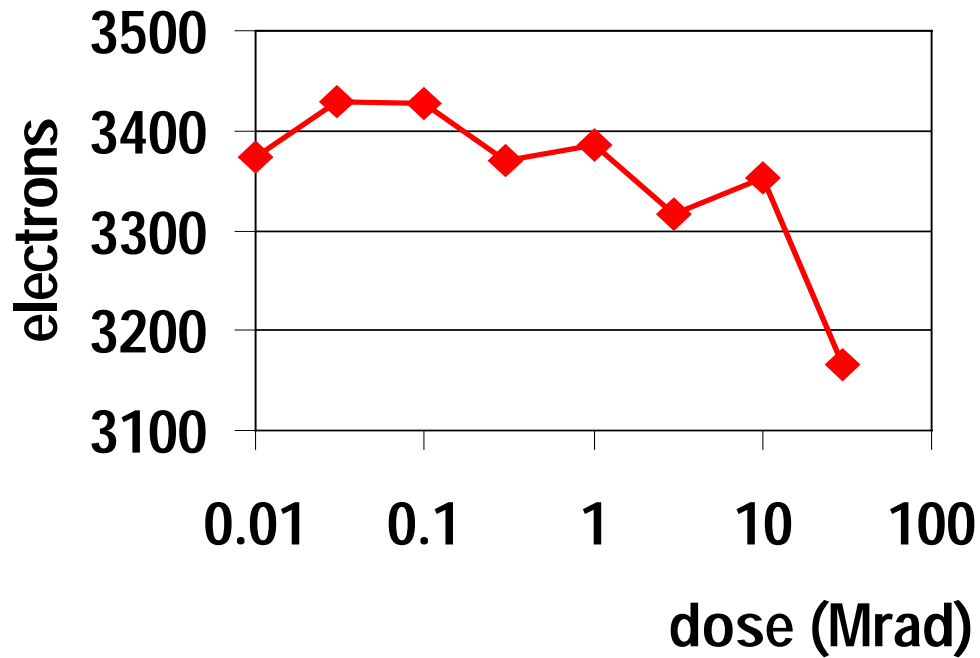
## 0.25 $\mu\text{m}$ testchip



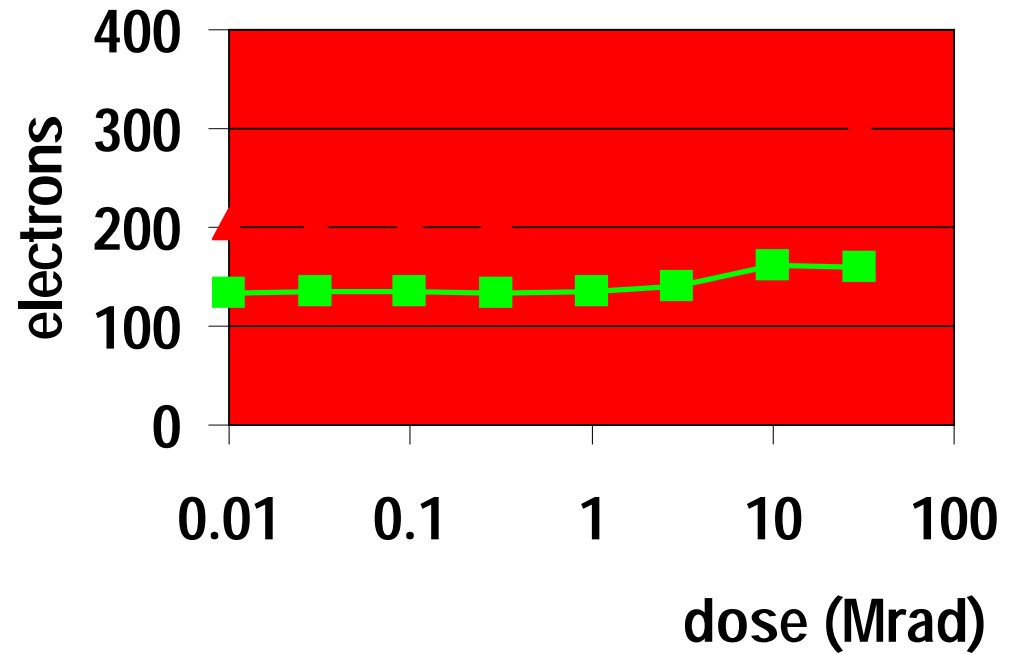
- ◆ Eliminated the current mirror (cfr ISSCC 2000) and shrunk the front end from 260  $\mu\text{m}$  to 125  $\mu\text{m}$
- ◆ Put synchronous delay (one column static, other dynamic) in the empty space and kept other logic identical to 0.5  $\mu\text{m}$  version
- ◆ 50  $\mu\text{W}$  per pixel
- ◆ Noise 220-250  $e^-$  rms
- ◆ Threshold dispersion 160  $e^-$  rms before 3 bit adjust, 25  $e^-$  rms after
- ◆ Used three metals only

# 0.25 $\mu\text{m}$ test chip : 10 keV X-ray Irradiation

## Pixel Threshold, Threshold Dispersion and Noise Vs Total Dose



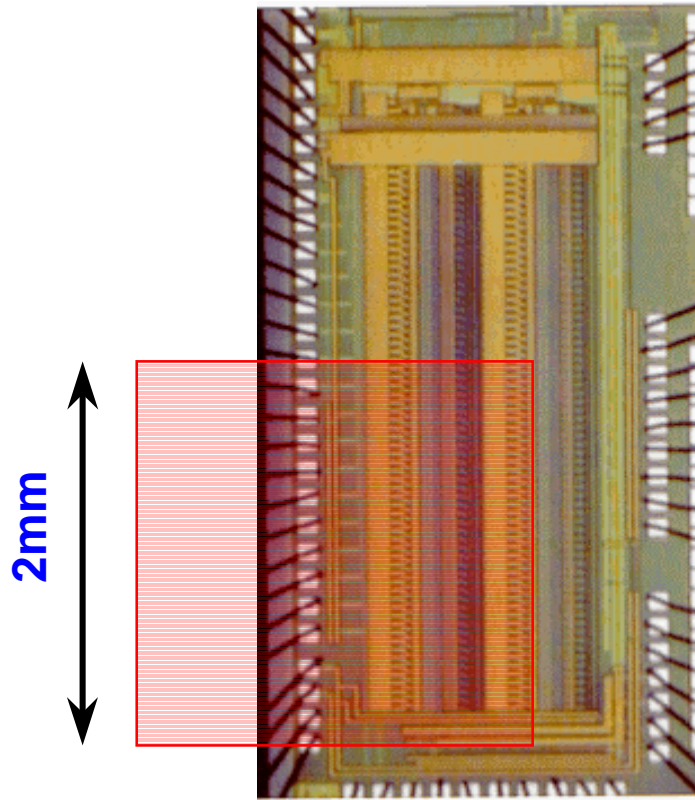
◆ average pixel threshold



■ threshold dispersion (rms)  
▲ noise (rms)

Supply currents virtually unaffected during the irradiation !

# Proton irradiation in NA50



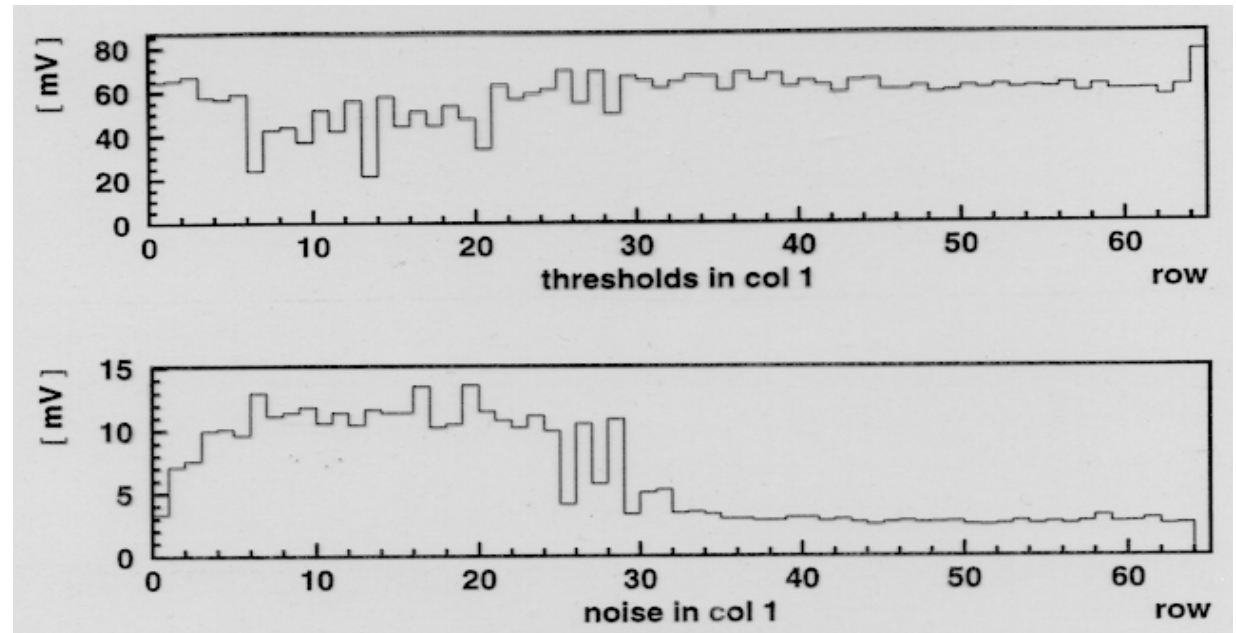
2mm

2mm

$3.6 \times 10^{13}$  protons/4mm<sup>2</sup>

=>

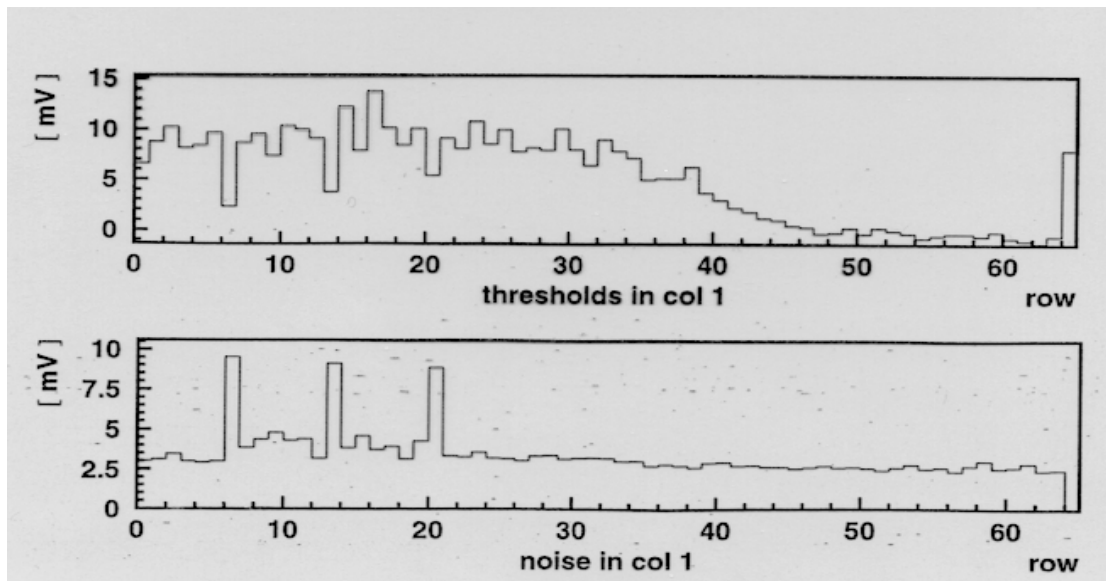
$9 \times 10^{14}$  protons/cm<sup>2</sup>



Threshold and noise on hit column  
after proton irradiation  
and 4 hour anneal @ room temperature  
(Note: 1 mV = 100 e<sup>-</sup>)

# Proton irradiation in NA50

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## Conclusions

- ◆ Also withstands non-uniform irradiation
- ◆ Did not see any evidence of hard failure, i.e gate rupture...

Threshold change and noise after proton irradiation  
and 20 hour anneal @ room temperature

Note: 1 mV = 100 e-



# Conclusions from test chips

## Challenges for full chip

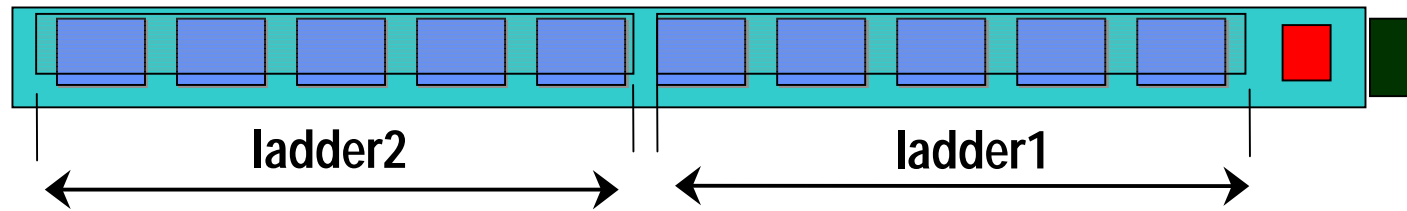
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- ◆ Speed, threshold uniformity and radiation tolerance (total ionizing dose and single event upset) proven
- ◆ Need to further characterize enclosed devices
- ◆ Challenges for full readout chip :
  - Architecture for two different applications
  - Large occupancy in LHCb, need to minimize dead time
  - Readout (=digital activity) while being sensitive
  - Large chip
  - Large system : testability, uniformity
  - Design for radiation tolerance : design implications revisited

## Two applications : pixel for tracking/vertex finding in ALICE

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### Half Stave

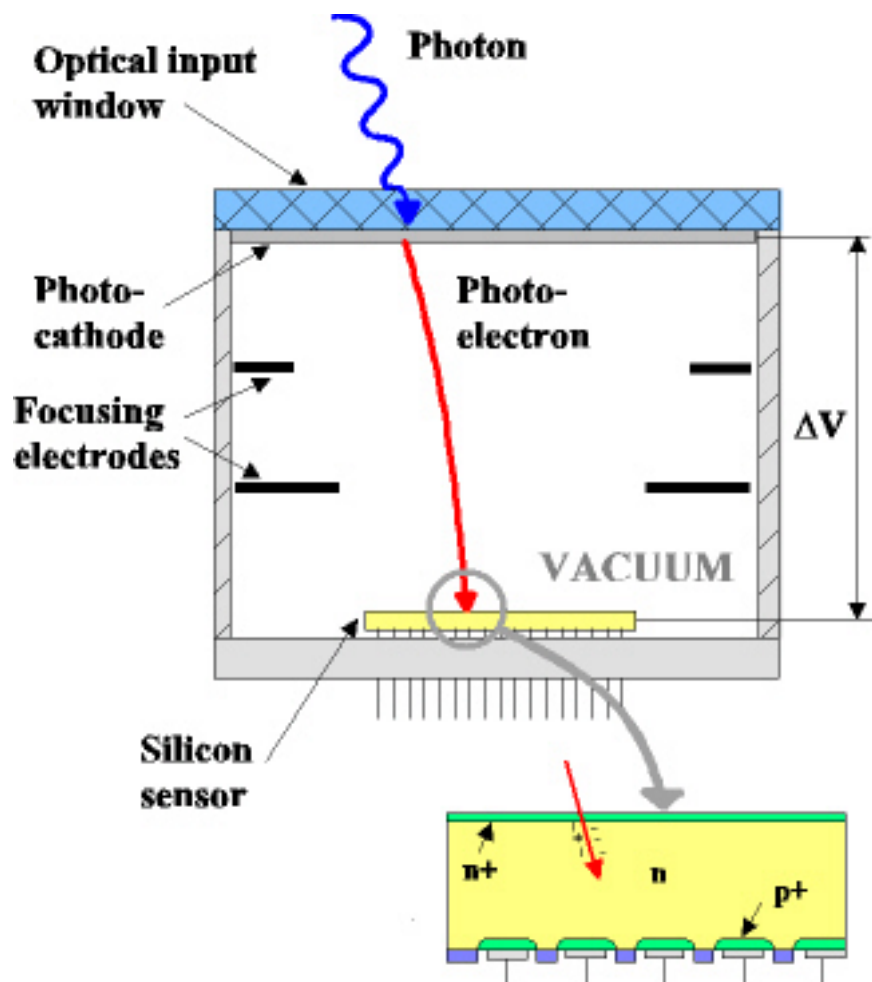


**10** chips of one **half-stave** read out sequentially in  $400\mu\text{s}$

**120** **half-staves** read out in parallel

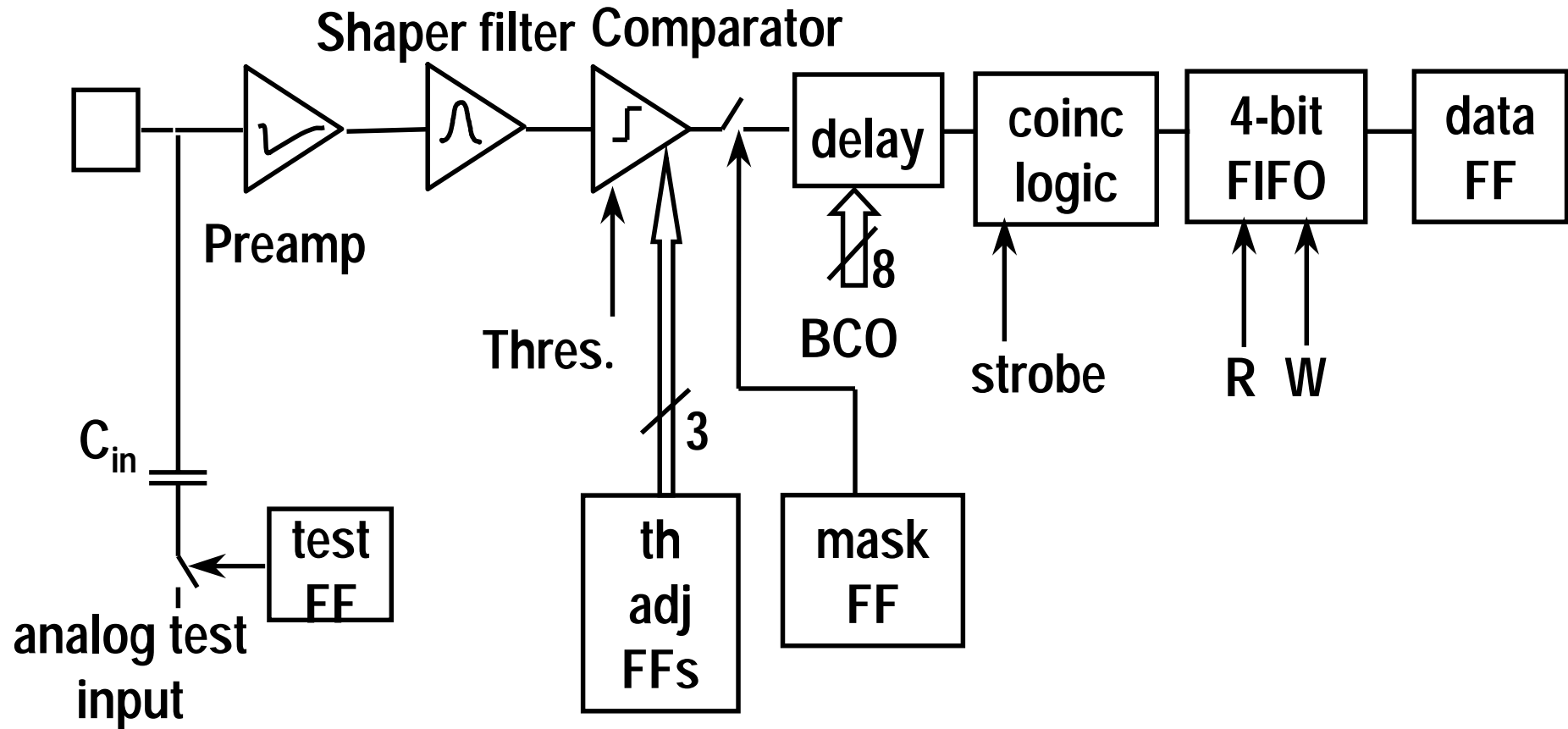
- ◆ Minimal mass, thin sensors => 12 000 e- most probable signal
- ◆ Spatial resolution of  $12\mu\text{m}$  in  $r\text{-}\phi$  =>  $50\mu\text{m}$  pixel pitch
- ◆ 1% average occupancy
- ◆ Level-1 trigger : latency of  $5.5\mu\text{s}$ , few kHz rate, buffering on chip
- ◆ Full event readout in  $400\mu\text{s}$  (deadtime about 10%), 10 MHz clock
- ◆ Radiation tolerant to  $\sim 500$  krad

## And... LHCb RICH : encapsulation of pixel chip-sensor assembly in HYBRID PHOTON DETECTOR for particle ID



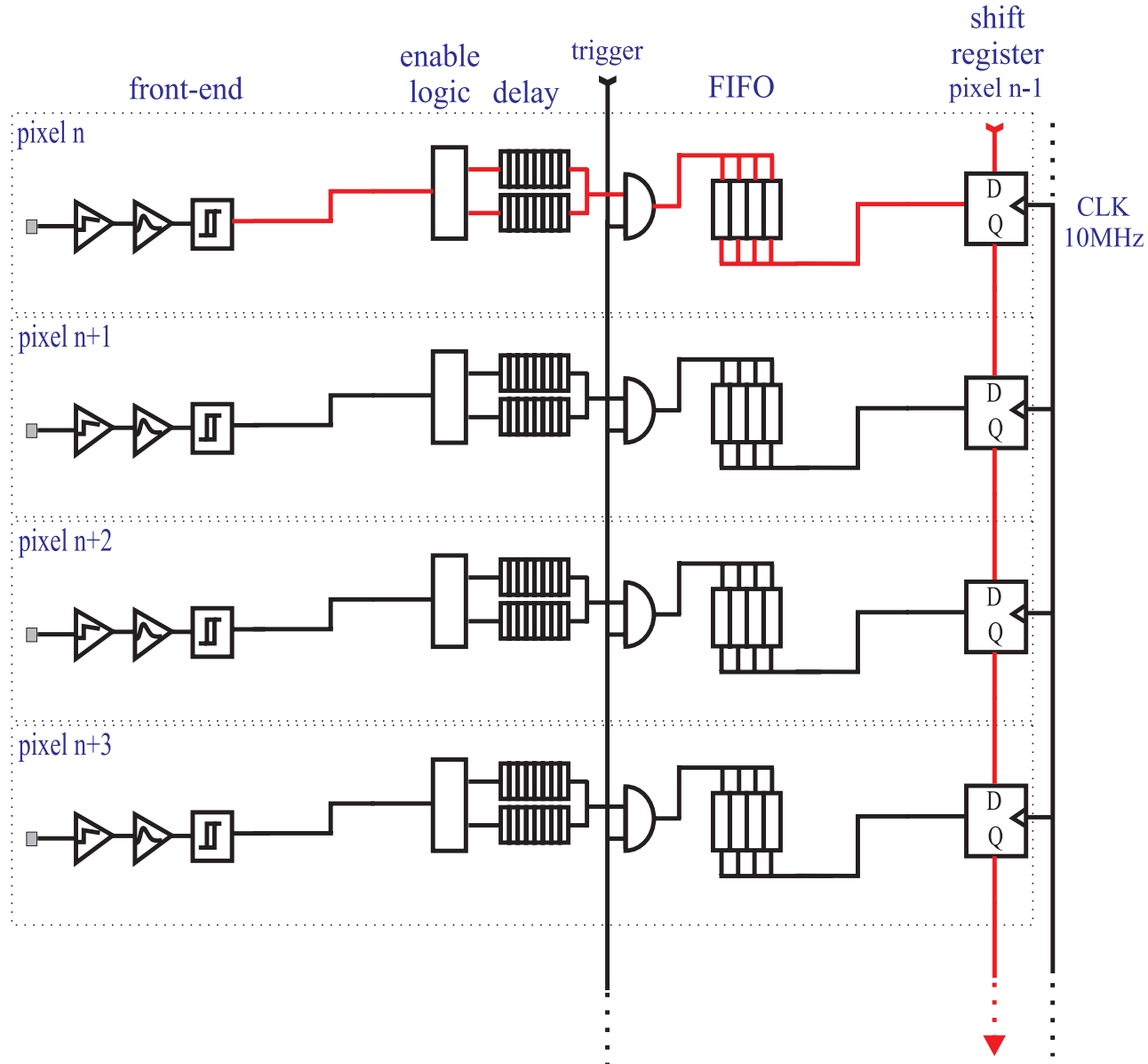
- ◆ Single photons yield 5000e<sup>-</sup> signal with 20kV accelerating potential
- ◆ 2.5mm x 2.5mm channel size, 5 x demagnification => 500 $\mu$ m  $\times$  500 $\mu$ m granularity
- ◆ 8% maximum occupancy
- ◆ 40 MHz event rate, also readout clock
- ◆ 1MHz average Level 0 trigger rate
- ◆ Buffering of Level-0 triggered events (latency of 4  $\mu$ s)
- ◆ Readout of triggered event in 900ns (deadtime  $\leq$  1%)

# New 8000 channel chip : pixel

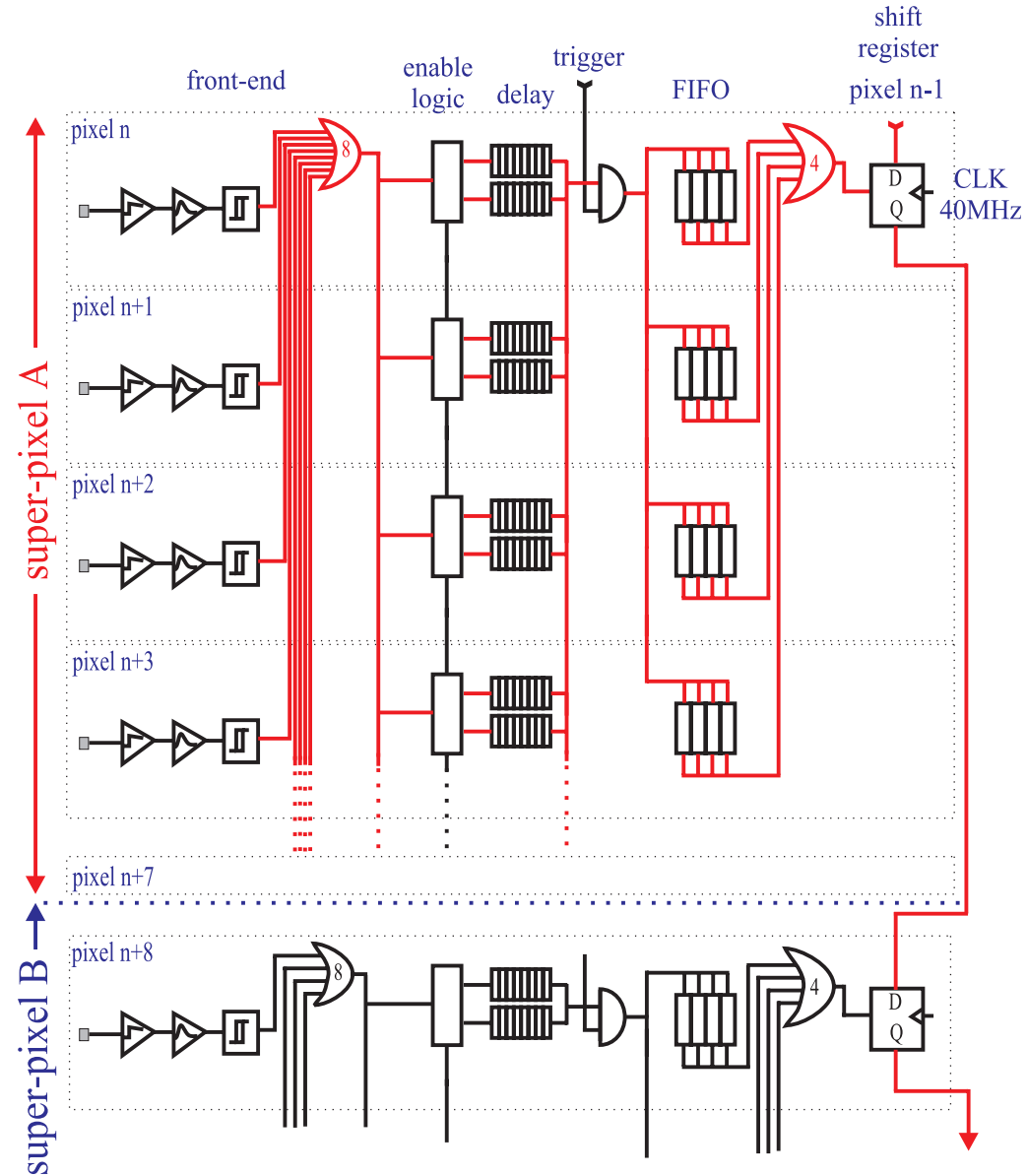


# Two applications : architectural solution

## ALICE mode of operation

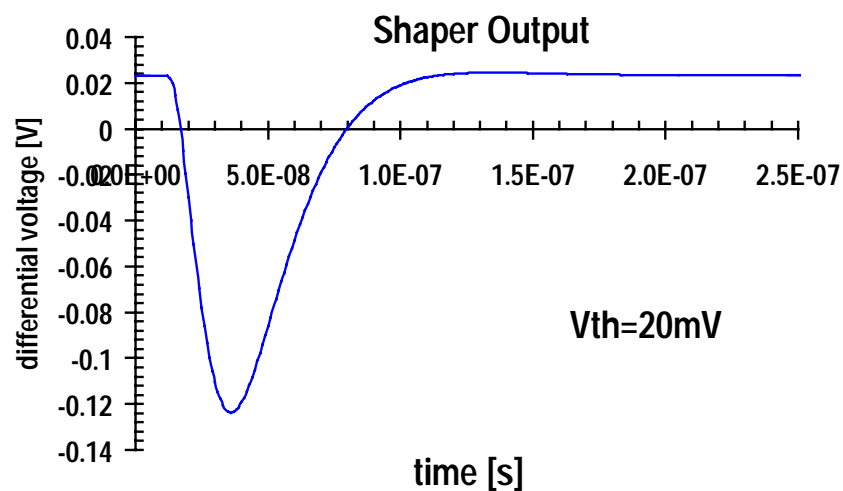
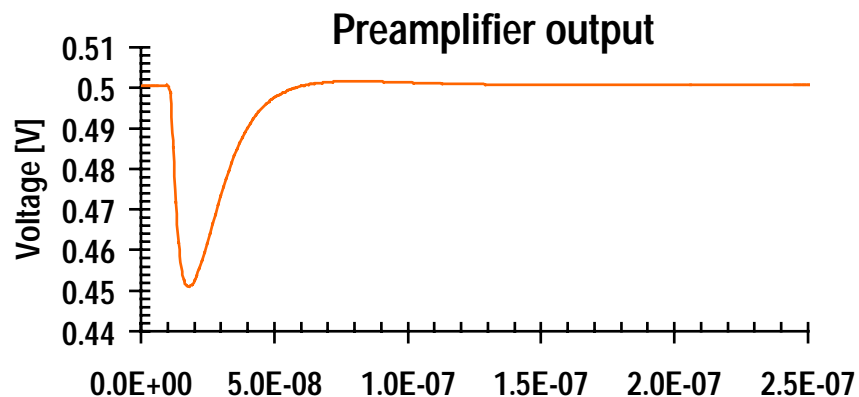


# Two applications : LHCb mode of operation



# FRONT END

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- ◆ Differential to reject substrate and supply noise
- ◆ Closed loop complex poles for fast return to zero to be immune to pile-up of subsequent signals

## Pixel Cell : digital part

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### Delay :

- stores a hit for duration of trigger latency
- latches the time-stamp of a hit from a periodic Gray-encoded pattern (modulo  $n$ ) on an 8-bit bus

### FIFO :

- Read/write addressable by Gray encoded bus

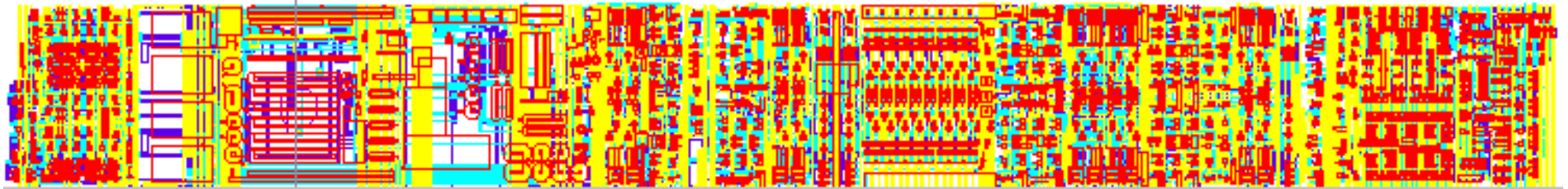
Risk of switching noise coupling into analog circuitry is reduced by:

- Gray encoding of patterns on busses
- Current starved logic cells



# Pixel cell

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- ◆ 125 $\mu$ m
  - ◆ pre-amp (differential)
  - ◆ shaper (differential)
  - ◆ discriminator (+ fast-OR)
  - ◆ 60 $\mu$ W static consumption
  - ◆ 265 $\mu$ m
  - ◆ two digital delay units
  - ◆ trigger coincidence logic
  - ◆ 4-event FIFO buffer
  - ◆ readout logic
  - ◆ 35 $\mu$ m
  - ◆ 5 un-upsettable latches for configuration
    - test input on/off
    - pixel mask on/off
    - 3 bits of threshold adjust
- 6 metal layers**  
**1500 transistors/pixel**  
**layout for radiation tolerance everywhere**

## Periphery and I/O

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- ◆ Periphery contains:
  - **Counters** to generate timestamp
  - **Counters** to address FIFO buffers
  - **8-bit DACs** to provide voltage and current references for analog circuitry and current-starved logic
- ◆ I/O pads :Single-ended : Gunning Transceiver Logic (GTL)
  - Low swing
  - Slew rate control
- ◆ **Separate supply** for output buffers
- ◆ **Multiple bonding pads** for supply lines to reduce inductance and limit on-chip power supply bounce during switching

## Design for testability

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- ◆ Configuration of peripheral logic and pixel cells by means of JTAG serial interface -
  - allows both **write** and **read** of configuration settings (test,mask...)
  - **reading back** of analog levels (currents & voltages) generated by DACs
  - **connectivity tests** of chips on stave using boundary scan allows detection of **bad chips** on stave
- ◆ Every pixel can be addressed individually for testing using analog input

## Very important fine print

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- ◆ **Single event effects :**
  - **Single event induced latch-up : radiation tolerant layout very effective also here**
  - **Single event upset : special SEU hardened flip-flops**
- ◆ **Power distribution and voltage drops :**
  - **Motivation for (late) decision to switch from 5 to 6 metal layers**
  - **Local mirroring of sensitive biases to reduce sensitivity to on-chip resistive drops**
- ◆ **Digital to analog cross-talk :**
  - **Slew rate control on all digital**
  - **Differential frontend**

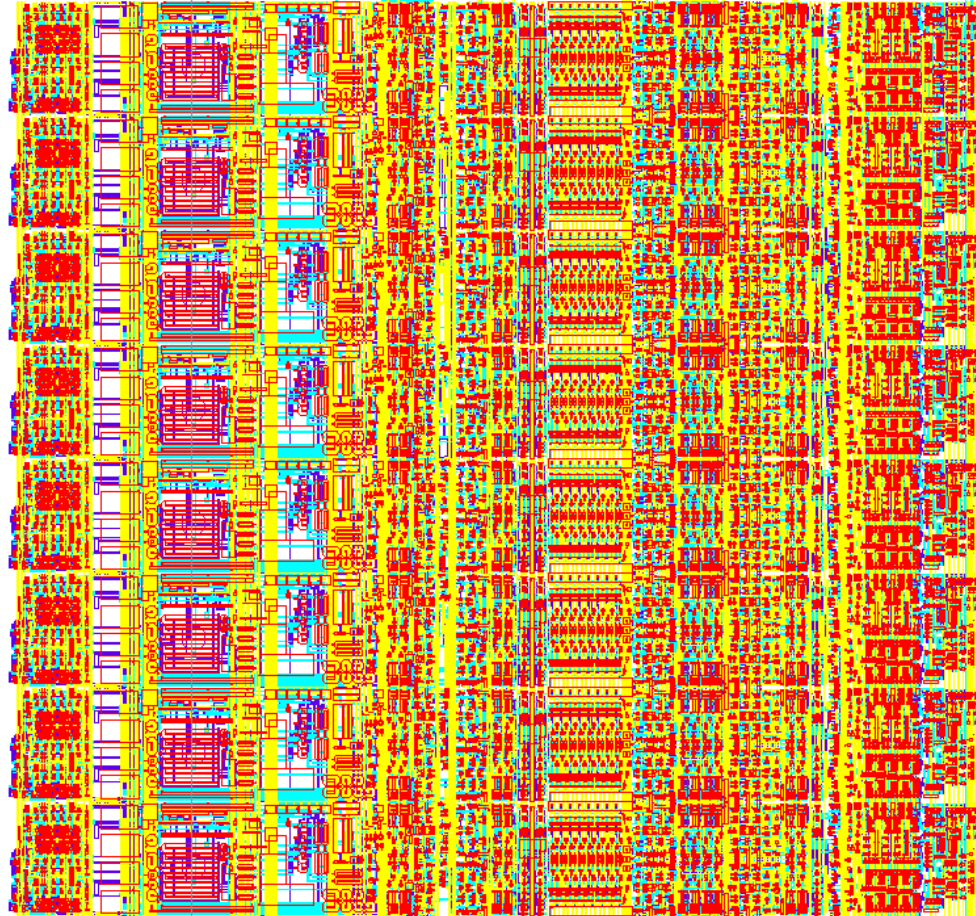
# Conclusions

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- ◆ Experience from omega2 and omega3/LHC1, and from the two test chips
- ◆ Commercial deep submicron CMOS allows :
  - High component density
  - Radiation tolerance
  - Good speed-power performance
- ◆ Full scale pixel readout chip designed
  - One chip for Alice pixel vertex and LHCb RICH
  - 8000 readout channels
  - 13 M transistors in 14 by 16 mm<sup>2</sup>
  - 6 metals
  - Testability and system integration
  - Uniformity
  - Important fine print

# Conclusions

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**Basic building block in full readout chip :  
8 pixels/12 000 transistors in 400 by 425  $\mu\text{m}^2$**