BaBar IFR
The IFR Crate Controller

Preliminary

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1 Introduction

The Instrumented Flux Return (IFR) detector of the BaBar experiment is made of Resistive plate Chambers (RPC). The passage of particle through the gas, induces a signal in the external strips. Each chamber is equipped with two orthogonal layers of strips and only digital information will be recorded. The readout of IFR can be divided in three parts: the first one is the Front End Card (FEC) where the data is digitized and read when L1 trigger arrives. The second part is the Front End (FE) crate, located around the Magnet, where are installed some IFR module used to store the data until the DAQ can read them. In total there are 8 crates, 4 for the barrel and 1 for each half endcap door. The last part of the electronic chain is the ReadOut Module (ROM), a common BaBar board used by all the detectors, with a powerful CPU and large memory banks where the IFR data will be sparsified and encoded.

2 Overall Description

In Front-End crate up to 16 boards of different kind, can be installed; the IFR FIFO (IFB) to store data until it will be read by DAQ system, the IFR Calibration Board (ICB) to send test pulse to the Front End Cards, the IFR TDC Board (ITB) to measure the bunch crossing time and the IFR Crate Controller (ICC). This board is connected to ROM via the G_link to receive the BaBar protocol commands and to send the data. A custom point-to-point backplane has been designed to connect the ICC to each of the 16 board with 3 lines, data-in, data-out and the 59.5MHz clock.

3 ICC Functional Description

In the BaBar DAQ project all the detectors must be synchronized with the $59.5MHz$ system clock; the time stamp, generated by this signal, will be used to check the data consistency and to build the events. The ICC must guarantee the clock and data distribution to the 16 boards of the crate with a jitter less than $\pm 0.5ns$. Unfortunately the use of high performance clock drivers does not guarantee free trouble operation. Only careful board layout and consideration of system noise issue can guarantee reliable clock distribution.

A block diagram of the ICC is shown in Fig 1. The PCB is a 8 layer board, 3 layers are used to supply +5V, -5V and -2V together with 12V . The remaining 5 layers are used for signals, all the lines are at controlled impedance of 50Ω or 100Ω. In Tab(1) there is the list of the components mounted in the board.

3.1 The G_link

The Finisar transceiver module FTR8510 is the physical interface with the optical link. It can guarantee a low cost and high reliability data link up to $1.5Gb/s$ for applications less than a kilometer in length.

The $HDMP - 1012$ transmitter and the HDMP-1014 receiver are used to serialize deserialize the data. The serial data of T/R link are selectable in four range and extends

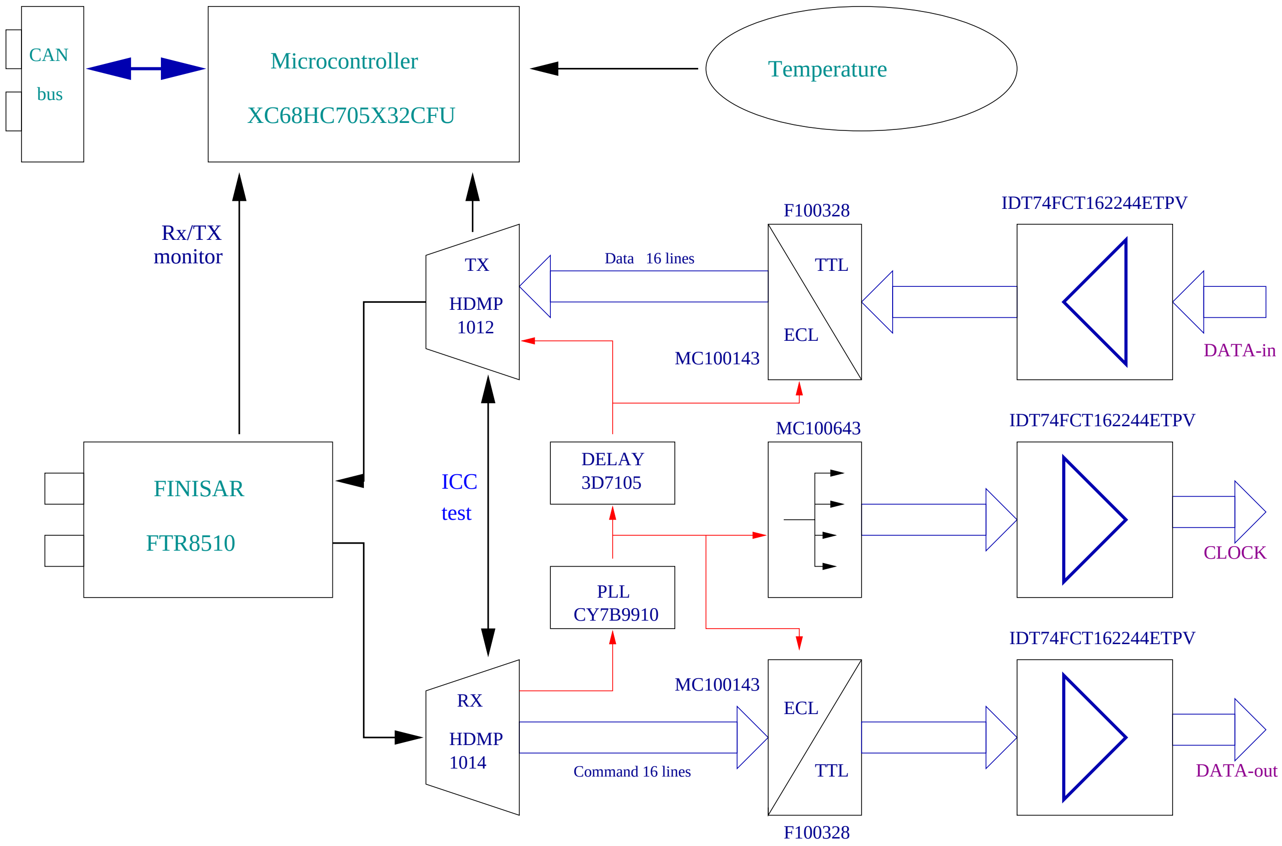

Figure 1: Block diagram of the ICC Module

from $120 Mb/s$ up to $1.25 Gb/s$. In current application the parallel data interface is 16 bit single ended ECL.

The HDMP-1014 receiver is used to convert the signal sent from a $HDMP - 1012$ (in the ROM) into 16 bit wide parallel data. In doing this, it performs the function of:

- Clock recovery
- Data recovery
- Demultiplexing
- Frame decoding
- Frame synchronization
- frame error detection
- Link state control

The $HDMP - 1012$ is used to accept 16 wide parallel data and transmit it over a high speed serial line. In order to accomplish this task the $HDMP - 1012$ perform the following functions:

- Parallel word input

Component	name
Optical Rx/Tx	FTR8510
HP mult	HDMP-1012/1014
PLL	CY7B9910
DELAY	3D7105
Line driver	IDT74CT162244CT
Clock distrib.	MC100EL14DW
ECL/TLL Clk driver	MC100H643
ECL/TTL/ECL	MC100EL24/25
Microcontroller	68HC705X32

Table 1: ICC part used

- High speed clock multiplication
- Frame encoding
- Frame parallel to serial multiplexing

The T/R chips are connected in full duplex configuration. The 5Vdc power supply line to the transceiver module FTR8510 is derived from 12V power line on the backplane to guarantee low level noise.

3.2 The Clock Distribution

At the exit of HP receiver the clock is recovered using the PLL CY7B9910, then delayed with Silicon Delay Line 3D7105 to wait the data coming from the backplane and then fed into the HP transmitter module. The same clock signal must be distributed to the 16 lines of the backplane together with the commands. The Hold Register MC100E143 is used to validate the data with the clock signal before the ECL/TTL conversion. The 16-Bit Buffer/Line driver 74FCT162244 is used to inject signals and clock into the backplane, this chip is required for application of high speed and low power dissipation. The same chain is used when the data is read from the backplane and prepared for the transmission.

3.3 The microcontroller

The microcontroller MC68hC705X32CFU is used in the board to monitor the status of transceiver module and to read the temperature inside the crate. A unique control system is built into all FINISAR chips. This system provides real-time control of the optical link as well as status reporting and diagnostic. This control system is interfaced with the microcontroller to monitor continuously status and optical performance of the link. Through the serial communication port the chip provides to the microncontroller link status information, optical power level, drive current, bias voltage, and transmitter temperature. All this data together with two values of the temperature will be available to detector control on the CAN bus port of the microntroller. In tab(2) there is the list of CAN commands used from the ICC to monitor the G_link status. One of the temperature value is available through a general purpose open collector output in the board front panel to be connected to the SIAM module in the electronic house.

CAN Code	FINISAR Code	Description
16		Read T sensors
17		RFD,SYS-STATUS,SIG-DET
18	37,40,48,49,50	Calibr. Value
19	32,33,41,42,43,44	Module ID
20	34,35,36,38	TX Status
21	39	RX Status
22	45, 46, 47	System Status

Table 2: FINISAR Monitor: CAN code Command

4 The backplane (PDB)

The design of this board requested a special care to guarantee the delivery of signal and clock at $59.5MHz$ within the requirements of the BaBar DAQ system. The "stripline" technology, used for prototype backplane, gave results well within the BaBar specification.

The Point-to-point Distribution Board (PDB) is a 21 slot backplane for standard VME crate, 17 slots are used by DAQ IFR boards. The remaining 4 slots are used to power IFR trigger boards. The signal are located on J2 connectors, A-C rows, the B row is used for power and ground. The first position is used for ICC card. All the 48 lines have the same length (14.8" ± .1") to minimize the skew between the lines. The PDB can be used to transmit single-ended signals (TTL or ECL). In Fig 2 the structure of the PDB is showed, the signal lines have controlled impedance (50Ω), the low voltage (-2V, +5V, -5V, 12V) and ground lines are on different planes. In total there are 9 planes. The signal Command lines exit from the ICC and not used can be terminated on the backplane, the data lines entering into the ICC are terminated in the crate controller. Termination on the PDB could be resistive or AC coupled. In table 3 the values of the stripline used to get the 50Ω impedance lines are showed:

Name	value
Line width	$0.305mm$
Cu lines thickness	$35\mu m$
Fiberglass type	FR4
Propagation Delay	2.16ns/ft
Dielectric const.	4.5

Table 3: Value of STRIPLINE technology

5 The Front-End Crate

The Fe crate is a standard 6U crate by WIENER company with our custom PDB mounted in J2 position. The crate consists of power supply (UEP5020) for +5V,-5.2, -2V and +12V, Plenum bin (UEV5022) and the 3U special BaBar fan tray. The remote control, based on CAN protocol, allows the monitor of the following parameters in addition to the remote on/off and SYSRES (VME):

- All voltages.
- All current limits.
- Over and Under voltage trip off points.
- Overcurrent trip off points.
- Temperature measuraments:
    1. Power supply.
    2. Fan Tray air inlet.
    3. Air outlet temperature on top of slot 1.
- Status signal.
- Avarage speed of the fan and display of every single fan speed.
- Identification of the crate.
- Configuration and adjustment.

If any error (fan failure) is detected a high priority message is transmitted from the CAN interface.

6 Test Setup

The test bench shown in Fig 3 has been used to test the prototype boards of IFR DAQ modules. The same setup will be used to validate the final production of the electronics.

It consists of 4 minicrates with 16 FECs each, and the crate populated with the ICC, 4 IFBs and 1 ICB. The data are read from the crate into the ROM via 40m optical fibre and stored in UNIX station. A second ICC is used close to the old ROM as personality board to allow the connection with the optical link.

During normal test the calibration signal is sent from the ICB to the FECs, after the trigger latency of 11.5, with L1 trigger command the FEC data are read into the IFB. The RDE (Read_Event) command provokes the transport of data from IFB to the ROM.

With this kind of test it is possible to test the signal and clock propagation from ICC to IFB and ICB and the correct behaviour of the boards.

It is important to stress that in this particular setup the noise conditions can be worse than in final system due to the special use of the old ROM together with the ICC.

Lines that require controlled impedance are placed on layers 2, 4, 6 and 8. The other planes are used for gnd and low voltage.

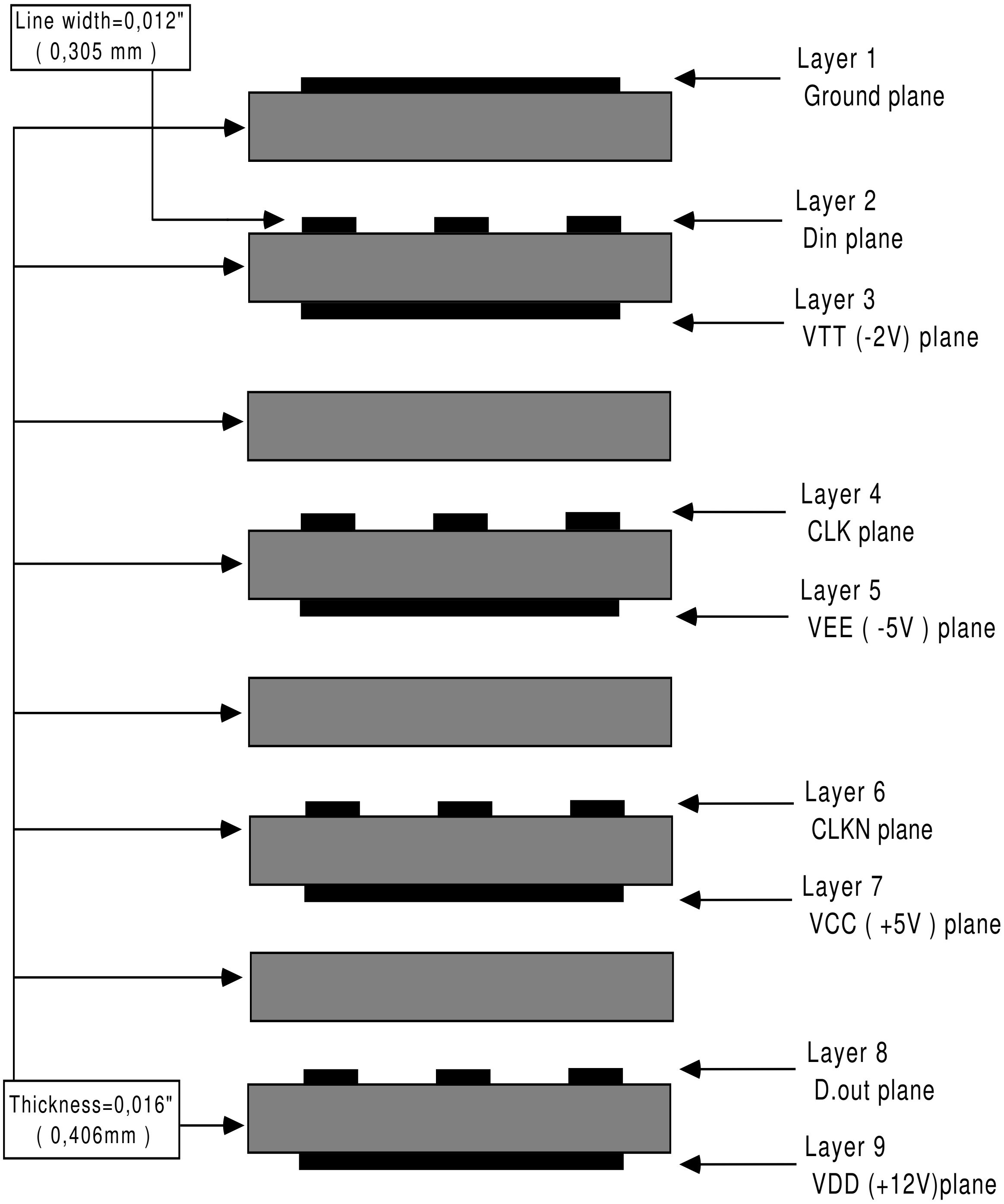

Figure 2: Stripline structure

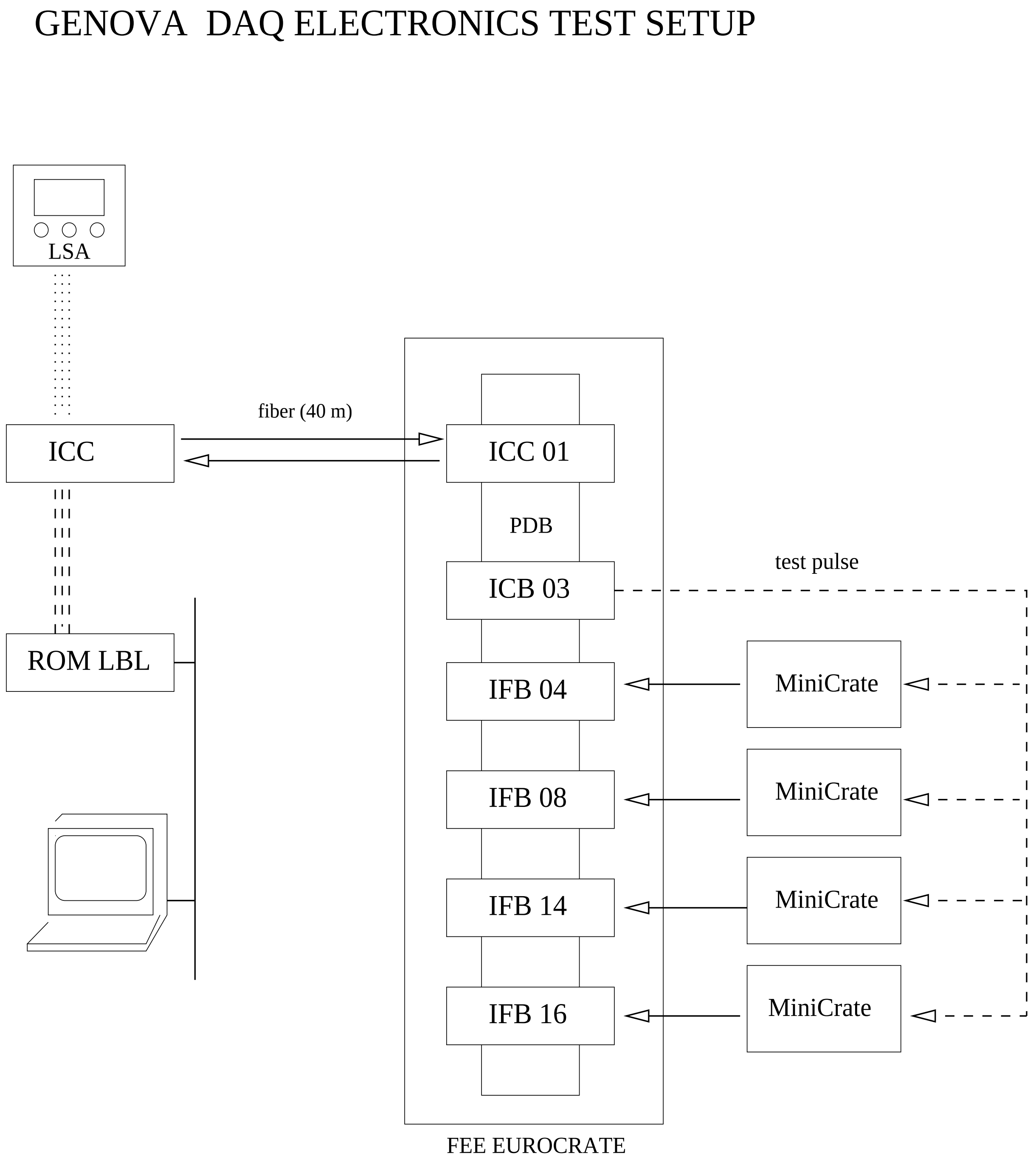

Figure 3: DAQ Test Setup