

# A 96 channels, 500 ps resolution TDC board for the *BaBar* experiment at SLAC



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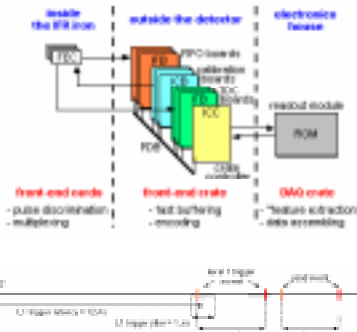


## Abstract

A TDC board has been designed and built to complete the readout of the Instrumented Flux Return of the BaBar experiment at the Stanford Linear Accelerator Center. The board has 96 input channels and makes use of 3 multi-purpose TDC chips designed at CERN, with time resolution up to 500 ps and configurable via a Test Access Port (IEEE standard 1149). Data are stored before readout in a multi-event buffer. Communication with BaBar DAQ system is realized through 3 serial lines on the backplane connector. All the logic, including internal registers and the interfaces with the BaBar protocol and the TAP controller, is implemented in two fast FPGAs. The board is designed to work at 59.5 MHz clock frequency.



Instrumented Flux Return

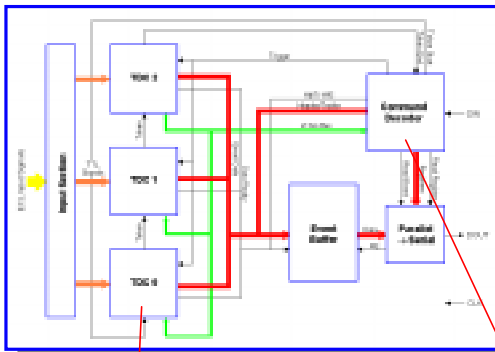


The *Instrumented Flux Return (IFR)* is one of the 5 major subdetectors building up the *BaBar* apparatus on the *PEPII e<sup>+</sup>e<sup>-</sup>* collider at SLAC. Its active part is made up of *Resistive Plate Chambers (RPCs)*, whose signals are read out by means of ~50,000 aluminum strips. Timing of these signals is useful for prompt bunch crossing determination, pattern recognition and noise rejection.

The *ITB (IFR TDC Board)* has been developed for this purpose and is part of the IFR front-end electronics; this is installed right outside the detector and is connected via a 1GHz optical link to the DAQ system inside the *BaBar* electronics house.

To serve its purpose, the ITB has to fulfill several requirements:

- it must have good time resolution, at least as good as the intrinsic RPC resolution of ~1 ns. This is necessary to deal with the close spacing of *PEPII* bunch crossings (4.2 ns).
- it has to comply fully with *BaBar* data transmission protocol, which makes use of 3 serial lines (a 59.5 MHz clock line, a command/data-in line and a data-out line) and a set of commands with related timing specifications.
- it must be able to work in the same VME-like crate as the other IFR front-end boards,, sharing the same custom backplane (*PDB*).



Simplified block diagram of the ITB

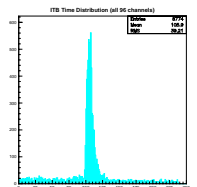


## Specifications

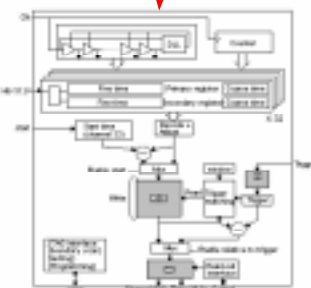
Input Signals	ECL diff. (96 channels)
Operating Clock Frequency	59.5 MHz
Time Bin Size	525 ps (= $T/32$ )
Dynamic Range	21 bit (1.1 ms)
Data Bus	32 lines
Event Buffer Size	512 × 32 (> 5 full sized events)
Communication	<i>BaBar</i> protocol (3 serial lines) on custom VME-like backplane
Maximum Trigger/Readout Rate (for full sized events)	58.5 kHz
Registers	3 configuration (128 × 1), 3 mask (32 × 1), 3 error (32 × 1)
Configurability	"trigger matching" window offset and width; trigger time subtraction flag; global offset; single channels offset; channel masks.

## Main components

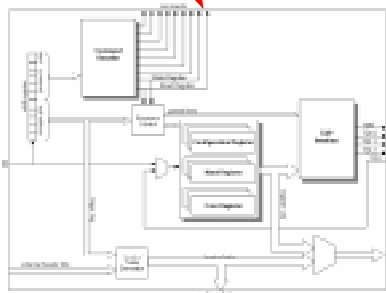
- TDC:** CERN 32 channel multi-purpose TDC
- Clock frequency: 20 MHz to 60 MHz
  - Time bin / dynamic range: 0.52 ns at 60 MHz / 21 bit
  - Highly configurable via JTAG Test Access Port
- Logic:** Xilinx XC4006E-1 and XC3142A-1
- Ultra-high speed FPGAs
  - Number of logic cells: 256 (XC4006), 144 (XC3142)
  - On-chip synchronous RAM (XC4006)
- Event Buffer:** Texas Instruments SN74ACT3631-15
- 512 × 36 clocked dual port FIFO memory
  - Clock frequency: up to 67 MHz
  - Independent clock for the two R/W ports



ITB time distribution for a *BaBar* cosmic rays run. The peak width is mainly due to the jitter of *BaBar* trigger.



Block diagram of the 32-channel CERN chip



Block diagram of the ITB Command Decoder / Registers / TAP Interface logic (XC4006E-1)