DESIGN AND PERFORMANCE OF A MULTICHANNEL MULTISAMPLING ANALOG TO DIGITAL CONVERTER BOARD FOR ENERGY MEASUREMENT

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1 ABSTRACT

This paper describes a VME multichannel multisampling ADC board designed for low energy physics experiments. To guarantee the maximum experimental flexibility the module is completely programmable through a Digital Signal Processor and a program register accessible via VME bus. With the frequency 40 MHz the single channel can acquire a variable number of samples of each analog input. Besides, it is possible to use the board as a 160 MHz waveform digitizer, grouping four channels together and feeding the same analog inputs via an external fan–out.

2 INTRODUCTION

We designed and built a VME slave module which fulfills several experimental requirements.

Electrical and Mechanical specifications	*Conform to VME CERN v430 standard*
Input Voltage Range	*2 Volt peak to peak*
Input Signal Shape	*Any Shape*
Rate of Input Signal Pulses	*20 kHz mean with peak rate at 100 – 200 kHz*
Resolution	*10 bit*
Sampling Frequency	*40 MHz*

Table 1: Requirements for the design of our board.

The low energy experiments can have mainly two kinds of approach for energy measurement: acquiring all energy pulse long with a waveform digitizer or acquiring one sample on the base line and one sample on the maximum of the energy pulse.
The experiments with cryogenic detectors [1], [2], [3], [4] choose generally the first kind of approach because they need a good energy resolution. By acquiring all energy pulse long and then storing whole samples on mass storage, it is possible an off line digital processing of the cryogenic detector signal to reduce white and microphonic noise [5], [6], [7] optimizing the signal to noise ratio.
The experiments with liquid scintillator based detector [8] prefer simply thus to acquire one sample on the base line of the energy pulse and one sample on the maximum of the energy pulse.

Our design sits in between these two scenarios: it records a small number of samples for every signal, only when it is non zero, permitting a good timing reconstruction of the energy distribution in the vicinity of the event.

The technical requirement coming from the experiments are summarised in Table 1.
The board needs an external discriminator stage and an external front – end stage.
Each channel has a ECL signal input coming from the external discriminator stage in time with the rising edge of the energy analog input. At the time the discriminator fires each channel stores a time tag which is used to associate the data with a possible external general trigger [9].
To have the maximum flexibility, we designed a programmable board with a Digital Signal Processor (DSP)[1] and with a program register writing by DSP at command of a master VME.
The DSP reads directly the data from the A/D channels and then writes them in a 32 bit dual port RAM.
The dual port RAM serves as memory buffer between the board and the VME master CPU.
The DSP controls also the main functions of the board and may use the non triggered data for statistical measurements and transfer them via dual port RAM to VME master.

[1] We used the TMS320C50 device by Texas Instruments

3 CIRCUIT DESCRIPTION OF THE BOARD

The board is composed of a mother board (dimensions 9U × 400 mm) and of 32 piggy – back cards, each one corresponding to an Analog to Digital (A/D) channel and connected to the mother board by means of multiple – contacts connectors. The actual dimensions for the channel piggy – back are 50 mm × 70 mm.
Figure 1 shows a picture of whole board taken during the early debugging period.
The analog input of the single channel piggy – back card arrives via coaxial cable from the module front panel to its input stage. In this way all possible effects due to cross – talk and induced noise are minimised.
The piggy – back solution has a little disadvantage in term of production costs, but several advantages: development and prototype testing, production test and spare parts maintenance are much easier.
The A/D channel is also interchangeable: if some application needs different characteristics, it is possible to set up a board with different channels, while keeping the same structure.
The board specifications are also available on a WEB page [12].

3.1 Circuit description of the mother board

The electrical and mechanical specifications of the board are conform to VME standard with power supply conform to CERN v430 standard, using Jaux connector for ECL power supply and geographical addressing.
Figure 2 shows the block diagram of the mother board.
The time tag for the data is given by a counter running at 20 MHz, which is unique for whole thirty – two channels. It is free running and is latched after a possible external general trigger signal. It is also possible to write the time counter in particular for debugging purposes.
On the mother board the channels are grouped by four, buffering several inputs and output data buses.
The DSP runs at the same frequency (40 MHz) of the channels and it is synchronous with them in order to reduce digital noise on the board.
A flash EPROM is foreseen to bootstrap the DSP. It is possible to implement software routines for downloading of new software applications through VME bus via the dual port RAM.
The DSP is interfaced with the channels for readout data using programmable logic components and with several registers used to read the channels status (EMPTY and FULL), to set the working conditions (ENABLE channels, set how many clock cycle wait before write data and how many data has to be written), to read the running time tag counter.
Among several registers, the program register is particularly important. This register is accessible by DSP at the command of the VME master crate controller. In Table 2 is shown the bit map of the program register.

Bit map of program register	Corresponding board function
bit 0 ÷ bit 2	Number of wait cycles before write data samples
bit 3 ÷ bit 6	Number of data samples to write on channel FIFO
bit 7	Connected to the channels piggy back
bit 8	Mode of operation (0 = 32 channels@40MHz, 1 = 8 channels@160MHz)
bit 9 ÷ bit 11	Delay for read clock generation (3ns/step)
bit 12 ÷ bit 15	Unused

Table 2: Bit map of the program register accessible by DSP at the command of the VME master.

3.2 Circuit description of the A/D channel

The measurement logic is to sample N times the analog input signal at 40 MHz frequency, starting from the rising edge of the ECL signal discriminator. In this way it is possible not only to measure the peak value, but also to reconstruct the analog input signal shape and evaluate the possible pile – up introduced by neighbouring events or low frequency noise.
Figure 3 shows the block diagram of the A/D channel.
The Analog to Digital converter is always running and acquiring at 40 MHz clock rate; the control logic of the channel writes the data in the FIFO only in case of discriminator firing.
When the discriminator signal arrives, the control logic of the channel starts its job: waits for a programmable number of clock cycles (from two to eight) before activating the control signal for writing a programmable number of samples in the FIFO (from two to sixteen). The number of cycles to wait and the number of the acquired samples to write in the FIFO are defined by DSP in the program register (ref. Table 2).
The corresponding 16 bit time tag is stored in another FIFO in parallel with the first two write cycles of the acquired samples.

3.3 Description of the DSP program

The DSP must essentially set up the board working condition, do board diagnosis and execute the data read–out from the single channel to the dual port RAM. Besides, in the case of an experimental apparatus requiring particular calibrations, the DSP can do statistical measurement.
Again, the data can be pre–processed by the DSP before these are transferred in the dual port RAM.
The routines to set up the working conditions and to check the board functionalities are organised as interrupt routines for the DSP.
When the VME master executes a writing access to VME dedicated addresses, the VME logic interface on the board generates the DSP interrupt signals INT2 or INT3.
Receiving the interrupt signal the DSP reads the handshaking zone of the dual port RAM for understanding the request of the VME master.
In general the set up routines are activated at power up and in accordance with a particular sequence defined by the VME master.
After setting up and executing diagnosis, the DSP runs the main program, keeping the channels FIFO almost empty: the DSP reads all the enabled channels, checks for FIFO empty flags and if not empty reads both time tag and the programmed number of converted data.

In case of trigger the DSP transfers the converted data to the dual port RAM on event basis, so it is easy to build up the complete event. This operation is completely software controlled so it can be tailored for various requirements.

4 PERFORMANCES

The board prototype required minor modifications to have the circuit correctly working so we didn't need to build a second prototype to carry out measurement and performance characterisations.

The first measurement we carried out was to characterise the transfer function of the A/D channel and to extract its working parameters.
We measured the flat region of a low frequency square wave, modifing its level to span the input range of the A/D and then fit the data with a straigth line.
The result is graphically reported inד and can be shown that the linearity is very good on the whole input range.
Using these data we measured a differential non-linearity of about 1.56 % and a integral non-linearity of about 0.26 %. These numbers show that the ADC characteristics are maintained by the whole electronic circuit (we used an Analog Devices AD9050 device).

We also checked the behaviour of the board, used as 160 MHz digitizer.
The same input signal was fed into 4 neighbouring channels, activated by the same starting signal.
We used a step of 1.4 V with a rise time of 100 nsec, placing the first sample of the 4 channels before the leading edge, and acquiring some sample up to about 200 nsec.
We put together the 4 data sets off – line and then reconstructed the input signal shape. Each data set has a 6 nsec timing difference respect to the preceding and the following.
The raw data didn't fit very well on a straight line, because the system had to be calibrated.
After a calibration process the data fitted quite well the input signal shape.
In ה both raw data and then calibrated data are shown: dotted line represent raw data, filled line represent the calibrated data.

Then we measured "real world" signals coming from a photomultiplier (PMT).
A PMT was connected to a front end stage implementing a gateless charge integrator and the output signal was fed into an A/D channel to measure the single photoelectron response of our PMT.
The histogram with the measure of the single photoelectron peak is shown in ו together the fit function parameters.

The dead time on each channel is one clock cycle, after the job to write data into the FIFO is finished: running at 40 MHz the single channel is dead for 25 nsec.

The maximum rate of the input signals is determined by the speed of the DSP program used to

keep the channel FIFO almost empty and by the programmed working conditions. We can say that with the actual implementation the mean rate is 20 KHz with peak of 100 – 200 KHz handled by the channel FIFO.
The trigger rate supported can be in the order of 5 KHz.

5 CONCLUSIONS

The design of a multichannel multisampling ADC board was presented.
The prototype is now working in our lab performing very well, as expected.
A possible real world utilisation can be the energy measurement for the muon veto detector in the Borexino experiment, but other low energy experiments can be set using this circuit, for example cryogenics low noise, high resolution apparatus.
Because the generality of the A/D conversion technique used here and the flexibility of the implementation (thanks to the DSP), many groups from high energy physics community are evaluating the use of our module for reading out multi anode photomultipliers.

6 ACKNOWLEDGEMENTS

We would like to mention here some of the various people that encouraged and helped us in the development of this design.
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Thanks also to doct. Oleg Smirnov, that worked with us in the measurements with the photomultiplier.
Fabio Siccardi and Adriano Bevilacqua, did the hard job of designing the printed circuit cards and assembling the prototypes.

7 FIGURES

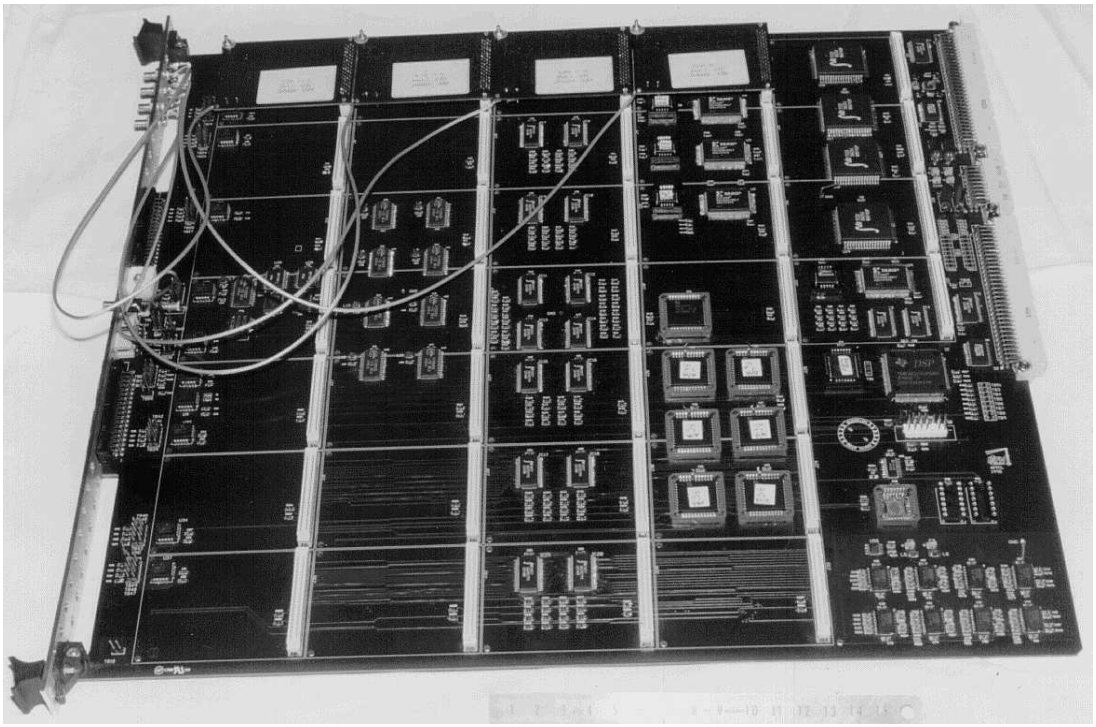

Figure 1 A picture of the multichannel multisampling analog to digital converter board.

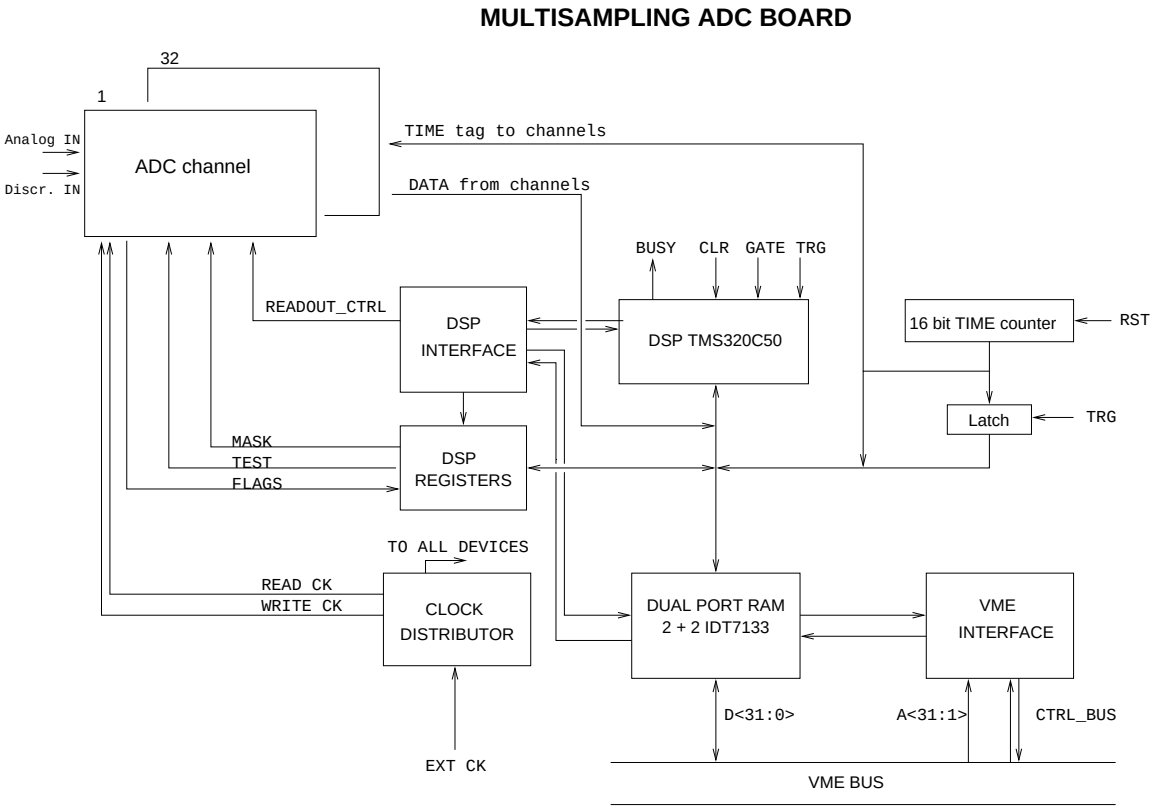

Figure 2 Block diagram of the mother board.

MULTISAMPLING ADC CHANNEL

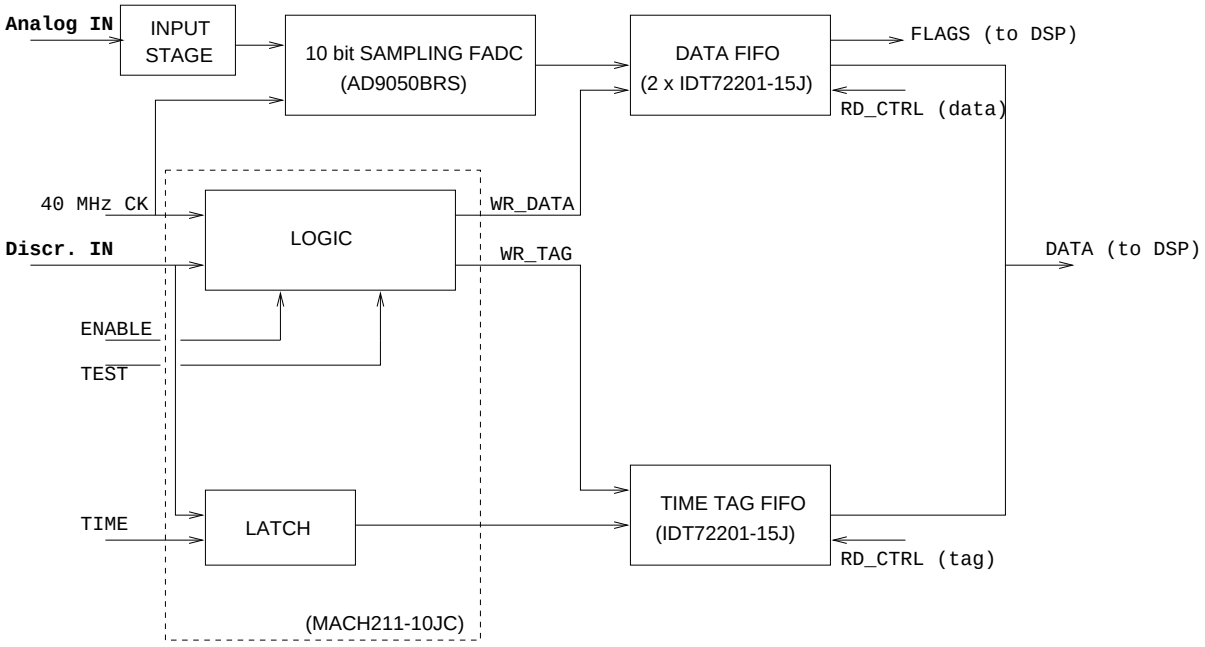

Figure 3 Block diagram of the channel circuit.

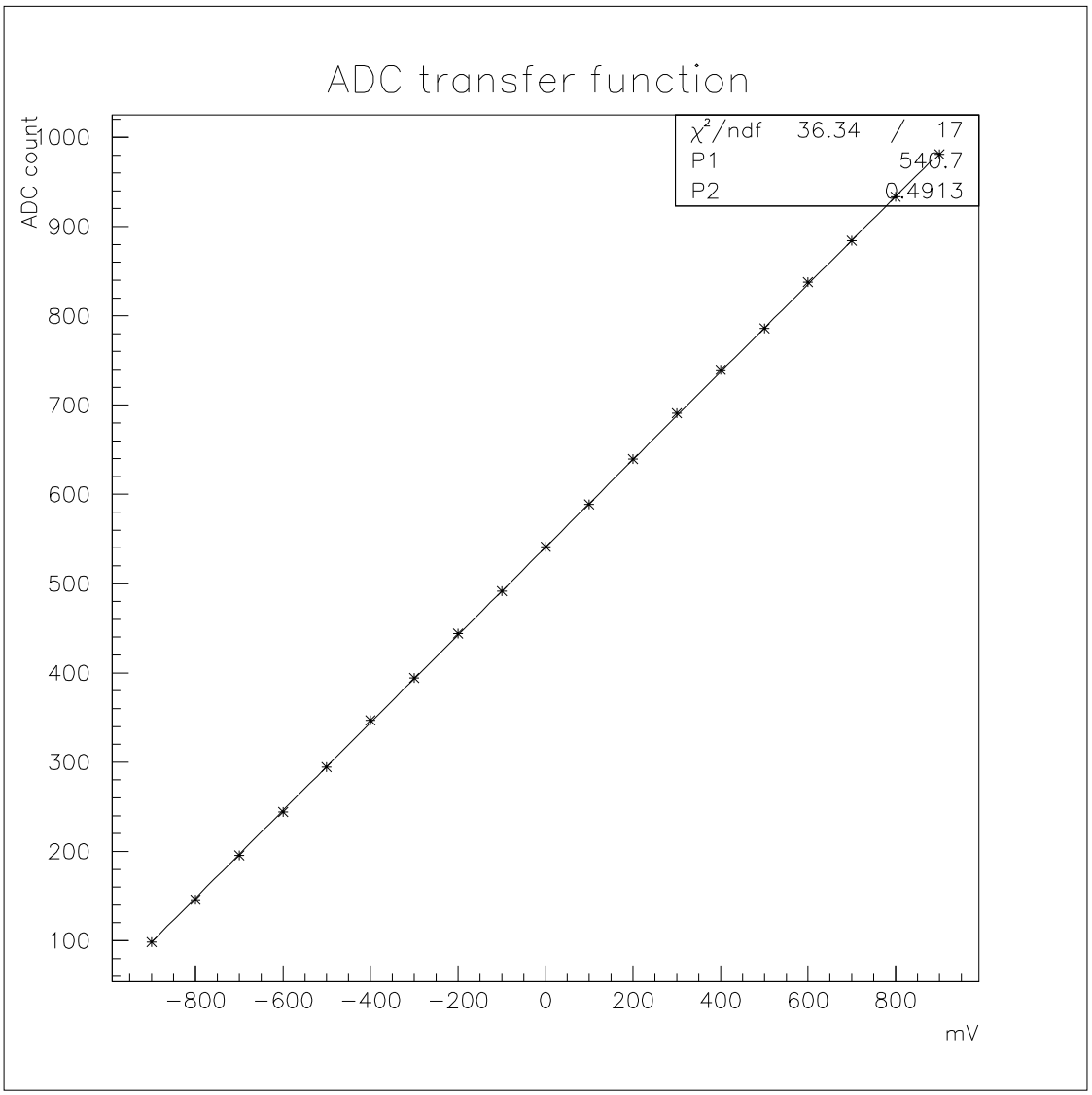

Figure 4 Transfer function of the A/D channel. The * are measured data, that fit very well the straight line.

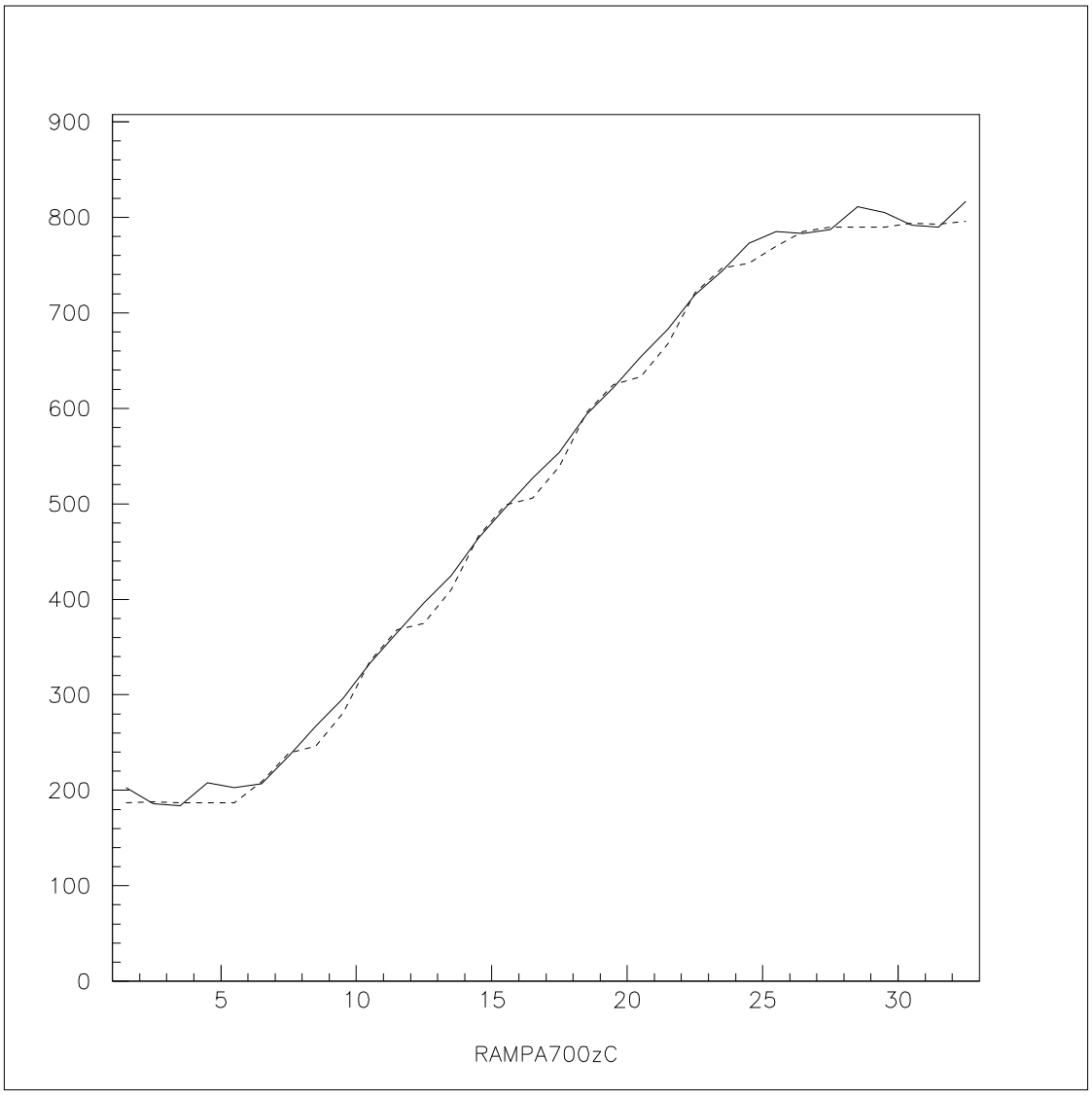

Figure 5 Reconstructed signal coming from 4 A/D channels. Raw data are dotted, elaborated data are continue.

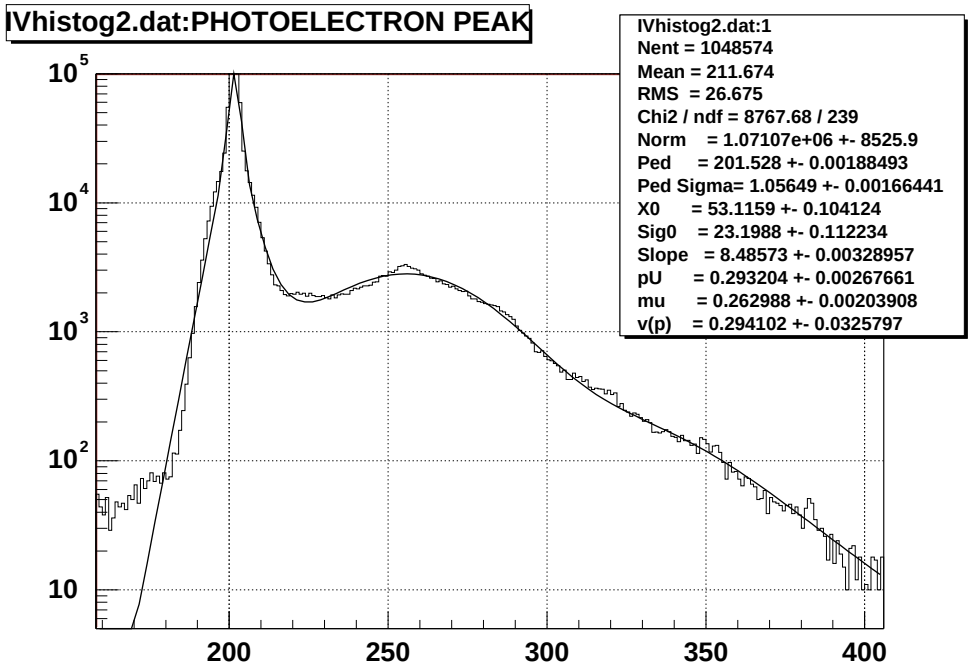

Figure 6 The single photoelectron response of an EMI photomultiplier. The fit function parameters are shown in the box.

8 REFERENCES

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