DAQ ELECTRONICS FOR BOREXINO EXPERIMENT

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Abstract

In this document we present the design and the implementation of an 8 channels VME board with the following functionalities (for each channel):

- Dual threshold discriminator
- Time to Digital Converter with resolution better than 500 psec
- Dual sampling 8 bit Analog to Digital Converter

The unit is controlled by a Digital Signal Processor. The DSP is used to collect data in order to have maximum flexibility and efficiency.

There is also the first stage of the trigger logic: the board outputs the number of photomultiplier fired in a time window of 50 nsec.

Another level of trigger logic is implemented at crate level on a dedicated unit which gives the number of PMT fired on a crate basis.

1 Introduction

The BOREXINO experiment main detector is composed by about 2000 8–inches photomultiplier tubes (PMTs). The PMT will work mainly in single photo electron mode (for neutrino events), but can also give very large signals due to cosmic rays.

Each PMT pulse carry two informations: the time of the event and the energy of the event (the charge collected on the photo cathod). We can define an "event" as the complete set of informations coming from all PMTs.

Each event will have an absolute time reference: the timing information coming from each PMT is needed to reconstruct the position of the event. The energy signal is used to compute the total energy of each event and also used to better estimate the event origin.

The requirement of the electronic system and a complete description of the detector can be found in [1].

A "trigger" must occour to start the data readout process. The BOREXINO trigger alghorithm is to count the PMTs fired in a 50 nsec time window and start the data acquisition if this number is greater than a given threshold. The data acquisition will read data in a time range from 1 μsec before the trigger to 4 – 5 μsec after the trigger.

In this document we describe the electronic system used to collect data coming from the PMTs after an analog processing (not described here) and the lowest levels of the trigger system.

A complete preliminary description for the trigger system can be found in [2].

A description of the front end analog section for the PMT can be found in [3].

In the following sections we will give an overview of the DAQ card and then we'll descrive with more details each building block.

We will give also a description of the trigger and synchronization card, used to implement the first level of the trigger logic and to distribute all needed control signals to the 20 DAQ boards housed in the crate. It is located in the back side of the crate, in horizontal position below the J2/P2 connectors, and it is used to implement the first level of the trigger alghorithm and to distribute clocks and all other control signals needed for the correct work of the DAQ system.

2 The DAQ board

A DAQ board block diagram is presented in figure 1.

The DAQ board is a VME slave unit in the format 6U $\times$ 280 mm.

It houses 8 independent channels and put the data in a VME accessible memory. The main control logic is implemented using a DSP [1] which gives a complete flexibility of operations and guarantees also future modifications and enhancements of the system.

[1] We use a Texas Instruments TMS320C50 device.

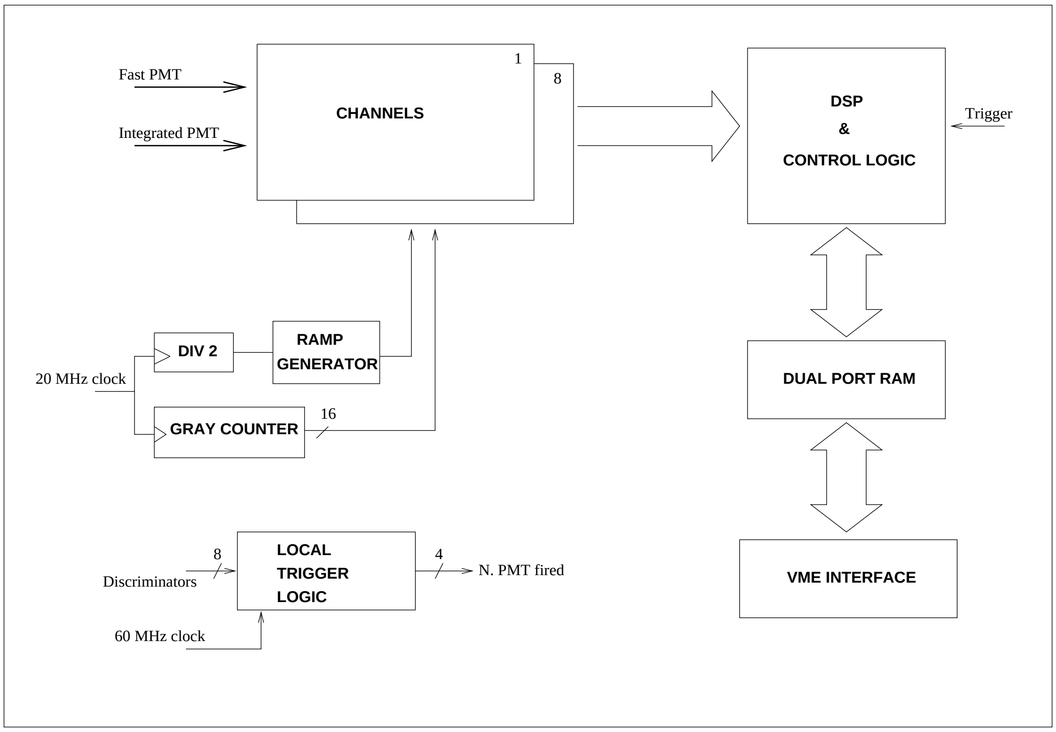

Fig. 1. The DAQ board block diagram.

The design was developed in collaboration with LABEN S.p.A. [2] which also developed several prototypes and now is in charge for the production of the complete system (about 250 cards housed in 13 crates).

In the VME crate are located 20 DAQ cards and a CPU controller. Each crate will handle $20 \times 8 = 160$ channels.

The DAQ system will read data form these cards through the CPU controller and send them to a main controller workstation on a local area network. A description of the DAQ system can be found in [4] and in [5].

3 The single acquisition channel

The acquisition channel block diagram is presented in figure 2.

Each channel has two inputs coming from the front–end stage:

– the fast PMT signal which is an inverted and amplificated copy of the PMT signal, used to fire the discriminator and to give the timing information

[2] LABEN S.p.A. Strada Padana Superiore, 290 - 20090 - VIMODRONE (Mi) - Italy

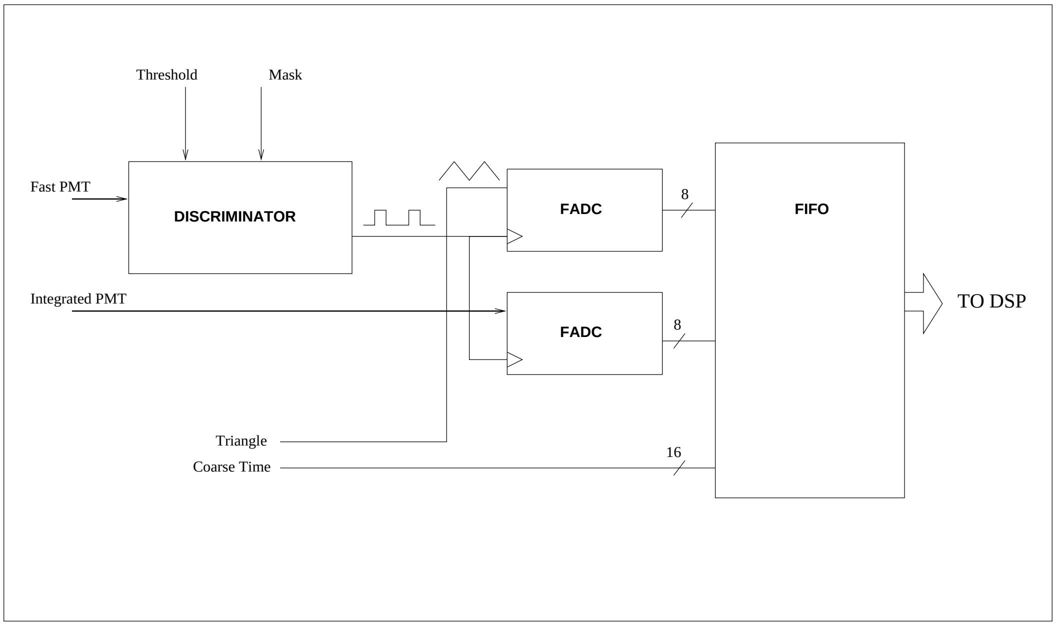

Fig. 2. The channel block diagram.

– the integrated PMT signal which gives the energy information

The functionalities of a single acquisition channel are the followings:

– Dual threshold discriminator, maskable and programmable. The output signal is a double pulse with 30 nsec width and 80 nsec delay between the two pulses.
– Time to Digital Converter (TDC) with resolution better than 500 psec.
– Dual sampling 8–bit ADC which samples the energy signal just before its rising edge and 80 nsec later, using the discriminator output signal. The difference between these two values is proportional to the charge collected on the photo cathod.
– Local FIFO buffer, 24 bit wide, 256 word deep, used to temporarily store the data while the system is waiting for a possible trigger. The maximum trigger latency possible is 6.4 μsec.

The TDC is the most complicated circuit and hence we'll describe it in more detail.

3.1 The TDC

The TDC is mainly composed by two sections:

(i) The coarse timing is given by a 16 bit synchronous Gray coded counter clocked with 20 MHz clock, which give a resolution of 50 nsec.

(ii) The fine timing is given sampling twice a 10 MHz triangular signal, synchronous with the counter clock, with the dual pulse signal coming from the discriminator.

For the coarse time information we used a Gray coded counter because the input signal is asynchronous and there is the possibility to sample the counter output while it is not stable.

The double sampling technique is used to have the correct timing also if a sample occours in a discontinuity of the triangular wave: it is assured that at least one sample is in the linear region of the signal.

The triangular wave generator and the Gray counter are common to the card and their output signals are distributed to all channels on the board.

The Gray code is then converted into binary before read out, in order to have the correct number without needing to convert it by software.

4 The main control and the VME buffer

The main control logic is implemented, as already mentioned, using a DSP.

The main program flow of the DSP code is to control the channel FIFO status and wait for triggers. While the DSP checks the FIFO it can read untriggered data to build up histograms. Energy histograms can be used for on–line analisys and control of the PMTs working point [3].

The trigger signal, coming from the trigger logic, interrupts the DSP and cause the readout of the data from the channels, reformat and store them in the memory bank.

The memory bank is organized on event basis: for each event there are all data coming from the channels, together additional informations such as absolute time, trigger identifier, module identifier and so on.

If a card contains no data for a particular event, an empty record is generated, to keep the system aligned.

The memory bank is a dual port memory (2048 word deep, 32 bit wide), accessible both from the VME bus and from the DSP. It is organized in three separate banks: some locations are reserved for exchanging configuration and

[3] The regulation of the PMT gain will be carried out controlling the supply voltage on the power supply system.

programming data, the main part is reserved for event data records and the remaining part is dedicated to store histograms.

5 The local trigger logic

On the board there is the very first stage of the trigger generation logic.

Each discriminator output feeds a one–shot circuit which generates a 50 nsec pulse and then the 8 signals are summed together using a logic network. The output of this logic is then sampled with a 60 MHz clock. So we have the number of the PMTs fired on the card in the 50 nsec time window available every 16.6 nsec.

The width of the one–shot and the sampling frequency are controlled independently using two separate clocks coming from the backside trigger card.

6 The trigger card

A dedicated unit is used to collect trigger data from all 20 cards in a crate and calculate the number of PMT fired on a crate basis. This number is then sent to the successive level of the trigger system.

This card is located in the back side of the crate, in horizontal position below the J2/P2 VME connectors.

This card is also used to distribute clocks and synchronization signals needed by the DAQ cards through the J2/P2 connectors.

It also receive the trigger number from ther main trigger logic, store it in a VME accessible register and distribute it to all DAQ cards using dedicated pins of the J2/P2 connectors.

References

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