DESIGN AND PERFORMANCE OF A MULTICHANNEL MULTISAMPLING ANALOG TO DIGITAL CONVERTER BOARD FOR ENERGY MEASUREMENT

P. Musico, A. Nostro
INFN – Sezione di Genova, via Dodecaneso 33 – 16146 Genova (Italy)

1 ABSTRACT

This paper describes a VME multichannel multisampling analog to digital converter board for the events energy measurement in low energy experiments. To guarantee the maximum experimental flexibility the module is completely programmable through a Digital Signal Processor and a program register accessible via VME bus. With the frequency 40 MHz the single channel can acquire a variable number of samples of the analog input. Besides, it is possible use the board as a 160 MHz waveform digitizer grouping four channels together feeding the same analog inputs via an external fan out.

2 INTRODUCTION

The low energy experiments of our institute needed a VME board for energy measurement. So we designed and built a VME slave module having skill to be suitable for the several experimental requirements.

Electrical and Mechanical specifications	*Conform to VME CERN v430 standard*
Input Voltage Range	*2 Volt peak to peak*
Input Signal Shape	*Any Shape*
Rate of Input Signal Pulses	*20 kHz mean with peak rate at 100 – 200 kHz*
Resolution	*10 bit*
Sampling Frequency	*40 MHz*

Table 1 Requirements for the design of our board.

The low energy experiments can have mainly two kinds of approach for energy measurement: acquiring all energy pulse long or acquiring one sample on the base line of the energy pulse and one sample on the maximum of the energy pulse.
The experiments with cryogenic detectors [1], [2], [3], [4] choose generally the first kind of approach because they need a large energy resolution. In fact, acquiring all energy pulse long and then storing whole samples on mass storage, it is possible an off line digital processing of the cryogenic detector signal to reduce white and microphonic noise [5], [6], [7] improving so the energy resolution.
The experiments with liquid scintillator based detector [8] prefer simply acquiring one sample on the base line of the energy pulse and one sample on the maximum of the energy pulse.
The technical requirement coming from the experiments are resumed in Table 1.
The board needs an external discriminator stage and an external front – end stage.
Each channel has a ECL signal input coming from the external discriminator stage in time with the rising edge of the energy analog input. At the same time of the discriminator firing each channel stores also a time tag used to associate the data with a possible external general trigger [9].
To have the maximum versatility we thought a programmable board with a Digital Signal Processor (DSP)[1] and with a program register writing by DSP at command of a master VME.
The DSP reads directly the data from the A/D channels writing successively them in a 32 bit dual port RAM.
The dual port RAM serves as memory buffer between the board and the VME master CPU working as crate controller.
The DSP controls also the main functions of the board and could use the non triggered data for statistical measurements and transfer them via dual port RAM to VME master for the slow control of the detector used in the experiment.
The VME master crate controller has substantially two main functions: communicating with the DSP through a flag handshaking zone of the dual port RAM and transferring the data from dual port RAM via bus VME to a workstation via Ethernet/fast – Ethernet link [9], [10].

The board was designed and built for allowing remote control of the experimental apparatus. For this reason we foresaw a flag handshaking zone of the dual port RAM so that a person can execute from his workstation some operation on the board via Ethernet (Remote Procedure Call)

[1] We used the TMS320C50 device by Texas Instruments

through the VME controller crate, as for example opening and closing the single acquisition channel, asking a energy histogram of a particular channel, resetting the DSP and so on.

3 CIRCUIT DESCRIPTION OF THE BOARD

The board is composed of a mother board having dimensions 9U × 400mm and of 32 piggy-back cards, everyone corresponding to one Analog to Digital (A/D) channel and connected to the mother board using multiple-contacts connectors. The actual dimensions for the channel piggy-back are 50mm × 70mm.
Figure 1 shows a picture of whole board during the debugging stage.
The analog input of the single channel piggy-back card arrives via coaxial cable from the module front panel to its input stage. In this way it is possible to minimise all possible effects due to cross-talk and induced noise.
The piggy back solution has a little disadvantage in term of production costs, but several advantages: development and prototype testing simpler, production test simpler, spare parts maintenance simpler.
The A/D channel is also interchangeable: if some application needs different characteristics, it is possible to set up a board with different channels, but keeping the same structure.
The board specifications are available on a web page [12].

3.1 Circuit description of the mother board

The electrical and mechanical specifications of the board are conform to VME standard with power supply conform to CERN v430 standard, using Jaux connector for ECL power supply and geographical addressing.
Figure 2 shows the block diagram of the mother board.
The time tag of the data is given by a counter running at 20 MHz which is unique for whole thirty-two channels. It is free running and is latched after a possible external general trigger signal. It is also possible writing the time counter in particular for debugging purposes.
On the mother board the channels are grouped by four, buffering several inputs and output data buses.
The DSP runs at the same frequency (40 MHz) of the channels synchronous with them so we can minimize digital noise on the board.
A flash EPROM is foreseen to bootstrap the DSP. It is possible to implement software routines for downloading of new software applications through VME bus via dual port RAM.
The DSP is interfaced with the channels for readout data using programmable logic components, and with several registers used to read the channels status (EMPTY and FULL), to set the working conditions (ENABLE channels, set how many clock cycle wait before write data and how many data has to be written), to read the running time tag counter.
Between the several registers there is the program register in particular. This register is accessible by DSP at the command of the VME master crate controller. In Table 2 is shown the bit map of the program register.

Bit map of program register	Corresponding board function
bit 0 ÷ bit 2	Number of wait cycles before write data samples
bit 3 ÷ bit 6	Number of data samples to write on channel FIFO
bit 7	Connected to the channels piggy back
bit 8	Mode of operation (0 = 32 channels@40MHz, 1 = 8 channels@160MHz)
bit 9 ÷ bit 11	Delay for read clock generation (3ns/step)
bit 12 ÷ bit 15	Unused

Table 2 Bit map of the program register accessible by DSP at the command of the VME master.

3.2 Circuit description of the A/D channel

The measurement logic is to sample N times the analog input signal at 40 MHz frequency, starting from the rising edge of the ECL signal discriminator. In this way it is possible not only to measure the peak value, but also to reconstruct the analog input signal shape and evaluate the possible pile – up introduced by neighbouring events or low frequency noise.
Figure 3 shows the diagram block of the channel circuit.
The Analog to Digital converter is always running and acquiring at 40 MHz clock rate; the control logic of the channel only allows the data writing on the FIFO in case of discriminator firing.
When the discriminator signal arrives, the control logic of the channel starts and waits for a programmable number (from two to eight) before activating the control signal for writing a programmable of samples on the FIFO (from two to sixteen). The number of cycles to wait and the number of the acquired samples to write on the FIFO are defined by DSP in the program register (ref. Table 2).
The corresponding 16 bit time tag is stored in another FIFO in parallel with the first two writing of the acquired samples.

3.3 Description of the DSP program

The DSP must essentially set up the board working condition, do board diagnosis and execute the data read-out from the single channel to the dual port RAM. Besides, in the case of an experimental apparatus requiring particular calibrating, the DSP can do the statistical measurement.
The routines for setting up the working condition and for doing the diagnosis of the board were organised as interrupt routines for DSP.
When the VME master executes a writing access to VME dedicated addresses, the VME logic interface on the board generates the DSP interrupt signals INT2 or INT3.
Receiving the interrupt signal the DSP reads the handshaking zone of the dual port RAM for understanding the request of the VME master.
In general the routine for setting up the board working conditions and executing the board diagnosis are activated at power up and in accordance with a particular sequence defined by the VME master.
After setting up and executing diagnosis the DSP runs the main program flow keeping the channels FIFO almost empty: the DSP reads all the enabled channels, checks for FIFO empty

flags and if not empty reads both time tag and the programmed number of converted data.
In case of trigger the DSP transfers the converted data to the dual port RAM on event basis, so it is easy to build up the complete event. This operation is completely software controlled so it can be tailored for various requirements.

4 PERFORMANCES

The board prototype required minor modifications to have the circuit correctly working so we didn't need to build a second prototype to carry out measurement and performance characterizations.

The first measure we carried out was to characterise the transfer function of the A/D channel and to extract its working parameters.
We measured the flat region of a low frequency square wave, modifing its level to span the input range of the A/D and then fit the data with a straigth line.
The result is graphically reported in
Figure 4 and can be shown that the linearity is very good on the whole input range.
Using these data we measured a differential non-linearity of about 1.56 % and a integral non-linearity of about 0.26 %.

We also checked the behaviour of the board, used as 160 MHz digitizer.
The same input signal was fed into 4 neighbouring channels, activated by the same starting signal.
We used a step of 1.4 V with a rise time of 100 nsec, placing the first sample of the 4 channels before the leading edge, and acquiring some sample up to about 200 nsec.
We put together the 4 data sets off-line and reconstructed the input signal shape. Each data set has a 6 nsec timing difference respect to the preceding and the following.
The raw data didn't fit very well on a straight line, because the system had to be calibrated.
After a calibration process the data fitted quite well the input signal shape.
In
Figure 5 both raw data and then elaborated data are shown: raw data on dotted line and elaborated data on continue line.

Then we measured real world signals coming from a photomultiplier (PMT).
A PMT was connected to a front end stage implementing a gateless charge integrator and the output signal was fed into an A/D channel to measure the single photoelectron response of our PMT.
The histogram with the measure of the single photoelectron peak is shown in
Figure 6 together the fit function parameters.

5 CONCLUSIONS

The design of a multichannel multisampling ADC board was presented.
The prototype is now working in our lab performing very well, as expected.
A possible real world utilisation can be the energy measurement for the muon veto detector in the Borexino experiment, but other low energy experiments can be set using this circuit, for example cryogenics low noise, high resolution apparatus.
Cause the generality of the A/D conversion technique used here and the flexibility of the implementation thanks to the DSP, groups from high energy physics are evaluating the use of our module for reading out multi anode photomultipliers.

6 FIGURES

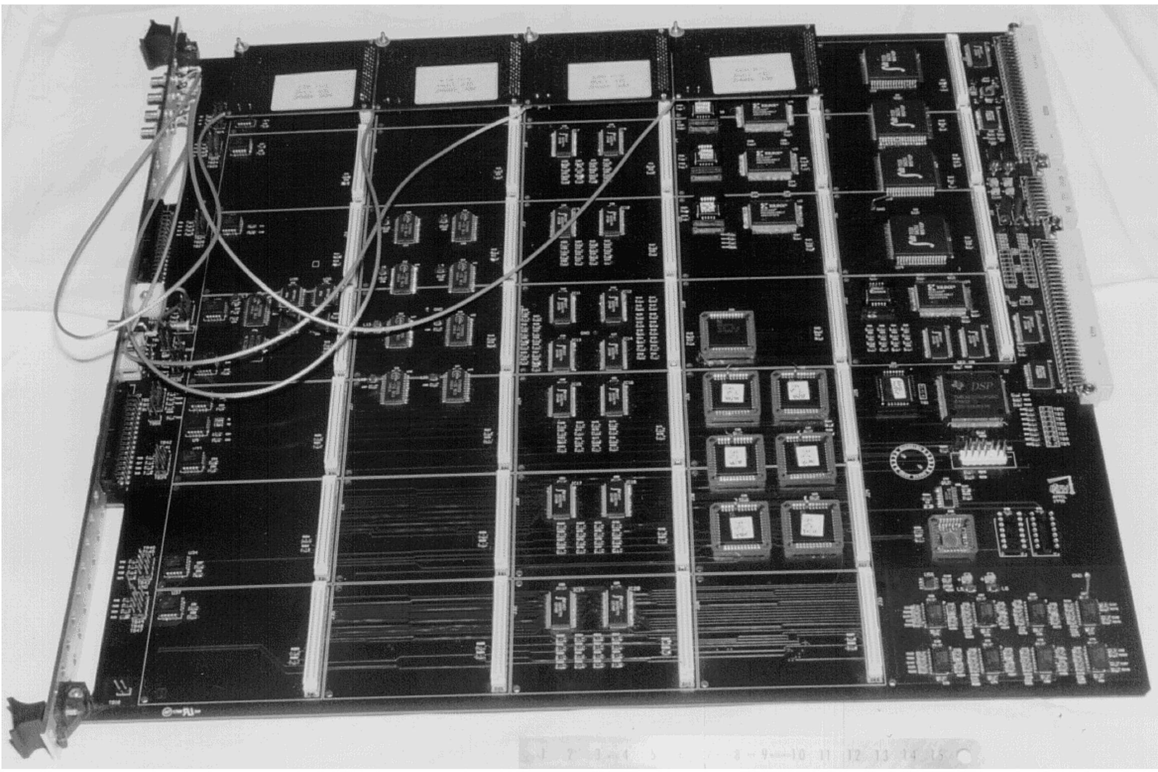

Figure 1 A picture of the multichannel multisampling analog to digital converter board.

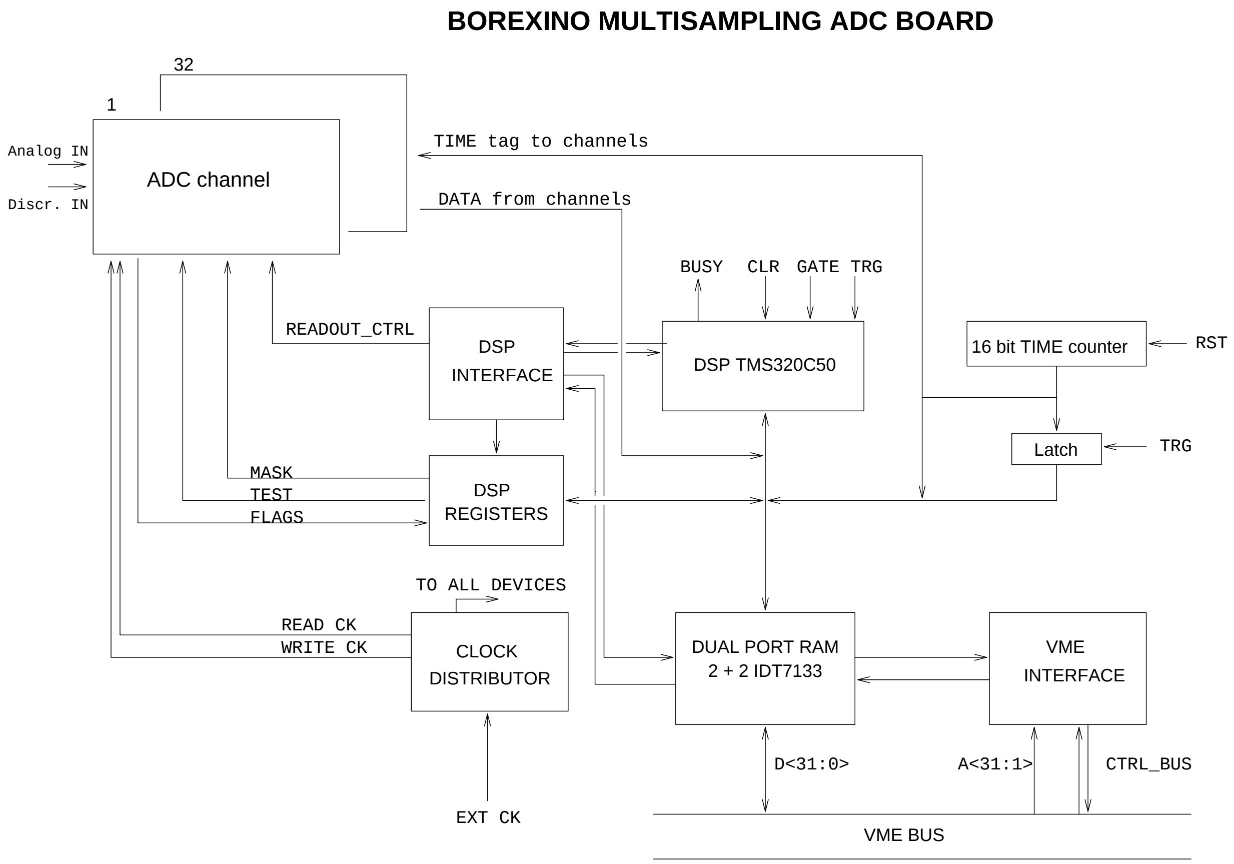

Figure 2 Block diagram of the mother board.

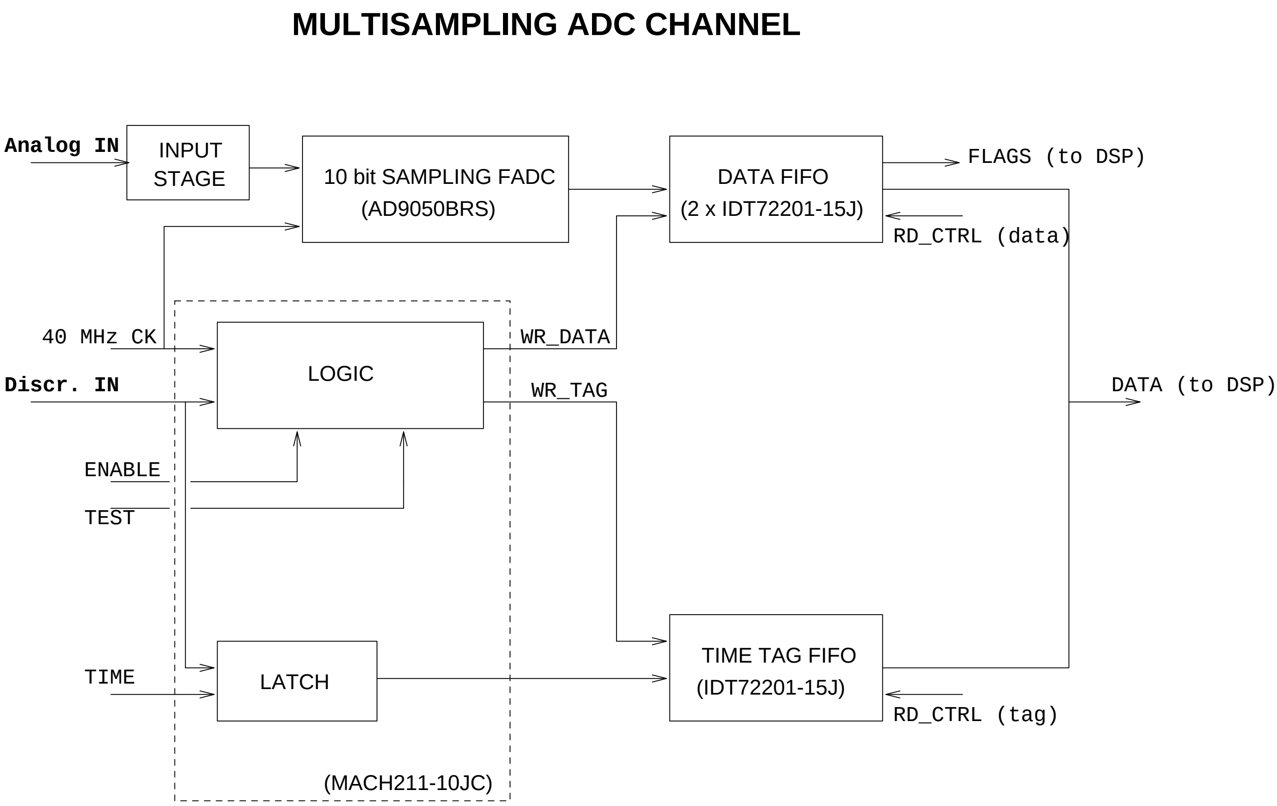

Figure 3 Block diagram of the channel circuit.

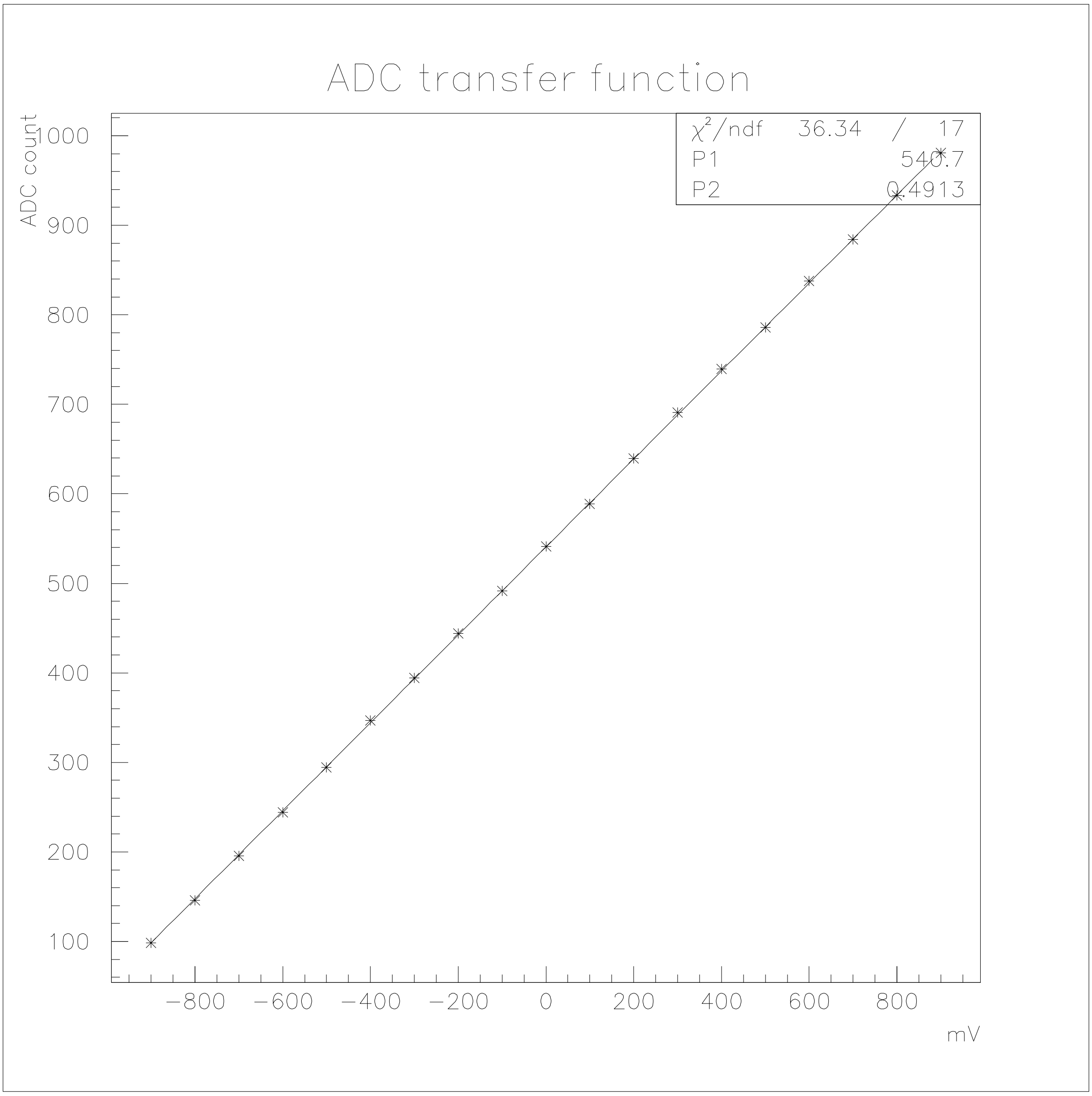

Figure 4 Transfer function of the A/D channel. The * are measured data, that fit very well the straight line.

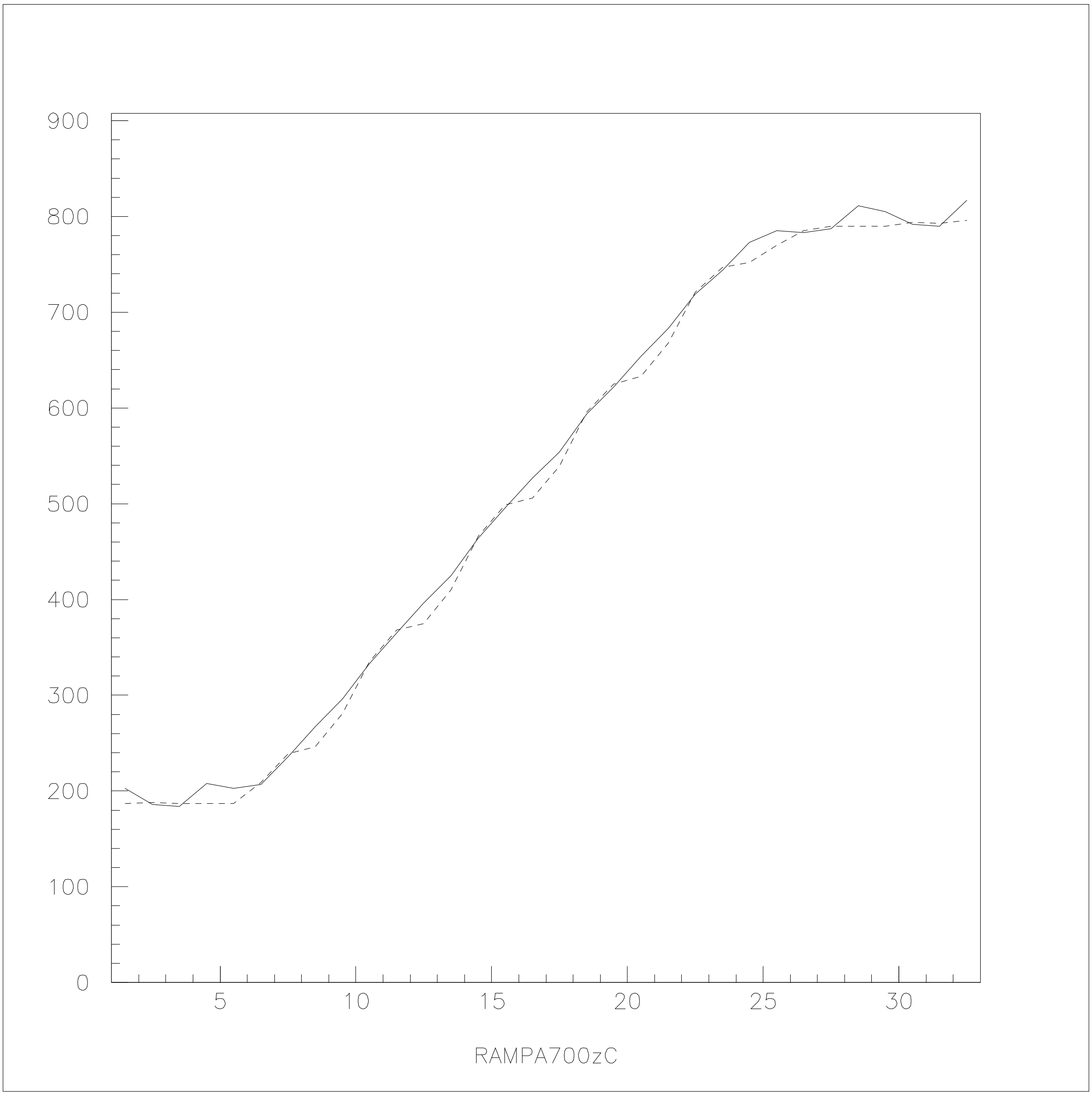

Figure 5 Reconstructed signal coming from 4 A/D channels. Raw data are dotted, elaborated data are continue.

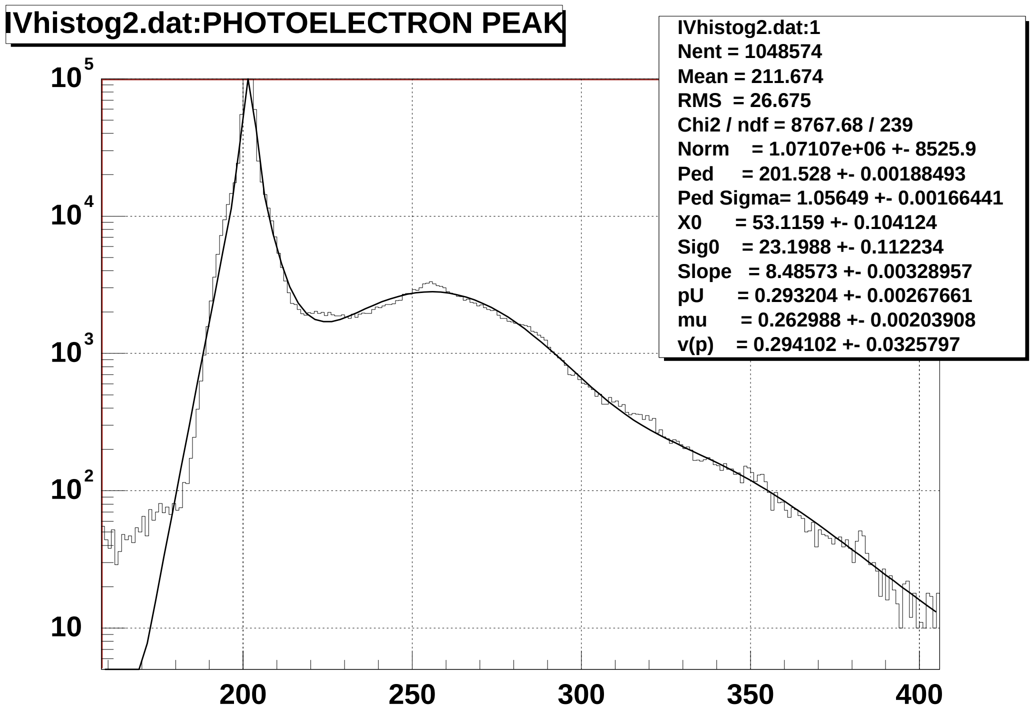

Figure 6 The single photoelectron response of an EMI photomultiplier. The fit function parameters are shown in the box.

7 REFERENCES

[1] E. Cosulich, G. Gallinaro, F. Gatti and S. Vitale, Phys. Lett. B 295 (1992) 143.
[2] A. M. Swift, Nuclear Physics (Proc. Supp.) 61B (1998).
[3] P. Meunier et al., Physics Letters B 398 (1997) 415-419.
[4] P. Meunier et al., Physics Letters B 398 (1997) 187-193.
[5] E. Cosulich and F. Gatti, Nucl. Instr. And Meth. A 321 (1992).
[6] F. Gatti and A. Nostro, Nucl. Instr. And Meth. A 368 (1996).
[7] F. Fontanelli, F. Gatti, A. Nostro, Nucl. Instr. And Meth. A 370 (1996).
[8] I.N.F.N., ed., Borexino at Gran Sasso, proposal for a real time detector for low energy solar neutrino (August 1991);
Princeton University, ed., a real time detector for low energy solar neutrinos (December 1992).
[9] P. Musico and A. Nostro, INFN/TC – 97/22 (4 Settembre 1997).
[10] P. Musico, M. Ruscitti, A. Nostro, INFN/TC – 97/23 (4 Settembre 1997).
[11] A. Nostro, Nucl. Instr. And Meth. A 409 (1998).
[12] ADC board for BOREXino experiment specifications, P. Musico and A. Nostro http://www.ge.infn.it/borexino/pub.html.