A POSSIBLE BOREXINO TRIGGER SYSTEM

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1. ABSTRACT

In this document a description of the BOREXINO experiment [1], [2], [3], [4], [5] trigger system is given.
First of all the main trigger alghoritm is explained and then a possible implementation is shown in detail.

2. THE ALGHORITM

The trigger must be generated when we have at least K Hits within a time ΔT=50 ns [6].
Due to the large number of channels a digital solution was preferred.
Speed and flexibility suggested a distributed structure.

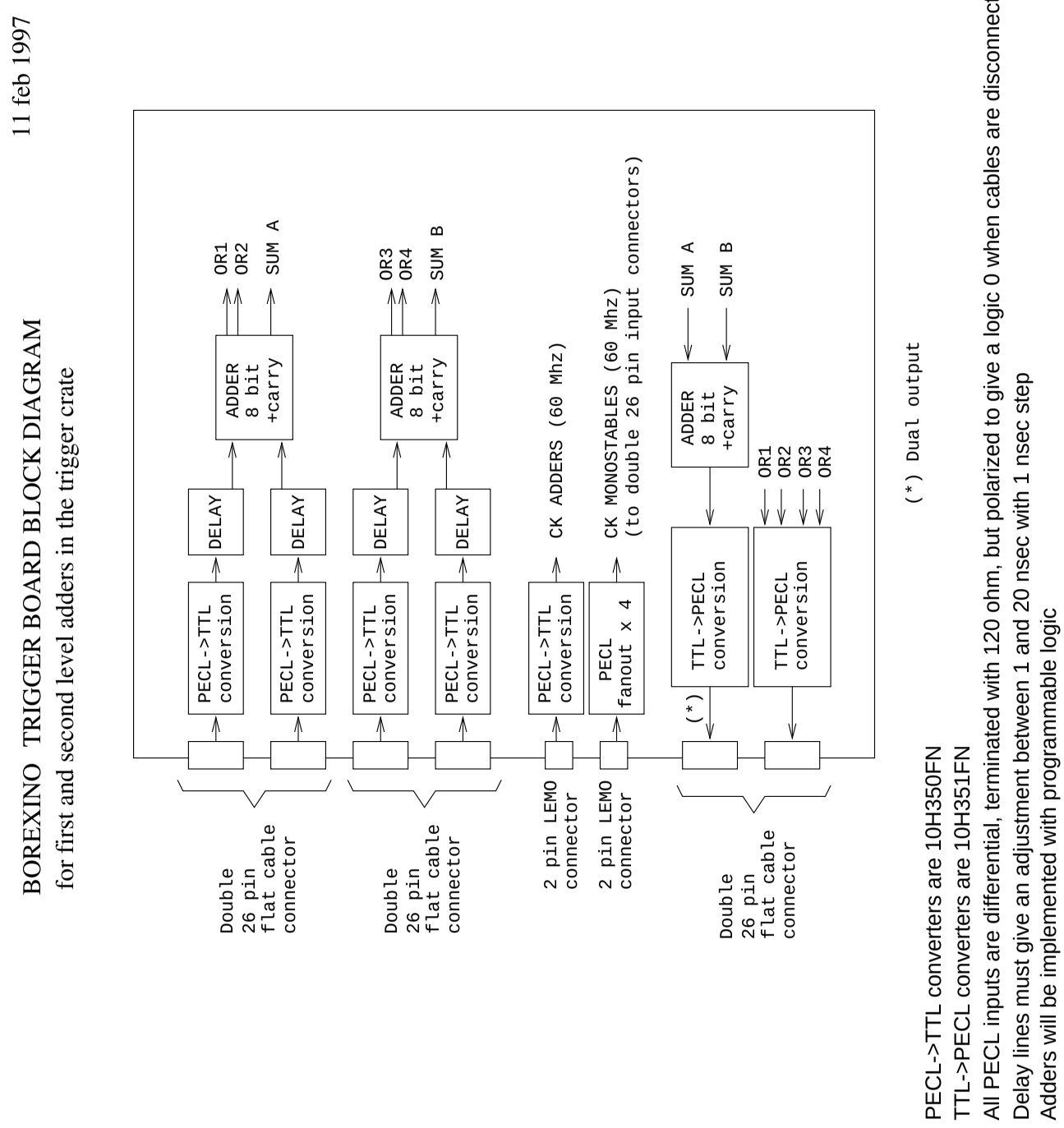

Figure 1 Block Diagram of the board used in the second and third levels.

BOREXINO MAIN TRIGGER BOARD BLOCK DIAGRAM

trgger generator and supervisor

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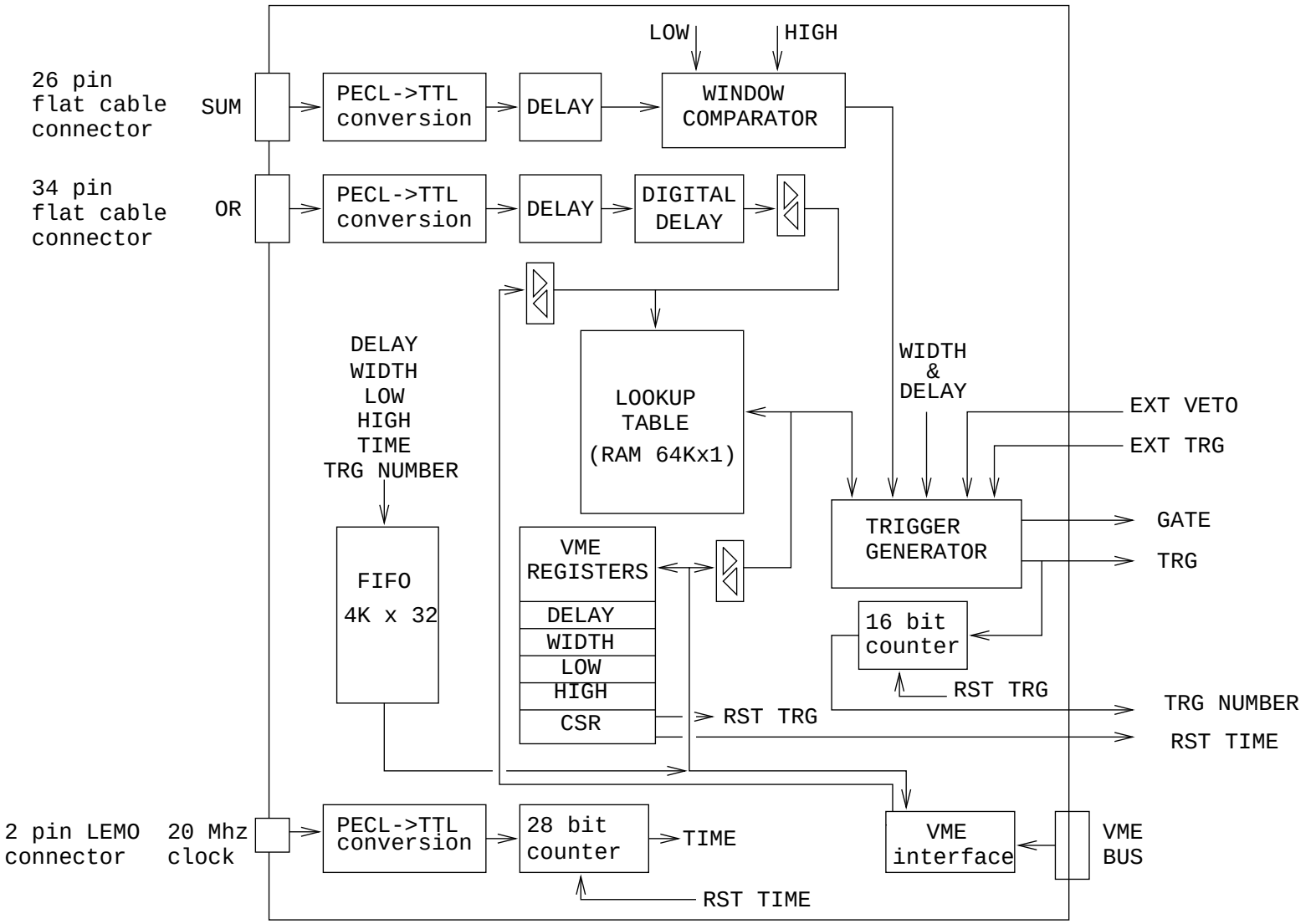

Figure 2 Block Diagram of the board used in the main level.

3. IMPLEMENTATION

3. 1. First level on Data Acquisition board

On the data acquisition board the output of the discriminators activate 8 corresponding monostables which generates a 50 ns (nominal width) pulse. The pulse width is multiple of period of a control clock signal (nominal frequency: 60 MHz). These signals feed a 4 bit adder which give the sum of PMT hit per board. The output of the adder is sampled at 60 MHz (nominal).

To have maximum flexibility 2 clock signal are provided: one to generate the pulse from monostables and the other to sample the adder output. Nominally they have the same frequency of 60 MHz. Modification on the frequency of the first clock signal corresponds in the variation of monostables pulse width.

In practical at the output of the data acquisition board we have the number of hit PMT every 16 ns (60 MHz).

3. 2. Second level in the local crate

This dedicated board is placed in the rear of the crate, below the power supply unit, near the J2/P2 backplane connectors, in orizontal position.

This unit collect trigger data from the 20 data acquisition boards and compute the sum of hit PMT per crate, building an 8 bit data bus which carry a number in the range 0 - 160 at 60 MHz frequency. The data bus must also contain an additional bit which is the carry-in signal for the next level: it must be set to 0 in order to insure the correct functionality of the system[1].

The other functions will be briefly described here.

In addition this unit distribute the 2 clock signal described above to the 20 data acquisition boards.

This board receives the TRIGGER and GATE signals and the TRG NUMBER 16 bit bus.

It distributes the above signals to the 20 data acquisition boards. In addition it has a VME accessible register to hold the 16 bit TRG NUMBER value and has the possibility to generate an interrupt to the master CPU when it receives a TRIGGER.

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[1] It could also left unconnected because the termination network on the successive level board will give a logic 0 with cable disconnected

The RESET TIME signal is also received and distributed to the 20 data acquisition cards. This is used to synchronise the entry data acquisition system, resetting the time counters.
Detailed description of this unit can be found elsewhere.

3. 3. Third level in the main crate

A specialised board will receive data from previous level, performs 2 addition steps and pass data to the next level. In addition a logical condition of one active channel at least is transmitted to the main level.
The board, shown in Figure 1, will receive data from 4 data acquisition crates at PECL levels.
For this level we need four boards ($160 \times 16 = 2560$ channels).
Each 8 bit data bus carrying the sum of PMT hit in the last 50 ns has an associated clock signal at nominal frequency of 60 MHz.
For each bus there is a level conversion section: this section contains also a termination network for each signal, designed to give a logic zero if the cable is disconnected.
This is very useful in the phase of building and debugging the complete system.
After the level conversion to TTL levels a de-skew section is necessary: all data are aligned with the master reference clock, synchronous with the incoming ones.
Two adders perform the computation of the sum of the hit PMT for each couple of crates.
The adder will have a carry input signal for each 8 bit data bus and a carry out bit to indicate an overflow.
The carry input signals will not be used in the third level trigger logic, because each bus can contain an 8 bit number between 0 and 160. The output of these adders is the sampled at the same frequency of the main clock (60 MHz).
The adder will have also 2 additional outputs (always sampled at 60 MHz) to indicate that there is at least one PMT hit in the input bus: this is a logical OR of the 8 input lines.
These OR signals are then converted to PECL levels and sent to the main trigger board via a 26 pins connector.
A successive adder, identical to the preceding, will perform an additional level of computation.
The output of this circuit is then converted to PECL levels and sent to the next level board via a 26 pins connector.
To have the maximum flexibility it is useful to foresee two identical outputs for the sum data bus: this could be useful for feeding two subsequent process in parallel.
All I/O signals are set on front panel connectors.

We will use double 26 pins connector to reduce space on the front panel[2].

PECL to TTL converters will be Motorola 10H350FN while TTL to PECL converter will be Motorola 10H351FN.

The three adders used are completely equivalent and will be implemented in programmable logic[3]

Delay lines will be silicon monholitic and must give an adjustment up to 20 ns in 1 ns.

Adjustment will be made via jumpers on PCB.

3. 4. Fourth level in the main crate

This level will be made with one board, identical to the previous level.

It will receive the four output bus from the previous level, performs two additional levels of computation and send the data to the main level board.

In this level the OR output will remain unconnected.

3. 5. Main level in the main crate

The main level trigger board block diagram is shown in Figure 2.

It will be a VME slave unit: the CPU can program the working conditions and read out data associated with the generation of control signals.

It will act as the supervisor of the entire data acquisition system.

This board will receive data from the preceding level and take the decision if and when generate the trigger signals. The conditions of generation of those signals are programmable writing an 8 bit register, giving a maximum time of 102.4 μs in step of 400 ns.

In addition to generate those control signals it will collect data on timing of the trigger events.

Via the VME bus we can set two thresholds (lower and upper) to programming the window of hit for which generate the trigger. If upper threshold is set to 0 it will be not used giving a single threshold behaviour. The duration of the data acquisition period is also programmable.

If a trigger condition occur when the system is already in data acquisition phase, no further trigger signal will be generated but the data acquisition period will be longer.

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[2] 3M P/N: 3429-D203 or 3429-L203.

[3] It is possible to use AMD MACH211.

31 28	27 24	23 16	15 8	7 0
0	TIME trg. n. 1			
0	TIME trg. n. 2			
0	.....			
0	TIME trg. n. N			
F	DELAY	WITH	HIGH	LOW
F	TRG TYPE	N trigger	TRG	COUNTER

Figure 3 The FIFO record format.

Practically it will be implemented loading a counter for each trigger condition, decrement it at 2.5 MHz[4] and close the GATE when it reaches 0. If GATE is already active its width will be incremented by the programmed duration.

This condition will be reported in a record for each generated trigger, which will be accessible on a VME memory.

To generate the trigger it is available a topological condition in addition to the thresholds: the OR signals coming from the third level will address a look-up table, implemented using a static RAM $64K \times 1$[5], the output of this table can enable or not the generation of control signals.

The OR signals must be delayed before addressing the look-up table to take into account the elapsed time to do 3 sum levels[6]: this will be done using a 3 bit shift register clocked at the same frequency of incoming signals. When no topological condition have to be satisfied we must load the look-up table with all ones: this will give always an OK for that condition.

An additional external signals of VETO is provided.

There is also the possibility to generate a trigger using an external signal: this is useful for testing and calibrations. For example with an external signal it is possible to generate the trigger and a synchronous laser light pulse.

In addition a trigger can be generated via software, writing an appropriate command in the CSR VME accessible register.

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[4] This will be obtained dividing by 8 the master 20 Mhz clock and gives a resolution of 400 nsec.

[5] Practically it will be implemented with a Cypress CY7C187 64K $\times$ 1component.

[6] One in the third level and two in the fourth level.

The TRIGGER and GATE signals will be generated with a programmable delay, set writing an appropriate VME register. The delay is programmable in the 0 -- 6 μs range in 400 ns step, using a 4 bit register. The delay is necessary to tune the acquisition time before the trigger: the data in the data acquisition board are delayed by 6.4 μs. Computing the trigger condition needs about 300 -- 400 ns.

The TRIGGER signal also increment the TRIGGER NUMBER 16 bit counter. The TRIGGER NUMBER is sent in parallel to all data acquistion crates: this number will be written in acquired data on data acquisition board for each event[7]. It will be possible to reset this counter writing an appropriate command in the CSR VME register.

The 20 MHz system clock[8] is received and increments a 28 bit counter[9]. This counter can be reset writing an appropriate command in the CSR VME register: the reset operation will act also on all counters in the data acquisition board, transmitting the RST TIME signal. The time information is used to tag each trigger condition: it will be written in a record for each event.

A 4K × 32 bit FIFO is provided. It will be used to store a record of information for each generated TRIGGER signal. The format of the record is shown in Figure 3.

The first N values are timing information related to each trigger condition that should generate the TRIGGER signal. The first condition generates the TRIGGER signal, while the others keep the GATE line active for an additional period with WIDTH duration.

The last two fields are used to reduce the possibility of confusion.

The word containing DELAY, WIDTH, HIGH, LOW is a copy of the condition used to generate the trigger. The last word containing TRG TYPE, N trigger, TRG COUNTER holds the number of preceding timing words and the trigger identification number: this is used in the event building phase to correlate acquisition data with trigger conditions. TRG TYPE field is used to identify the kind of trigger: normal, external, software.

The timing tag are recognised by the highest 4 bit set to 0, while the last two word have the highest 4 bit set to 1.

Flag to indicate FIFO conditions (empty, half, full) are accessible reading the CSR VME register.

This unit can also generate an interrupt to the CPU crate controller for every generated trigger: this can be enabled via the CSR VME register.

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[7] The transmission to the crates is made using 74FCT2541T octal line drivers.

[8] It must be distributed with high precision to all system components (13 crates for 2000 channels) via a low skew fanout.

[9] It must record time in range of seconds to garantee a good syncrhronization with absolute time.

A dead time between successive trigger is foreseen: it can be set up via jumpers and must be kept to the minimum possible value[10].

4. REFERENCE

[1] BOREXino Collaboration, "Proposal of BOREXino: A Real Time Detector for Low Energy Solar Neutrino", LNGS (1991).

[2] J.B. Benziger et al., "BOREXino: A Real Time Detector for Low Energy Solar Neutrino", Princeton (1992).

[3] BOREXino Collaboration, "BOREXino Project: The Counting Test Facility, Its Result and The BOREXino design", document of the BOREXino collaboration (1995).

[4] BOREXino Collaboration, "Addendum the BOREXino Proposal", document of BOREXino collaboration (1996).

[5] BOREXino Collaboration, "The High Sensicity Test of The BOREXino Experiment at LNGS", document of BOREXino collaboration (1996).

[6] F.Gatti, A.Nostro, G.Testera and S.Vitale, "Trigger Rate in BOREXino: Accidentals and Spurious Trigger", document of BOREXino collaboration (1995).

[10] A good dead time should be less than 1 μs.