Accelerating PWA Fits

Exploiting Current Trends in Computing Technology

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on leave of absence from
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Workshop on
New Partial-Wave Analysis Tools
for Next-Generation Hadron-Spectroscopy Experiments

Camogli, June 21st, 2012

Outline

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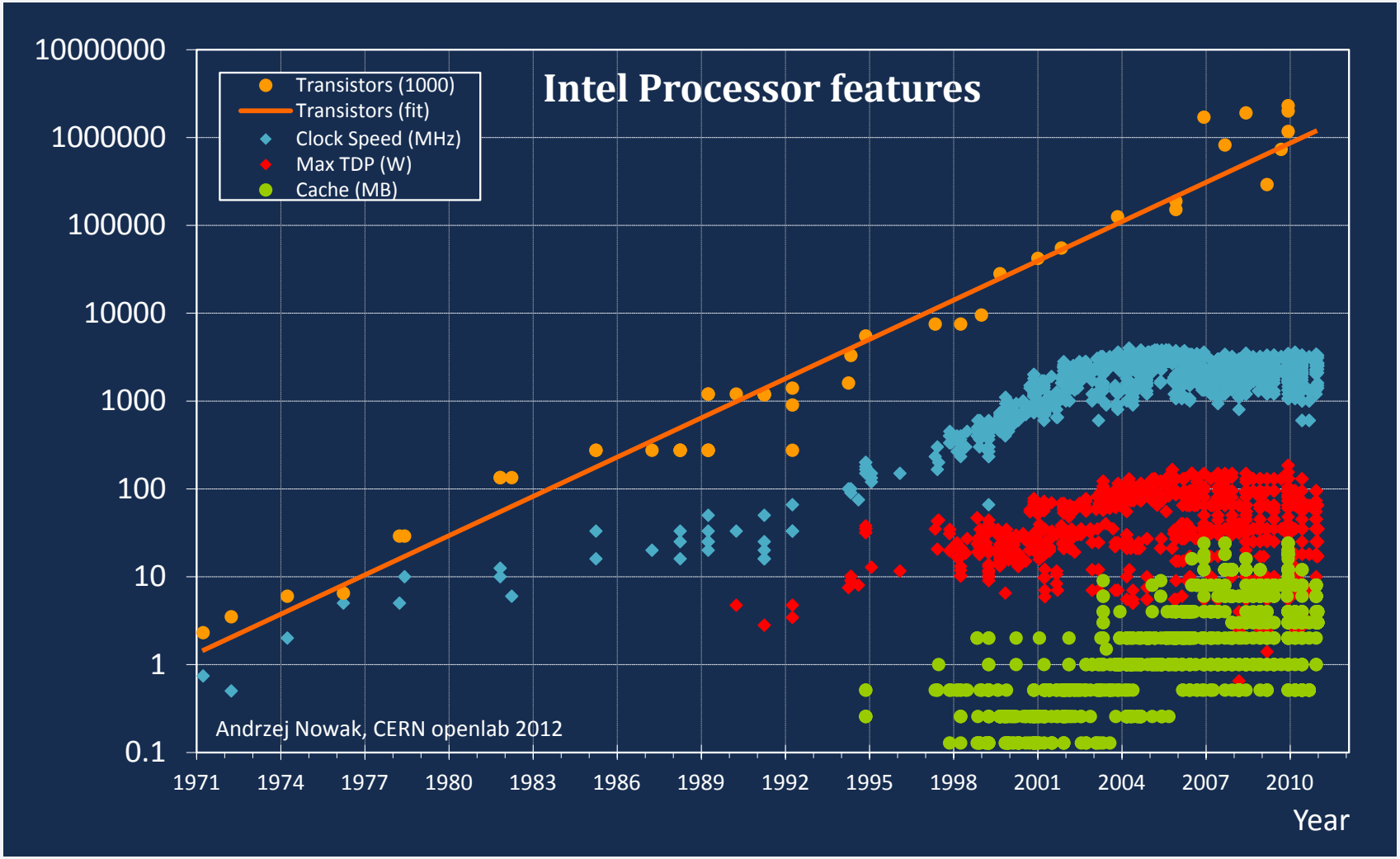
Current Trends in Computing Technology

Moore's Law — Exponentially Growing Number of Transistors



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Clock speed stagnates

- Limited by power consumption
- **Times of free speedup are over**

Performance increases along multiple dimensions

- Larger caches
- More powerful vector units
  - **Single Instruction, Multiple Data (SIMD)**
  - E.g. Advanced Vector Extension (AVX)
    - 256 bit register size
    - Parallel processing of 4 double-precision floating point values
- Growing number of cores per CPU
  - **Multithreading/processing**
  - Growth tapering of
    - Limited by interconnection (number of pins/pads)

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Performance increases along multiple dimensions (cont.)

- Growing number of CPU sockets in systems
  - Limited by reliability, networking, and cost
  - Efficiency decreases with system size
- Hybrid computing using more specialized hardware
  - **General-purpose computing on graphics processing units (GPGPU)**
  - Reconfigurable logic devices (FPGA)
  - Digital signal processors (DSP)
  - ...

Overall trend

- From multicore to **manycore**
- From parallel to **massively-parallel computing**

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How to Make Your Programs Run Faster?

Put the additional transistors to use!

- Utilize vector units in CPUs
- Parallelize software so that it runs on multiprocessor systems
  - Well-established programming models (*OpenMP, Intel TBB, OpenMPI, ...*)
- Exploit potential of **hybrid computing**
  - **GPGPU most promising**
    - Hardware-specific programming models (*CUDA, OpenCL*)
  - Potential game changer: Intel's Many Integrated Core (MIC) architecture (Xeon Phi)

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- Memory, disk, and network bandwidth grow with lower rate
- **Amount of transferred bytes per FLOP decreases**
- **Optimize memory access patterns**
- E.g. Intel Core i7 3960X
  - Cache miss: 167 clock cycles latency to fetch data from RAM
  - During the same time the AVX unit could perform
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Change of software-development paradigm

- **Merge two design philosophies**
  1. Design software independent of hardware
  2. Optimize software for specific hardware
- Hardware is a moving target $\Longrightarrow$ longevity issues
- Tradeoffs between performance and flexibility/programmability
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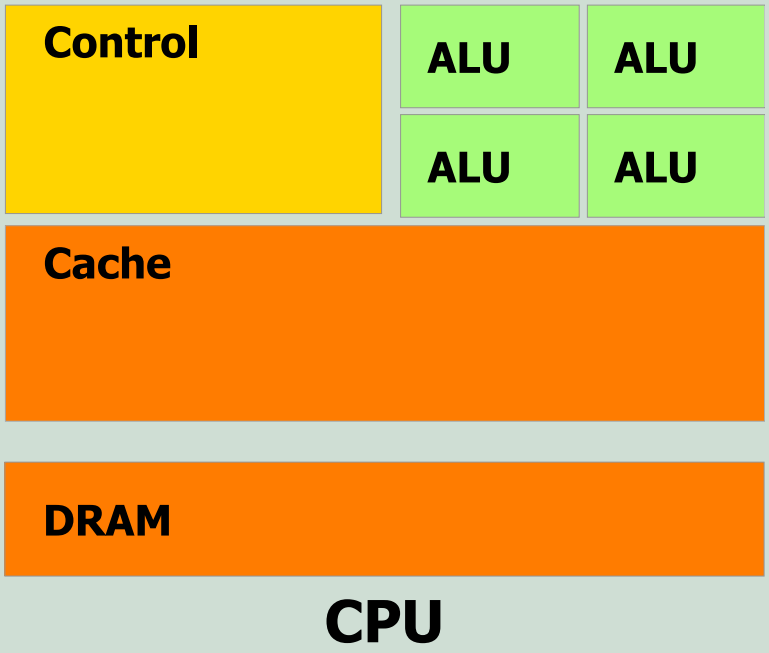
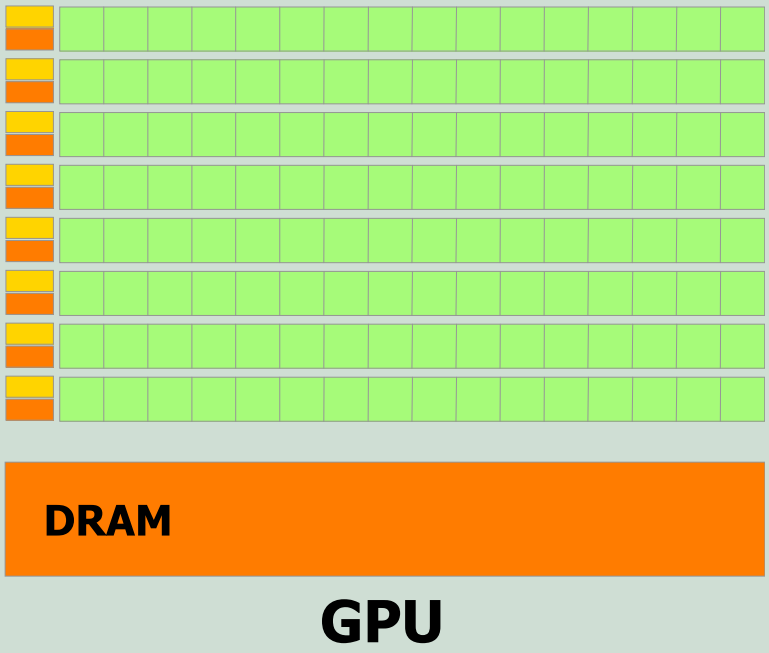
Why GPGPU?

Central Processing Unit vs. Graphics Processing Unit





- Large fraction of die devoted to data caching and flow control
- Most part of die devoted to data processing

Why GPGPU? Price per GFLOPS!

Central Processing Unit	vs.	Graphics Processing Unit
• General-purpose; not optimized for specific task		• Optimized for highly parallelizable problems
Intel Core i7 3960X		**nvidia GeForce GTX 680**
• 6 cores @ 3.3 GHz		• 1536 cores @ 1 GHz
• Max. processing power		• Max. processing power
– Single precision: 158 GFLOPS		– Single precision: 3000 GFLOPS
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Up to now mostly via low-level interfaces

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Recent developments

- Higher-level interfaces
  - *CUDA* : supports some C++ features (simple objects, templates)
  - *Thrust* : CUDA-based C++ template library
- Libraries for heterogeneous computing (CPU + GPU)
  - *OpenCL* : GPUs and x86 multicore CPUs
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GPGPU landscape is very dynamic

- New hardware generation with every ≈ 1.5 y
- Rapidly evolving software environment

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The Computational Challenges of PWA

Main challenges

- Huge data sets from existing and future experiments
  - BESIII, COMPASS, GlueX, Panda, ...
- Huge model space
  - Exploration requires many PWA fits $\mathcal{O}(10^4 \ldots 10^5)$
- More complex and computationally expensive models

Two main bottlenecks

1. Calculation of decay amplitudes $A_{\text{wave}}(\tau)$
   - Need to calculate $\mathcal{O}(100)$ complex amplitudes for each event
2. Unbinned likelihood fit
   - Fits with $\mathcal{O}(10^6)$ events

Both problems

- Very floating-point intense
- Easy parallelizable (events are independent)

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  - Amplitude code has to be rewritten
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Likelihood computation

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- IT industry moves to massively-parallel architectures
  - In principle ideal for PWA analyses
  - Leveraging this potential requires development work
    - Optimize critical software parts for specific hardware
  - At the moment GPGPUs have best performance/price ratio
    - Speedups between 20 $\times$ and 150 $\times$ seen in real analyses
    - Hard- and software still evolving
    - High-level programming interfaces and libraries for heterogeneous computing started to emerge
- Examples for implementations available on the web
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