
ATLAS Read Out Driver VMEbus Implementation

Recommendations of the
Detector Interface Group
ROD Working Group*

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1. INTRODUCTION

This document contains the recommendations of the ATLAS DIG ROD Working Group for a minimal subset of the features described in the VME64 and VME64x specifications essential for the correct functioning of the VMEbus interface of the ATLAS Read Out Drivers (ROD). The aim is to allow a common approach to the ROD to ROD Controller communication software and to ensure interoperability between the RODs and any COTS components in the ROD systems, particularly the SBCs used as ROD crate controllers, as well as with the subracks ("crates").

The document also contains additional information on important aspects of the implementation of the ROD systems.

1.1 Scope

This document is not intended to be exhaustive and in no way attempts to replace a thorough reading of the relevant specifications. A thorough familiarity with the specification documents is assumed.

1.2 Classification

The DIG ROD WG classifies the various optional features described in the specification documents:

- **Mandatory** - required to be implemented in the RODs for reasons of good engineering practice, interoperability and compatibility with the communication software.
- **Preferred** - recommended for use in the ROD,
- **Optional** - the ROD designer may choose to implement them for specific requirements,
- **N/a** - Not applicable. Usually associated with 3U VMEbus functionality,
- **Reserved** - not to be used.

Any divergences in the classification from a strict implementation of the VME64 and VME64x specifications are noted.

2. MECHANICAL & ELECTRICAL ENHANCEMENTS

2.1 VME64x Additional Features

Compared to VME64 the only additional mandatory feature in VME64x is the use of 160 pin connectors whose extra pins are used for additional power and grounds, slot geographical addressing, live insertion and a test and maintenance bus. VME64x also calls for a number of mechanical and electrical enhancements (specified in IEEE1101.10) designed to improve the reliability and compatibility of VMEbus systems. The additional features described in VME64x are classified in Table 1.

Table 1. VME64x Additional Features - Classification

VME64x Feature	Classification	Reference	Notes	
160 pin P1 & P2 connectors	Mandatory	VME64x		
EMC front panel		VME64x	Good practice. ESD discharge clips are specified in the ATLAS standard subrack.	
ESD strips on modules and discharge clips on card guides			Required by the increased insertion force of the 160 pin connectors and essential in 9U systems.	
Injector/extractor/ locking handles (with optional micro-switch - see Appendix C).			For electrostatic discharge and front-panel alignment when EMC gaskets are used.	
Multi-function alignment pin			For system initialisation and standard set-up and control (see Section 3.4).	
Slot geographical address			Good practice.	
CR/CSR definitions			ROD WG	Power at 3.3V will be available in the ATLAS standard subrack.
Extra grounds				For on-board power conversion. Power at 48V will be available in the ATLAS standard subrack.
+3.3 V power	The VPC may be used for additional power. See VME64x section 3.2.6.			
48 V power	To prevent contact with EMC gaskets on adjacent front panels when inserting or removing modules in a live insertion/extraction system			
+5 V pre-charge supply for live-insertion	Protection against the insertion of incompatible boards into inappropriate backplane positions. See Appendix D.			
Solder side covers with ESD protection	Preferred			
Keying				

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VME64x Feature	Classification	Reference	Notes
Test and maintenance bus	Optional	ROD WG	
95 pin P0 connector			The VME64x backplane in the ATLAS standard subrack will be equipped with a J0 and RJ0 connectors (unassigned pins).
2eVME enhanced data transfer protocol			Data transfers <160Mbyte/s. See Section 3 and Appendix B.

2.2 Other Additional Features

A number of other enhancements to VMEbus have been published subsequent to the publication of VME64x. These are classified in Table 2.

Table 2. Other Additional Features - Classification

Feature	Classification	Reference	Notes
Slave terminated and suspended transfers	Optional	ROD WG	Optimised slave readout. See Appendix A.
2eSST enhanced data transfer protocol			Data transfers >160 Mbyte/s. See Section 3 and Appendix B.
Live insertion & extraction			See Appendix C.
6U boards in 9U subracks			See Appendix E.

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3. BUS INTERFACE

3.1 Slave Interface

3.1.1 Capabilities

VME64 contains a number of rules designed to ensure compatibility between masters and slaves having various addressing and data transfer widths. Since the ROD system is unlikely to house any legacy devices with limited capabilities, these recommendations relax these rules. A32 D32 single cycle transactions are preferred and all other combinations of address and data widths made optional. A24 D32 single cycle transactions are mandatory to service the mandatory CR/CSR space required by these recommendations. A32 addressing is preferred for block transfers.

Commercially available SBCs will, in most cases, fully implement the VME64 requirements for address and data widths. Table 3 and Table 4 list the classifications of the various VMEbus DTB cycles, and Table 5 gives a complete list of the Slave's responses to AM Codes.

Table 3. Slave Interface Single Cycle Classification

Address Width	Data Width	Classification	Reference	Notes
A16	D08(O), D08(EO), D16, D32	Optional	ROD WG	Relaxation of VME64 ^(*)
A24	D32	Mandatory		CR/CSR space (AM 2F)
A24	D08(EO), D16, D32	Optional		Relaxation of VME64 ^(*)
A32	D08(EO), D16	Optional		Relaxation of VME64 ^(*)
A32	D32	Preferred		
A64	D08(EO), D16, D32	Reserved		Few masters implement A64
A40	Any	N/a		

^(*) VME64 Rules 2.76, 2.77

Table 4. Block Transfer and Enhanced Protocol Classification

Trans-action	Address Width	Data Width	Classification	Reference	Notes
A40BLT		Any	N/a		3U only
BLT		D08(EO)	Optional	ROD WG	
	A24, A32	D16			
	A24	D32	Preferred		
	A32				
MBLT	A24	D64	Optional		
	A32		Preferred		
	A64		Optional		
2eVME	A32	D64	Optional		
	A64		Reserved		Few masters implement A64
	A40	D32	N/a		3U only
2eSST	A32	D64	Optional	ROD WG	Few masters implement A64
	A64		Reserved		
	A40	D32	N/a	3U only	
2eSST Broadcast	A32	D64	Optional	ROD WG	Few masters implement A64
	A64		Reserved		
	A40	D32	N/a		3U only

Table 5. Slave AM Code Classification

AM Code	Function	Classification		
3F	A24 supervisory block transfer (BLT)	Optional		
3E	A24 supervisory program access			
3D	A24 supervisory data access			
3C	A24 supervisory 64-bit block transfer (MBLT)			
3B	A24 non privileged block transfer (BLT)			
3A	A24 non privileged program access			
39	A24 non privileged data access			
38	A24 non privileged 64-bit block transfer (MBLT)			
37	A40BLT	N/a (3U)		
36	Reserved	Reserved		
35	A40 lock command (LCK)	N/a (3U)		
34	A40 access			
33	Reserved	Reserved		
32	A24 lock command (LCK)	Optional		
31 - 30	Reserved	Reserved		
2F	Configuration ROM/Control & Status Register (CR/CSR)	Mandatory		
2E	Reserved	Reserved		
2D	A16 supervisory access	Optional		
2C	A16 lock command (LCK)			
2B - 2A	Reserved	Reserved		
29	A16 non-privileged access	Optional		
28 - 22	Reserved	Reserved		
21	2eVME / 2eSST (3U)	XAM		
		FF - 23	Reserved	Reserved
		22	A40/D32 broadcast 2eSST	N/a
		21	A32/D32 broadcast 2eSST	
		20 - 13	Reserved	Reserved
		12	A40/D32 2eSST	N/a
		11	A32/D32 2eSST	
		10 - 03	Reserved	Reserved
		02	A40/D32 2eVME	N/a
		01	A32/D32 2eVME	
		00	Reserved	Reserved

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AM Code	Function	Classification		
20	2eVME/ 2eSST (6U)	XAM		
		FF - 23	Reserved	Reserved
		22	A64/D64 broadcast 2eSST	
		21	A32/D64 broadcast 2eSST	Optional
		20 - 13	Reserved	Reserved
		12	A64/D64 2eSST	
		11	A32/D64 2eSST	Optional
		10 - 03	Reserved	Reserved
		02	A64/D64 2eVME	
		01	A32/D64 2eVME	Optional
		00	Reserved	Reserved
1F - 10	User defined	Optional		
0F	A32 supervisory block transfer	Preferred		
0E	A32 supervisory program access			
0D	A32 supervisory data access			
0C	A32 supervisory 64-bit block transfer (MBLT)			
0B	A32 non-privileged block transfer (BLT)			
0A	A32 non-privileged program access			
09	A32 non-privileged data access			
08	A32 non-privileged 64-bit block transfer (MBLT)			
07 - 06	Reserved	Reserved		
05	A32 lock command (LCK)	Optional		
04	A64 lock command (LCK)	Reserved		
03	A64 block transfer (BLT)			
02	Reserved			
01	A64 single transfer access			
00	A64 64-bit block transfer (MBLT)			

3.1.2 Read-Modify-Write

Table 6. Read-Modify-Write Classification

Slave	Byte(0) RMW	Byte(1) RMW	Byte(2) RMW	Byte (3) RMW
D08(O)	N/a	Optional	N/a	Optional
D08(E0)	Optional	Optional	Optional	Optional
	Byte(0-1) RMW		Byte(2-3) RMW	
D16	Optional		Optional	
	Byte(0-3) RMW			
D32	Preferred			
MD32	N/a			

3.1.3 Unaligned Transfers

Table 7. Unaligned Transfer Classification

Slave	Classification
D08(O), D08(E0), D16	N/a (only D32 slaves can perform unaligned transfers)
D32	Optional
MD32	N/a

3.1.4 Address-Only & Lock Capability

Table 8. Address Only Cycles

Cycle	Classification	Notes
ADO, ADOH	Reserved	It is unlikely that the ROD controller will generate ADO or ADOH cycles.

3.2 Master Interface

3.2.1 General

The RODs will, in general, have slave-only capability. In the event that a master capability is required, the following points are worthy of note:

1. The system arbiter and other "slot 1 functions" will normally be available in the ROD crate controller.
2. Many SBCs with internal buses (typically PCI) are incapable of resolving potential deadlock conditions, which can arise in multi-master (multi-arbiter) systems.

3.3 Interrupts

3.3.1 Interrupter

The ROD WG strongly recommends the implementation of an interrupter on all RODs to provide an efficient, low-overhead mechanism for communication with the ROD Controller (see Appendix B for a discussion on the system aspects of the use of interrupts as compared to polling).

ROD interrupter shall be capable of generating interrupts on all seven IRQ[x]* lines.

VMEbus interrupters will release their interrupt requests according to one of two strategies:

1. Release On Register Access – RORA
The IRQn* line is released following a specific read or write performed on a register in the slave associated with the interrupter.
2. Release On Acknowledge – ROACK
The IRQn* line is released automatically during the interrupt acknowledge cycle.

The RORA strategy requires a data transfer cycle and was included in the VME64 specification for reasons of backward compatibility. Refer to Table 9.

Table 9. Interrupt Release Strategy

Interrupter	Classification	Reference	Notes
RORA	Reserved	ROD WG	ROACK is the more efficient interrupt release strategy
ROACK	Preferred		

Table 10. Status id Classification

Status Id	Classification	Reference	Notes
D08(O)	Preferred	ROD WG	It is unusual to find a VMEbus interrupt handler capable of handling Status ids of more than 8 bits.
D16, D32	Reserved		

3.3.2 Interrupt Handler

It is unlikely that a ROD will need to handle interrupts. If an interrupt handler is implemented it shall be capable of servicing interrupts on all seven IRQ [x]* lines.

3.4 Geographical Addressing

Geographical addressing (see VME64x Section 3.2.11) is mandatory for the ATLAS ROD implementation.

At power-on in normal operation or after any reset operation, bits [7:3] of the Base Address Register will be loaded with the board's geographic address (see Table 11 and Table 15). These bits correspond to bits A[23:19] of the CR/CSR addresses. The system monarch may then locate the modules in the subrack in CR/CSR space and, if required, can remap the base address

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by reloading the BAR with an appropriate value. Address switches or jumpers may be implemented on the RODs in addition to geographical addressing for backwards compatibility with VME64 backplanes (see VME64x Permission 3.6).

VME64x recommends the parity checking of the geographical address (VME64x Recommendation 3.8).

VME64 specifies Auto Slot ID as a mechanism for the pseudo-geographical addressing of modules. It has been superseded by the VME64x slot geographical addressing and should not be implemented.

Table 11. Base Address Register

Bits [7:3]	Bits [2:0]	Byte	Notes
0	0	00	Auto-Slot id
1	0	08	Module in slot 1
2	0	10	Module in slot 2
3	0	18	Module in slot 3
4	0	20	Module in slot 4
5	0	28	Module in slot 5
6	0	30	Module in slot 6
7	0	38	Module in slot 7
8	0	40	Module in slot 8
9	0	48	Module in slot 9
A	0	50	Module in slot 10
B	0	58	Module in slot 11
C	0	60	Module in slot 12
D	0	68	Module in slot 13
E	0	70	Module in slot 14
F	0	78	Module in slot 15
10	0	80	Module in slot 16
11	0	88	Module in slot 17
12	0	90	Module in slot 18
13	0	98	Module in slot 19
14	0	A0	Module in slot 20
15	0	A8	Module in slot 21
1E	0	F0	"Amnesia" address - GA parity error detected.

3.4.1 Configuration Register (CR) Space

Logical Address Remapping

The features of the VME64x CR/CSR space make possible the assignment of logical addresses to the slave without the use of DIP-switches or other error-prone methods.

The Geographical Address of the module (its slot number) is mapped into the upper five bits of the Base Address Register (see Table 11 and Table 15), thereby placing the 512kByte space of the board uniquely in the total CR/CSR space. The system monarch may then assign logical addresses to up to 8 internal functions by writing to the ADER registers in the CSR (see also Table 15). The board's address decoders then use these values for comparison during VMEbus address broadcast cycles.

Table 12. Configuration ROM Assignments – Classification

Notes

1. CR/CSR space may be accessed with D08(O), D08(E0), D16 and D32 cycles (one, two or four bytes wide). The data in the CR is contained in every fourth byte so when reading from the CR with D32 cycles, the relevant data will be in the low order byte.
2. All undefined and reserved locations shall be read as zero.

Address Offset	Bytes	Value	Definition	Classification	Refer
0x03	1		Checksum	Mandatory	VME64 Table 2-32
0x07 - 0x0F	3		Length of ROM to be check-summed		
0x13	1	Value	CR data access width		
0x17	1	Value	CSR data access width		
0x1B	1	02	VME64x CR/CSR space		VME64x Table 10-12
0x1F	1	43	ASCII C		VME64 Table 2-32
0x23	1	53	ASCII R		
0x27 - 0x2F	3	08 00 30	Manufacturer's ID (CERN 080030 ₁₆ ¹)		
0x33 - 0x3F	4		Board ID ²		
0x43 - 0x4F	4		Revision ID		
0x53 - 0x5B	3		Pointer to a null terminated ASCII string		
0x5F - 0x7B	8	0x00	Reserved	Reserved	
0x7F	1	0x00	Program ID code (not used)	Mandatory	

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¹ IEEE Organizationally Unique Identifier (OUI) - see <http://standards.ieee.org/regauth/oui/index.shtml>. The CERN value is given as an example.

² The ATLAS Technical Coordination will issue Board Ids. A register of ids will be kept on the ATLAS web site at <http://atlas.web.cern.ch/Atlas/GROUPS/DAQTRIG/DIG/ROD/>

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Address Offset	Bytes	Value	Definition	Classification	Refer
0x83 - 0x8B	3		User Configuration ROM - offset to BEG_USER_CR	Optional	VME64x
0x8F - 0x97	3		User Configuration ROM - offset to END_USER_CR		
0x9B - 0xA3	3		User Configuration RAM - offset to BEG_USER_CRAM		
0xA7 - 0xAF	3		User Configuration RAM - offset to END_USER_CRAM		
0xB3 - 0xBB	3		User Control and Status Register - offset to BEG_USER_CSR		
0xBF - 0xC7	3		User Control and Status Register - offset to END_USER_CSR		
0xCB - 0xD3	3		User Serial Number - BEG_USER_CR		
0xDF	3		End User Serial Number - END_USER_CR		
0xE3	1		Slave characteristics		
0xE7	1		User defined slave characteristics	Optional	
0xEB	1		Master characteristics	Mandatory if master functions implemented. (Table 14)	
0xEF	1		User defined master characteristics	Optional	
0xF3	1	Value	Interrupt handler characteristics	Mandatory (if IH implemented)	
0xF7	1	Value	Interrupter capabilities	Mandatory (if Interrupter implemented)	
0xFB	1	0x00	Reserved	Reserved	
0xFF	1		CRAM access width	Optional	

Contd. ➔

Address Offset	Bytes	Value	Definition	Classification	Refer
0x103	1	0x00 ³	Function 0 data access width	Mandatory	VME64x
0x107	1		Function 1 data access width	Optional	
0x10B	1		Function 2 data access width		
0x10F	1		Function 3 data access width		
0x113	1		Function 4 data access width		
0x117	1		Function 5 data access width		
0x11B	1		Function 6 data access width		
0x11F	1		Function 7 data access width		
0x123 - 0x13F	8	Value	Function 0 AM code mask	Mandatory	
0x143 - 0x15F	8		Function 1 AM code mask	Optional	
0x163 - 0x17F	8		Function 2 AM code mask		
0x183 - 0x19F	8		Function 3 AM code mask		
0x1A3 - 0x1BF	8		Function 4 AM code mask		
0x1C3 - 0x1DF	8		Function 5 AM code mask		
0x1E3 - 0x1FF	8		Function 6 AM code mask		
0x203 - 0x21F	8		Function 7 AM code mask		
0x223 - 0x29F	32	Value	Function 0 XAM code mask	Mandatory (if (2eVME, 2eSST implemented))	
0x2A3 - 0x31F	32		Function 1 XAM code mask	Optional	
0x323 - 0x39F	32		Function 2 XAM code mask		
0x3A3 - 0x41F	32		Function 3 XAM code mask		
0x423 - 0x49F	32		Function 4 XAM code mask		
0x4A3 - 0x41F	32		Function 5 XAM code mask		
0x523 - 0x59F	32		Function 6 XAM code mask		
0x5A3 - 0x61F	32		Function 7 XAM code mask		

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³ Value 0 indicates that the feature is not implemented. Necessary unless a VME64 compliant set of data transfer cycles is accepted (see VME64x Table 10-3).

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Address Offset	Bytes	Value	Definition	Classification	Refer
0x623 - 0x62F	4		Function 0 addr. decoder mask	Mandatory	VME64x
0x633 - 0x63F	4		Function 1 addr. decoder mask	Optional	
0x643 - 0x64F	4		Function 2 addr. decoder mask		
0x653 - 0x65F	4		Function 3 addr. decoder mask		
0x663 - 0x66F	4		Function 4 addr. decoder mask		
0x6730x67F	4		Function 5 addr. decoder mask		
0x6830x68F	4		Function 6 addr. decoder mask		
0x6930x69F	4		Function 7 addr. decoder mask		
0x6A3 - 0x6AB	3	00	Reserved	Reserved	
0x6AF	1	Value	Master data access width	Optional	
0x6B3 - 0x6CF	8	Value	Master AM capability		
0x6D3 - 0x74F	8	Value	Master XAM capability		
0x753 - 0xFFFF	555	00	Reserved	Reserved	

Table 13. Slave Characteristics

Bit	Value	Meaning	Classification
7	0	Supports unaligned transfers	Optional
	1	Does not support unaligned transfers	
6	0	Supports read-modify-write transfers	
5	0	Supports address-only cycles	
	1	Does not support address-only cycles	
4	0	Supports address-only cycles with handshake	
	1	Does not support address-only cycles with handshake	
3	0	Supports RETRY* and RESP*	
	1	Does not support RETRY* and RESP*	
2	1	Implements P2 connector	
1	0	Uses TTL transceivers	Optional
	1	Uses ETL transceivers	
0	0	Reserved	Reserved

Table 14. Master Characteristics

Bit	Value	Meaning	Classification
7	0	Supports un-aligned transfers	Optional
	1	Does not support un-aligned transfers	
6	0	Supports read-modify-write transfers	
	1	Does not support read-modify-write transfers	
5	0	Supports address-only cycles	
	1	Does not support address-only cycles	
4	0	Supports address-only cycles with handshake	
	1	Does not support address-only cycles with handshake	
3	0	Supports RETRY* and RESP*	
	1	Does not support RETRY* and RESP*	
2	1	Implements P2 connector	Mandatory
1	0	Uses TTL transceivers	Optional
	1	Uses ETL transceivers	
0	0	Reserved	Reserved

3.4.2 Control and Status Register (CSR) Space

Table 15. CSR Space Assignment

Reference: VME64x Table 10-13

Address	Definition	Size (bytes)	Classification	Refer
0x7FFFF	CR/CSR Base Address Register (BAR)	1	Mandatory	VME64
0x7FFFB	Bit set register	1	See Table 16	
0x7FFF7	Bit clear register	1	See Table 17	
0x7FFF3	CRAM_OWNER register	1	Optional	VME64x
0x7FFE7	User-defined bit set register	1		
0x7FEB	User defined bit clear register	1		
0x7FE3 - 0x7FE7	Reserved	2	Reserved	
0x7FD3 - 0x7FDF	Function 7 ADER	4	Optional	
0x7FC3 - 0x7FCF	Function 6 ADER	4		
0x7FB3 - 0x7FBF	Function 5 ADER	4		
0x7FA3 - 0x7FAF	Function 4 ADER	4		
0x7F93 - 0x7F9F	Function 3 ADER	4		
0x7F83 - 0x7F8F	Function 2 ADER	4		
0x7F73 - 0x7F7F	Function 1 ADER	4		
0x7F63 - 0x7F6F	Function 0 ADER	4	Mandatory	ROD WG
0x7FC0 - 0x7F5F	Reserved	216	Reserved	VME64x

Table 16. Bit Set Register

Refer VME64x Table 10-6

Bit	Value	Write	Classification	Read	Classification	Refer
7	1	Place module in reset mode	Optional	Module in reset mode	Mandatory	VME64
	0	No effect		Module not in reset mode		
6	1	Enable SYSFAIL driver		SYSFAIL driver enabled		
	0	No effect		SYSFAIL driver disabled		
5	1	Set module fail (test)		Module failed		
	0	No effect		Module not failed		
4	1	Enable module		Module enabled		VME64x
	0	No effect		Module disabled		
3	1	Set BERR* flag		Module issued BERR*		
	0	No effect		Module did not issue BERR*		
2	1	Set CRAM_OWNER (test)	CRAM owned	Optional		
	0	No effect	CRAM available			
1	1	Reserved	Reserved	Reserved		
	0	No effect	Optional			
0	1	Reserved	Reserved			
	0	No effect	Optional			

Table 17. Bit Clear Register

Refer VME64x Table 10-7

Bit	Value	Write	Classification	Read	Classification	Refer
7	1	Remove module from reset mode	Optional	Module in reset mode	Mandatory	VME64
	0	No effect		Module not in reset mode		
6	1	Disable SYSFAIL driver		SYSFAIL driver enabled		
	0	No effect		SYSFAIL driver disabled		
5	1	Clear module fail		Module failed		
	0	No effect		Module not failed		
4	1	Disable module		Module enabled		
	0	No effect		Module disabled		
3	1	Clear BERR* flag		Module issued BERR*		
	0	No effect		Module did not issue BERR*		
2	1	Clear CRAM_OWNER		CRAM owned	Optional	VME64x
	0	No effect		CRAM available		
1	1	Reserved		Reserved	Reserved	
	0	No effect		Optional		
0	1	Reserved	Reserved			
	0	No effect	Optional			

Appendix A. SLAVE TERMINATED AND SUSPENDED TRANSFERS

VME64x and associated documents describe mechanisms, which allow a slave to terminate a data transfer, and thus allow the efficient operation of a master having no prior knowledge of the quantity of data to be transferred.

A.1 2eVME, 2eSST

Slaves can terminate a block transfer at any time by simply asserting **RETRY*** followed by **BERR***, the master having given the slave its block size limit in the address broadcast (beat count).

Similarly, slaves can suspend a transfer for later resumption by asserting **RETRY*** and toggling **DTACK***.

Refer to Appendix C and VME64x Section 11.1.7.

A.2 Chained Block Transfers

The CBLT mechanism described in the VME64xP specification provides a mechanism for the read-out of contiguous set of modules with one block transfer in a single-master environment.

Refer to VME64xP Appendix E.

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Appendix B. POLLING AND INTERRUPTS

Whether interrupts are implemented or not in the ROD VMEbus interface has consequences for the functioning of the software processes in the ROD Crate Controller SBC, and requires careful study. It is likely that several processes, accessing VMEbus, will be running concurrently on the ROD Crate SBC such as the online controller skeleton communicating with the RODs to provide run control, and error reporting functionality. Another process extracts data fragments from the RODs and makes them available for local processing, remote sampling or local storage (see DIG ROD Crate presentations at the ATLAS week in BNL, June 2001).

If the RODs cannot produce VMEbus interrupts, these processes have to poll the RODs and will, therefore, compete for CPU time and VMEbus access which will have an impact on the performance of the ROD Crate Controller software. The conventional way to solve this problem is to use interrupts: the RODs will signal when they need attention e.g. that a message is ready, an error has occurred or a data fragment is available. In particular the use of interrupts would be appropriate for the online controller, which has a low frequency interaction with the RODs,

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Appendix C. 2eVME AND 2eSST DATA TRANSFER PROTOCOLS

In certain modes of operation, the RODs may need to transfer large quantities of data at relatively high rates.

For rates of greater than the approximate 60 Mbyte/s practical limit of VME64 multiplexed block transfers (MBLT), the optional 2eVME two-edged data transfer protocol, and the 2eSST two-edged source synchronous protocol, offer significant improvements.

The 2eVME protocol, described in the VME64x specification, permits a doubling of the theoretical maximum bandwidth of VME64 from 80Mbyte/s to 160Mbyte/s.

The 2eSST protocol is based on 2eVME. It was specified after the publication of VME64x and exists in draft form only. With the appropriate transceiver and backplane technology and a master having the necessary internal architecture, for 6U (and 9U) modules 2eSST specifies rates of 160, 267 and 320 Mbyte/s. Future enhancement is foreseen, given the availability of adequate backplanes and transceivers.

In addition, the synchronous nature of the protocol has allowed the specification of a data broadcast (and multicast) mode of operation.

To date, only a few commercial implementations of the 2eVME and 2eSST enhanced protocols have been announced.

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Appendix D. LIVE INSERTION AND EXTRACTION

The ANSI/VITA 3-1995 "Board Level Live Insertion for VMEbus" describes mechanisms for the insertion and extraction of modules from a VMEbus system without removing power from the subrack.

At the time of writing, the system aspects of "high availability", where the system software is able to recognise and deal with the removal and addition of modules have not been addressed except in outline draft, form (see the VME64x Live Insertion System Requirements VITA 1.4 - Draft 0.6 December 1998).

The need for high availability in the ROD subracks is debatable and, apart from the challenging software aspects, would require the use of backplane transceivers designed with a pre-charge mechanism to allow glitch-free insertion. However, the ability to be able to remove and insert modules without powering down the whole system, with the consequent need to reload and re-initialise software in all modules, can be achieved relatively simply. It will have a positive impact on in-service faultfinding and repair time, as well as during the hardware development phase.

Leaving aside the system aspects, ANSI/VITA3, Section 6.3 describes three implementation options:

1. Mount live insertion logic on a short "stub" board (buffer or paddleboard) positioned between a standard backplane and a standard VMEbus board.
2. Place the live insertion logic on an active backplane.
3. Mount the live insertion logic on the connector.

Solution 1 is commercially available, but is only practical for test purposes. Solution 3 may be possible, but no known implementations exist and would probably be expensive and be detrimental to the connector lifetime. Solution 2 is described in VITA1.4. It is also commercially available and in conjunction with a suitable power controller⁴ on the module will allow for the safe insertion and extraction of modules to and from a powered subrack

D.1 Implementation

D.1.1 Backplane Control Signals

VME64x specifies two pins, LI/O* and LI/I*, to be used for live insertion / extraction control. The VITA 1.4 199x "VME64x Live Insertion System requirements" draft document specifies their use as follows:

- **LI/O*** - driven true by the VME64x module to signal when it is capable of correctly handling the VMEbus daisy-chain signals (BGn* and IACKIN*/IACKOUT*),

⁴ Example: Linear Technology LTC1643-1,
http://www.linear.com/prod/prod_home.html?product_family=hotswap
http://www.linear.com/pub/q_srch.html?target=1643&pub_type=All&product_family=All

Note: Modules not equipped with the live insertion/extraction mechanism are advised to connect LI/O* to GND

- **LI/I*** - The LI/I* is an active low input signal to a VME64x LI module that is used to enable (high) and disable (low) its power control logic. The LI/I* can be either floating or activated by a radial power control module for centralised power control. A resistor pulls it up to VPC on the VME64x module.

D.1.2 Typical Insertion Sequence

1. All backplane activity is stopped, manually or otherwise.
2. The module enters the card-guide and the electrostatic discharge (ESD) sequence takes place,
3. The module connector contacts mate with the (long) GND and VPC pins on the backplane,
4. A VMEbus interface reset signal is generated,
5. The VMEbus interface ASICs that are powered by VPC stabilise and reset,
6. The VMEbus signal pins are pre-charged.
7. VMEbus signal pins and remaining power pins contact the backplane,
8. The module's power controller circuit is itself powered,
9. The injector/extractor handles are seated and handle micro-switch closes,
10. When the module's power controller circuit senses that the LI/I* signal is true (low) and the micro-switch is closed, it proceeds with the module's power-up sequence.
11. The module's logic reset signal is generated. (BRn* and INTn* are inhibited),
12. VMEbus interface ASICs and transceivers are enabled,
13. When the module has completed its internal initialisation, it drives LI/O* true (low) to signal to the backplane logic to relinquish control of the daisy-chain signals.

D.1.3 Typical Extraction Sequence

1. All backplane activity is stopped, manually or otherwise,
2. The injector/extractor handles are unseated and the handle micro-switch opens
3. The module drives LI/O* high and hands control of the daisy-chain signals to the backplane logic,
4. VMEbus interface ASICs and transceivers are disabled, and an internal reset is made,
5. The module's power controller circuit proceeds with the module's power-down sequence,
6. The module is removed from the card guide and breaks contact with the ESD contact.

Appendix E. KEYING

Chapter 7 of the VME64x specification describes the optional application of the keying mechanism specified in IEEE1101.10. Section 1 of this document classifies keying as preferred for use in the ROD system.

The overhead involved in implementing keying is minimal, since the ATLAS standard subracks are specified with keying chambers and the necessary multi-function alignment pin and front panels are readily available with the keying mechanism.

Keying in a complex system has a number of advantages, such as:

- Protection against potentially dangerous installation of boards into inappropriate backplane slots (with, for instance, special power voltages on I/O pins),
- Foolproof board exchange by inexperienced personnel.

The system architect has to invent and manage the particular keying scheme and to ensure its correct implementation.

The ROD WG recommends that the ROD systems implement the VME64x keying mechanism.

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Appendix F. 6U BOARDS IN 9U SUBRACKS

The use of 6U x 160mm boards, such as the ROD Controller (normally a COTS SBC) in 9U x 400mm subracks, poses some practical problems.

Two solutions are possible: the direct insertion of the 6U board into the 9U subrack's backplane, or the use of a 6U to 9U adapter.

The ATLAS standard 9U subrack will be available with up to 4 6U slots grouped to the left of the subracks (slots 1 to 4) for direct backplane insertion, in addition, 6U to 9U active adapters are commercially available.

F.1 Direct Backplane Insertion

The advantages of direct backplane insertion are:

1. Best electrical and signal transmission environment,
2. Least expensive solution.

The disadvantages are:

1. The need for special mechanics in the subrack to support and guide the 6U board,
2. The possible loss of slots owing to the installation of the 6U mechanics,
3. The 6U board's front panel is "buried" inside the 400mm deep card-cage.

F.2 6U to 9U Adapter

The advantages of using a 6U to 9U adapter are:

1. The 6U board's front panel will be flush with those of adjacent 9U modules,
2. No loss of slots,
3. The additional, otherwise unused, board space on the adapter could potentially be used for system functions.

The disadvantages are:

1. For correct signal transmission on the backplane given the long, out of specification, signal stub lengths, the adapter must provide electrical buffering (i.e. the adapter must be "active")
2. The adapter will be relatively costly and will add complexity to the system.

F.3 Recommendations

The ROD WG recommends that direct backplane insertion be used whenever possible, and 6U to 9U adapters only be used if easy access to COTS front panels is essential, or when it is necessary to intersperse 6U boards between 9U boards.

Appendix G. RELEVANT STANDARDS

The standards listed below are relevant to this document.

1. VME64 (ANSI VITA 1-1994, ISO/IEC 15776)5
2. VME64 Extensions "VME64x" (ANSI VITA 1.1-1997)
3. VME64 Extensions for Physics and other Applications "VME64xP" (ANSI VITA 23-1998)
4. 2eSST Source Synchronous Transfer protocol (VITA 1.5-1999 Draft standard for trial use)
5. VME64x Live Insertion System Requirements (VITA 1.4 Draft 0.6 December 1998)
6. Board Level Live Insertion for VMEbus (ANSI/VITA 3-1995)
7. IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors (IEEE1101.1-1991)
8. IEEE Standard for additional Mechanical Specifications for Microcomputers using the IEEE 1101.1 Equipment Practice (IEEE1101.10-1996)
9. IEEE Standard for Mechanical Rear Plug-in Units Specifications for Microcomputers Using the IEEE 1101.1 and the IEEE 1101.10 Equipment Practice (IEEE1101.11-1998)

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⁵ ANSI/VITA specifications are available from the VMEbus International Trade Association (VITA), Scottsdale, Arizona, USA, URL <http://www.vita.com> or from the ATLAS web site at <http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/VMEbus/>

Appendix H. TERMINOLOGY

Unless otherwise defined below, the terminology used in this document corresponds to that described in the following documents:

- Appendix A of VME64 (ANSI VITA 1-1994, ISO/IEC 15776),
- Appendix A of VME64 Extensions "VME64x" (ANSI VITA 1.1-1997),
- Appendix A of ANSI/VITA 1.3-1997 VME64x 9U x 400mm Form Factor.

H.1 Additional Terminology

Card-cage	the mechanical unit that supports VMEbus or transition modules, providing mechanical alignment with respect to the backplane.
Control and monitoring	the subsystem providing for the remote and/or local monitoring and control of the functioning of the subrack.
Cooling unit	the subsystem providing the cooling for the electronic boards inserted in the subrack, which may also cool the power supply.
COTS	Commercial Off The Shelf - commercially available "catalogue" items.
Backplane	the unit carrying the VMEbus and, optionally, other signal paths and the power distribution.
Front (of subrack, etc.)	the front of the subrack is the face that receives VMEbus modules.
Module	the 3U, 6U or 9U electronic board together with a front panel, injector/extractor handles, alignment pin, ESD gaskets and strips, and mandatory and optional rear edge connectors for insertion into the backplane's rear mating connectors.
Power supply	the unit containing the power supplies required to power the electronic modules inserted in a subrack as well as for ancillary functions such as backplane termination.
SBC	Single Board Computers.
Rear (of subrack, etc.)	the rear of the subrack is the face that receives transition modules.
Subrack ("Crate")	the unit consisting of front and optional rear card-cages, backplane(s) mounted together with the card-cages and a means to connect power to the backplane(s).
VMEbus	used in this document as a generic term to denote VME64, VME64x and other related standards.