Pixel readout electronics development for ALICE PIXEL VERTEX and LHCb RICH


EP Division - CERN, Geneva

*Rome III INFN **INFN and Politecnico Bari ***Nikhef
Outline

◆ Previous full readout chips
  ■ Omega2
  ■ Omega3/LHC1

◆ Two testchips
  ■ 0.5 µm CMOS
  ■ 0.25 µm CMOS

◆ New chip for ALICE pixel and LHCb RICH
  ■ Chip description
  ■ Design for radiation tolerance
  ■ Design for testability
  ■ Design for uniformity

◆ Special issues

◆ Conclusions
- Binary position information
- **Pixel 75x500 \( \mu \text{m}^2 \), 64 rows by 16 columns**
- Leakage current sensing cell at the bottom of each column
- Internal delay per pixel (current deprived invertors), dead for twice the trigger delay
- Shift register readout after level 1 trigger
- Limited testability: only one test row at the top
- Two metal layers only: no shielding between electronics and detector
- ~ 80 transistors/pixel (Self Aligned Contact 3 \( \mu \)m technology)
- Dies at < 50krad
Pixel 50x500 \( \mu \text{m}^2 \), 128 rows by 16 columns

- Internal delay per pixel (current deprived invertors), front end reset after small fraction of the trigger delay
- Shift register readout after level 1 trigger
- All pixels can be tested electrically
- Third metal shield
- \( \sim 380 \) transistors/pixel (Self Aligned Contact 1 \( \mu \text{m} \) technology
- Dies at < 50krad
- Discriminator (see left) trade-off between threshold uniformity and speed
- Preamplifier feedback
Omega3 testability gave a wealth of information

Top-down threshold variation due to resistive drop fixed in correction run
3 bit delay adjust on half plane (~ 50 000 channels)

Before

After
Omega2 and Omega3 worked well
(CERN RD-19, WA97 and NA57)

Pixel Ladders
(6 chips)

Half plane ~ 50 000 sensing elements

LHC1: 2000 CMOS readout channels

WA97 NA57 Experiment
1.2 M channels
Two test chips in commercial submicron CMOS

- 2 columns of 64 pixels + 1 test pixel with analog outputs
- Radiation tolerant layout
- 2 by 5 mm²
- Full mixed mode circuit

LHC2TEST/ALICE1TEST
0.5 \( \mu \text{m} \) CMOS
25000 transistors

ALICE2TEST
0.25 \( \mu \text{m} \) CMOS
50000 transistors
Changes in front end

- DC level of input and output no longer coupled
- Leakage current compensation

Change in discriminator for speed, went to current comparator

Vref
\[ C_{fb} \]
IN
OUT

Vbias
Threshold setting

In
I_{out} to current comparator
0.5 µm test chip

Counts (pro mille)

Input (mV) (thresh. ~ 2100 el.)
- Ileak = 1.4 nA, noise ~ 180 e rms
- Ileak = 16 nA, noise ~ 210 e rms
- Ileak = 100 nA, noise ~ 330 e rms

Added delay (ns)

Input charge (electrons, uncalib.)
- threshold = 1650 el.
- threshold = 2000 el.
- threshold = 6400 el.

Leakage current compensation works
(for both signs of leakage)

Timewalk LHC compatible
0.5 µm test chip: evolution of Threshold and Threshold Variation with Xray Dose

Supply currents virtually unaffected during the irradiation!
Circuit dies around 1 Mrad because of transistor Vt-shifts which are still non-negligible in 0.5 µm

Confirmed for electrons, and for (cfr. F. Meddi et al.) gamma-rays and protons
$0.5\, \mu\text{m}$ test chip: conclusions

- Threshold dispersion too large: edgeless transistor show much larger mismatch (see left)
- $\Rightarrow$ need other front end topology
- Motivations to go deeper submicron:
  - Need more density
  - Will get even higher radiation tolerance
- Need for further modeling of edgeless transistors

Mismatch for edgeless transistors

cfr. G. Anelli et al.
0.25 \mu m testchip

- Eliminated the current mirror (cfr ISSCC 2000) and shrunk the front end from 260 \mu m to 125 \mu m
- Put synchronous delay (one column static, other dynamic) in the empty space and kept other logic identical to 0.5 \mu m version
- 50 \mu W per pixel
- Noise 220-250 e^{-} rms
- Threshold dispersion 160 e^{-} rms before 3 bit adjust, 25 e^{-} rms after
- Used three metals only
0.25 μm test chip: 10 keV X-ray Irradiation
Pixel Threshold, Threshold Dispersion and Noise Vs Total Dose

Supply currents virtually unaffected during the irradiation!
Proton irradiation in NA50

Threshold and noise on hit column after proton irradiation and 4 hour anneal @ room temperature

(Note: 1 mV = 100 e-)

3.6 x 10^{13} protons/4mm^2

=>

9 x 10^{14} protons/cm^2
Proton irradiation in NA50

Conclusions

- Also withstands non-uniform irradiation
- Did not see any evidence of hard failure, i.e. gate rupture...

Threshold change and noise after proton irradiation and 20 hour anneal @ room temperature

Note: 1 mV = 100 e-
Conclusions from test chips

Challenges for full chip

- Speed, threshold uniformity and radiation tolerance (total ionizing dose and single event upset) proven
- Need to further characterize enclosed devices
- Challenges for full readout chip:
  - Architecture for two different applications
  - Large occupancy in LHCb, need to minimize dead time
  - Readout (=digital activity) while being sensitive
  - Large chip
  - Large system: testability, uniformity
  - Design for radiation tolerance: design implications revisited
Two applications: pixel for tracking/vertex finding in ALICE

Minimal mass, thin sensors $\Rightarrow$ 12 000 e- most probable signal

Spatial resolution of 12 $\mu$m in $r-\phi$ $\Rightarrow$ 50 $\mu$m pixel pitch

1% average occupancy

Level-1 trigger: latency of 5.5 $\mu$s, few kHz rate, buffering on chip

Full event readout in 400 $\mu$s (deadtime about 10%), 10 MHz clock

Radiation tolerant to $\sim$ 500 krad
And... LHCb RICH: encapsulation of pixel chip-sensor assembly in HYBRID PHOTON DETECTOR for particle ID

- Single photons yield $5000e^-$ signal with 20kV accelerating potential
- 2.5mm x 2.5mm channel size, 5x demagnification $\Rightarrow$ $500\mu m \times 500\mu m$ granularity
- 8% maximum occupancy
- 40 MHz event rate, also readout clock
- 1MHz average Level 0 trigger rate
- Buffering of Level-0 triggered events (latency of 4 $\mu s$)
- Readout of triggered event in 900ns (deadtime $\leq 1\%$)
New 8000 channel chip: pixel

- Preamp
- Shaper filter
- Comparator
- Thres.
- Delay
- Coincidence logic
- 4-bit FIFO
- Data FF
- analog test input
- test FF
- th adj FFs
- mask FF
- R W
- strobe
- BCO
- C_in
Two applications: architectural solution

ALICE mode of operation
Two applications: LHCb mode of operation
Front End

- Differential to reject substrate and supply noise
- Closed loop complex poles for fast return to zero to be immune to pile-up of subsequent signals
Pixel Cell: digital part

Delay:
- stores a hit for duration of trigger latency
- latches the time-stamp of a hit from a periodic Gray-encoded pattern (modulo n) on an 8-bit bus

FIFO:
- Read/write addressable by Gray encoded bus

Risk of switching noise coupling into analog circuitry is reduced by:
- Gray encoding of patterns on buses
- Current starved logic cells
Pixel cell

- 125µm
- pre-amp (differential)
- shaper (differential)
- discriminator (+ fast-OR)
- 60µW static consumption
- 35µm
- 5 un-upsettable latches for configuration
  - test input on/off
  - pixel mask on/off
  - 3 bits of threshold adjust
- 265µm
- two digital delay units
- trigger coincidence logic
- 4-event FIFO buffer
- readout logic
- 6 metal layers
- 1500 transistors/pixel
- layout for radiation tolerance everywhere
Periphery and I/O

- Periphery contains:
  - Counters to generate timestamp
  - Counters to address FIFO buffers
  - 8-bit DACs to provide voltage and current references for analog circuitry and current-starved logic
- I/O pads: Single-ended: Gunning Tranceiver Logic (GTL)
  - Low swing
  - Slew rate control
- Separate supply for output buffers
- Multiple bonding pads for supply lines to reduce inductance and limit on-chip power supply bounce during switching
Design for testability

- Configuration of peripheral logic and pixel cells by means of JTAG serial interface -
  - allows both write and read of configuration settings (test, mask...)
  - reading back of analog levels (currents & voltages) generated by DACs
  - connectivity tests of chips on stave using boundary scan allows detection of bad chips on stave

- Every pixel can be addressed individually for testing using analog input
Very important fine print

- **Single event effects:**
  - Single event induced latch-up: radiation tolerant layout very effective also here
  - Single event upset: special SEU hardened flip-flops

- **Power distribution and voltage drops:**
  - Motivation for (late) decision to switch from 5 to 6 metal layers
  - Local mirroring of sensitive biases to reduce sensitivity to on-chip resistive drops

- **Digital to analog cross-talk:**
  - Slew rate control on all digital
  - Differential frontend
Conclusions

- Experience from omega2 and omega3/LHC1, and from the two test chips
- Commercial deep submicron CMOS allows:
  - High component density
  - Radiation tolerance
  - Good speed-power performance
- Full scale pixel readout chip designed
  - One chip for Alice pixel vertex and LHCb RICH
  - 8000 readout channels
  - 13 M transistors in 14 by 16 mm²
  - 6 metals
  - Testability and system integration
  - Uniformity
  - Important fine print
Conclusions

Basic building block in full readout chip:
8 pixels/12,000 transistors in 400 by 425 µm²