Preliminary draft

BaBar IFR TDC Board (*ITB*):

requirements and system description

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1. Timing measurement with the IFR

Accurate track reconstruction in the *BaBar* detector requires a precise determination of the instant of the bunch crossing corresponding to each event. This is necessary for the drift chamber to reconstruct the trajectories starting from measured values of drift time. The good properties of time resolution offered by RPC detectors can be profitably exploited to this end and can help in greatly reducing the amount of CPU time required [1].

A high resolution measurement of the impact time in the IFR can be also extremely beneficial in pattern recognition: as a matter of fact the interleaving connections of the front end electronic allows a coarse determination of the longitudinal coordinate (30-40 cm) using the "phi" hits in the barrel. A complete reconstruction of the shape of the hadronic showers is needed to identify charged and neutral hadrons detected in the IFR: any extra information, that one could get on pattern recognition/reconstruction is clearly of great importance.

Timing measurements can also be suitably used to get rid of "opposite sign" cross talk, as hits originating from it will occur in time later than the real hits.

Last but not least, timing will allow to get an handle on energy measurement of neutral hadrons, especially K_long, which in the direct B decay have a very soft momentum spectrum.

The IFR in *BaBar* consists of several layers (19 and 18 respectively for the barrel and the end-caps) of RPCs, for each of which a time resolution of about 2 ns is estimated from measurements with a similar detector in L3 experiment. Each *Front End Card* (*FEC*) equipping the IFR reads 16 strips individually and also provides a *FAST-OR* output: this signal can be used for the time determination by feeding it into an appropriately designed TDC board.

The present document sets the requirements for the *IFR TDC Board* (*ITB*), describes its functionality and presents a first proposed design.

2. Requirements specifications

The ITB must satisfy the following requirements.

Board functionality:

1) total number of channels: 96;
2) adherence to *BaBar* transmission protocol as specified in [2]: in particular must recognize (global) run-time commands (*Clear Readout, Sync*, *L1 Trigger Accept*, *Read Event*, *Calibration Strobe*);
3) event buffer of at least 4 events depth;

TDC features:

1) timing resolution: ≤ 1 ns;
2) double hit resolution on single channel: ≤ 100 ns;
3) maximum hit rate on single channel (average): ≥ 10 kHz;
4) dynamic range: ≥ 10 μs
5) continuous mode operation (i.e. no dead time during *Read Event*);
6) selective readout of data within proper time window (no common START/STOP signals);
7) noisy channels masking capability;
8) long term stability (including temperature effects).

3. Choice of the TDC chip

Two different TDC chips have been considered for use on the ITB: one designed at CERN for LHC experiments [3] and the one designed at Paris VI-VII for the DIRC elctronics* [4]. Both of them responded to the above requirements: the design on the present document is based on the CERN chip for the reasons that are explained below. The main characteristics of this chip are (see [3] for complete specfications):

- number of channels: 32;
- hit input threshold voltage: standard TTL
- clock frequency: 20 to 60 MHz;
- time bin size: $T_{\text{clock}}/32$ (= 0.52 ns at 60 MHz);
- dynamic range: 21 bit (≈ 1 ms at 60MHz);
- double pulse resolution: 15 ns;
- maximum hit rate on single channel: $f_{\text{clock}}/80$ (= 750 MHz at 60 Mhz clock);
- event buffer size: 256 words;
- read-out buffer size: 32 words;
- enable/disable of single channels during normal operations;
- complete configurability via JTAG protocol.

The determination of hits time is done by means of a coarse timer running at clock frequency (59.5 MHz in our case) and a chain of delay gates for the fine timing, giving a bin size of 1/32 the clock period. A self calibration scheme based on the use of a Delay Locked Loop (*DLL*) balances variations in the gates delays due to temperature and voltage. Being conceived as a general purpose device, this IC features a series of different operational modes and have many programmable registers (e.g. overall and single channels offset).

The choice of the CERN chip has been made on the following basis:

* The TDC chip designed in Rome for the drift chamber of the KLOE experiment was also considered initially but it turned out not to suit *BABAR* requests: besides having a bin size larger than 1.0 ns, it can operate only in 'common START' or 'common STOP' modes and does not support selective readout of data through a time window.

- higher number of channels ⇒ lower number of chips (3 instead of 6);
- larger dynamic range (21 bits instead of 16);
- recovery of stored hits with a 'trigger matching' procedure ⇒ need for just one level of external FIFO (event buffer)[*];
- configuration through JTAG protocol ⇒ 4 dedicated serial lines, no need for bi-directional buses;
- possibility of daisy chain connection ('token ring') for the 3 chips both on read-out and configuration;
- programmable offset both on global counter and trigger time and on individual input channels;
- chip already extensively tested in laboratory in Genoa[†] [5] by means of an evaluation board (CAEN V667);
- final version of the chip already in production.

In summary, it appears that this choice results in a simpler board design having the same or better performances. The slightly higher cost per TDC channel is balanced by the smaller number of other electronic components needed.

4. Board design

The board block diagram is shown in fig. 1. The input signals are 96 ECL fast-OR coming each from one FEC: these have to be converted TTL before entering the TDC input. Input commands and data coming serially from the backplane through the 60 MHz *DIN* line are decoded and/or written into registers by one sequencer (*SEQ1*). A 16 bits, 128 word deep FIFO stores temporarily the configuration data (128 bits for each chip) to be written into the TDCs. A second sequencer (*SEQ2*) acts as a JTAG interface between the command decoder and the TDC chips by driving the 4 lines of the bus at 15 MHz frequency (obtained by dividing the 60 MHz clock signal). At the occurence of a *L1 Trigger Accept*, data corresponding to the appropriate time window are transferred to the TDC read-out buffer and hence to the board event buffer through a token ring protocol. The event buffer is a 32 bit, 512 words deep FIFO working at 60 MHz frequency; a header is written before each event set of data and a trailer appended (see below for the format). Eventually, at the occurrence of a *Read Event* command, data are transferred in parallel from the buffer to a third sequencer (*SEQ3*) and here serialized and sent out on the 60 MHz *DOUT* line.

[*] In the case of the DIRC chip the selection of hits in the right time window is made by keeping them in an internal FIFO for a time corresponding to the *L1* jitter (1.0 μs), after the proper latency time has passed (11 μs). This requires the presence of a first level of FIFO for each TDC chip besides the (global) event buffer. In contrast, with the 'trigger matching' procedure all the hits can be read sequentially and directly written into the event buffer without losing any of them.

[†] With clock frequency up to 80 MHz.

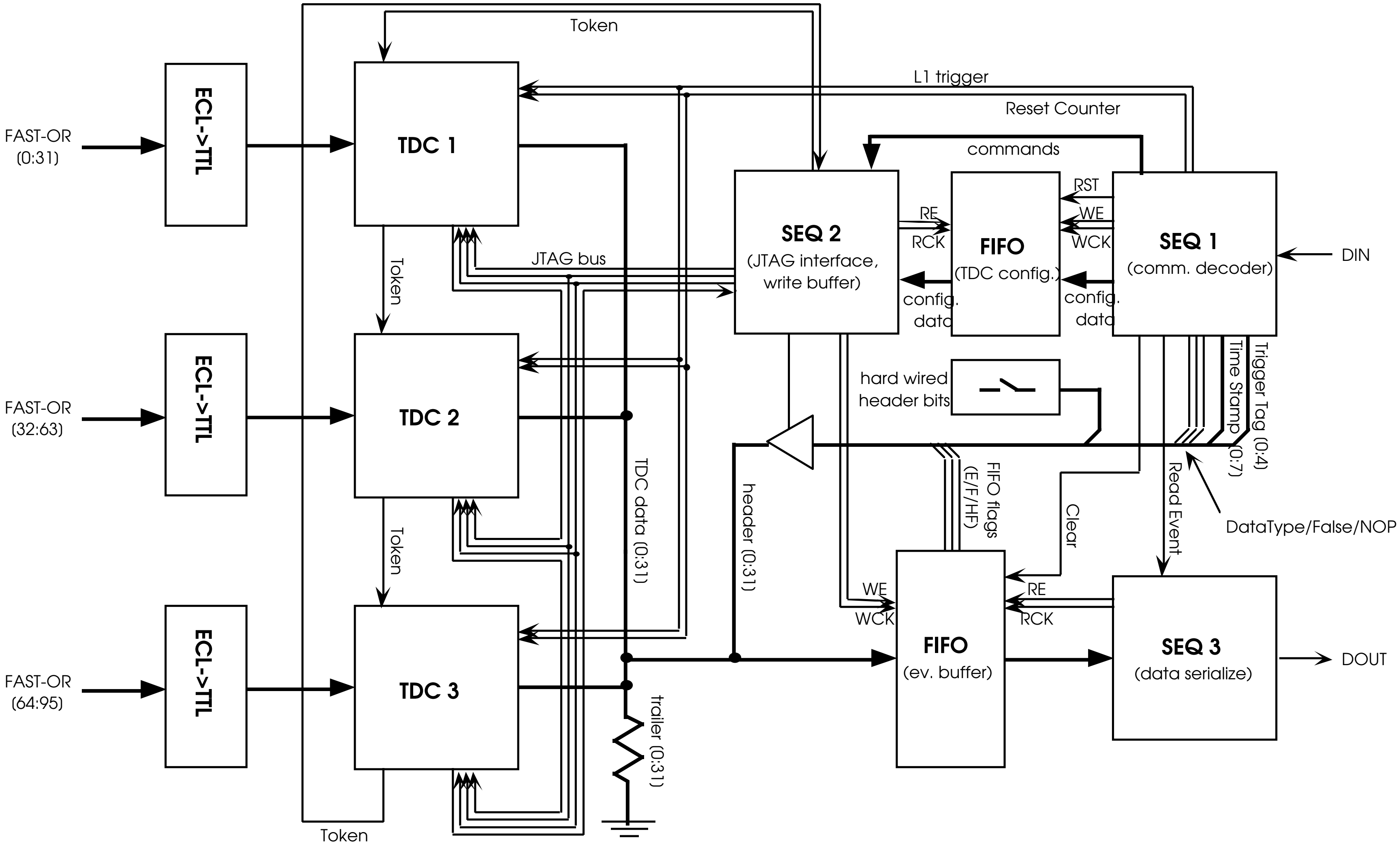

Figure 1 *ITB* Block Diagram

5. Board commands

The ITB must respond to *BaBar* run-time commands as specified by the *BaBar* protocol [2][*]. In addition other non-run-time, subsystem-specific commands can be implemented. Below are listed all commands in both classes, followed by the description of how the board will respond to them.

Run-time (global) commands:

- *No Op*: no action;
- *Clear Readout*: the event buffer is emptied (i.e. the FIFO pointer reset);
- *Sync*: a RESET command is sent to all TDCs, so that all counters are reset, together with all internal FIFOs[†] (but the DLL stays locked);
- *L1 Trigger Accept*: a TRIGGER signal is sent to all TDCs simultaneously and the related time stored in their trigger buffers; the trigger matching procedure is applied and selected data are read out with a "token ring"[‡] protocol and written into the event buffer, enclosed between a proper header and trailer (see following section for data format);
- *Read Event*: data stored in the event buffer are read in parallel by *SEQ3* and output serially on the *DOUT* line until a trailer is found;
- *Calibration Strobe 1*: no action;
- *Calibration Strobe 2*: a pulse is sent simultaneously to all TDCs' input pins.

Non-run-time (subsystem-specific) commands:

- *Configure*: all TDCs are configured: 3×128 bits are read serially by *SEQ1* from the *DIN* line and stored as 8 bit words in the configuration FIFO; these are subsequently read by *SEQ2* and written via the JTAG protocol into all TDCs' setup registers[§] (a single *Configure* command is required to configure all TDCs' setup except for single channels offset values; two are required to reset the DLL; 32 are required to set all single channels offset values);
- *Write Mask*: single channel enable/disable masks are written: 3×32 bits are read serially by *SEQ1* from the *DIN* line and stored as 8 bit words in the configuration FIFO; these are subsequently read by *SEQ2* and written via the JTAG protocol into all TDCs' control registers;

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[*] With respect to [2] a new calibration command (here called *Calibration Strobe 2* to distinguish it from the "old" one, *Calibration Strobe 1*) has been added to the list of run-time commands: this is going to be used by the *ITB*.

[†] The time needed to read out data from all three TDCs, in the limiting case of maximum occupancy of their read-out FIFOs (i.e. 3×32 hits) is about 1.8 μs: this is less than the minimum time allowed between a *Read Event* and a follwing *Sync* command (2.2 μs), so that at the occurrence of a *Sync*, all data to be read are already stored in the event buffer.

[‡] The bits of each time datum are read out in parallel from the chip output pins, while the three chips are "polled" in a serial fashion by shifting a proper "token" signal.

[§] The JTAG protocol allows data to be passed "transparently" through components if desired, so that a single write command and line can be used to fill serially all three registers.

- *Read Error*: the error status of all three TDCs is checked: 3×5 bits are read serially from TDCs' status registers by *SEQ2* via the JTAG protocol; these are subsequently sent out on the *DOUT* line by *SEQ3*.

6. Data format

Events data will be written into the event buffer in 32 bit words format. Each event will consist of one header word, *n* data words, corresponding to all the hits within the right time window, and one trailer word. Single bits in these words will have the meaning explained below:

Header (identical to *IFB* header):

- 0: always 1;
- 1-2: module type (0 = *IFB*, 1 = *ICB*, 2 = *ITB*);
- 3: data type (0 = run, 1 = test);
- 4-6: event buffer FIFO flags (Full, Empty, Half Full);
- 7: always 0;
- 8-12: trigger tag;
- 13: always 0;
- 14: False Command received;
- 15: No Op received;
- 16-23: time stamp;
- 24-26: *ITB* ID #;
- 27-28: always 0;
- 29-31: crate ID #.

Data:

- 0: always 1;
- 1-5: channel #;
- 6-7: TDC chip #;
- 8: always 0;
- 9: error flag;
- 10: always 0;
- 11-15: fine time count;
- 16-31: coarse time count.

Trailer:

- 0-31: always 0.

7. References

[1] L. Morelli, M.G. Pia, *Determination of the bunch crossing with the IFR*, *BABAR* note

[2] *BABAR* DAQ Group, *BABAR note* 281

[3] J. Christiansen, *32 Channel general purpose Time to Digital Converter*, CERN/ECP-MIC

[4] P. Bailly, J. Chaveau, J.F. Genat, H. Lebbolo, Z. Bo, *DIRC Digital TDC Chip Reference*

[5] A. Caccia, *graduation thesis*, University of Genova