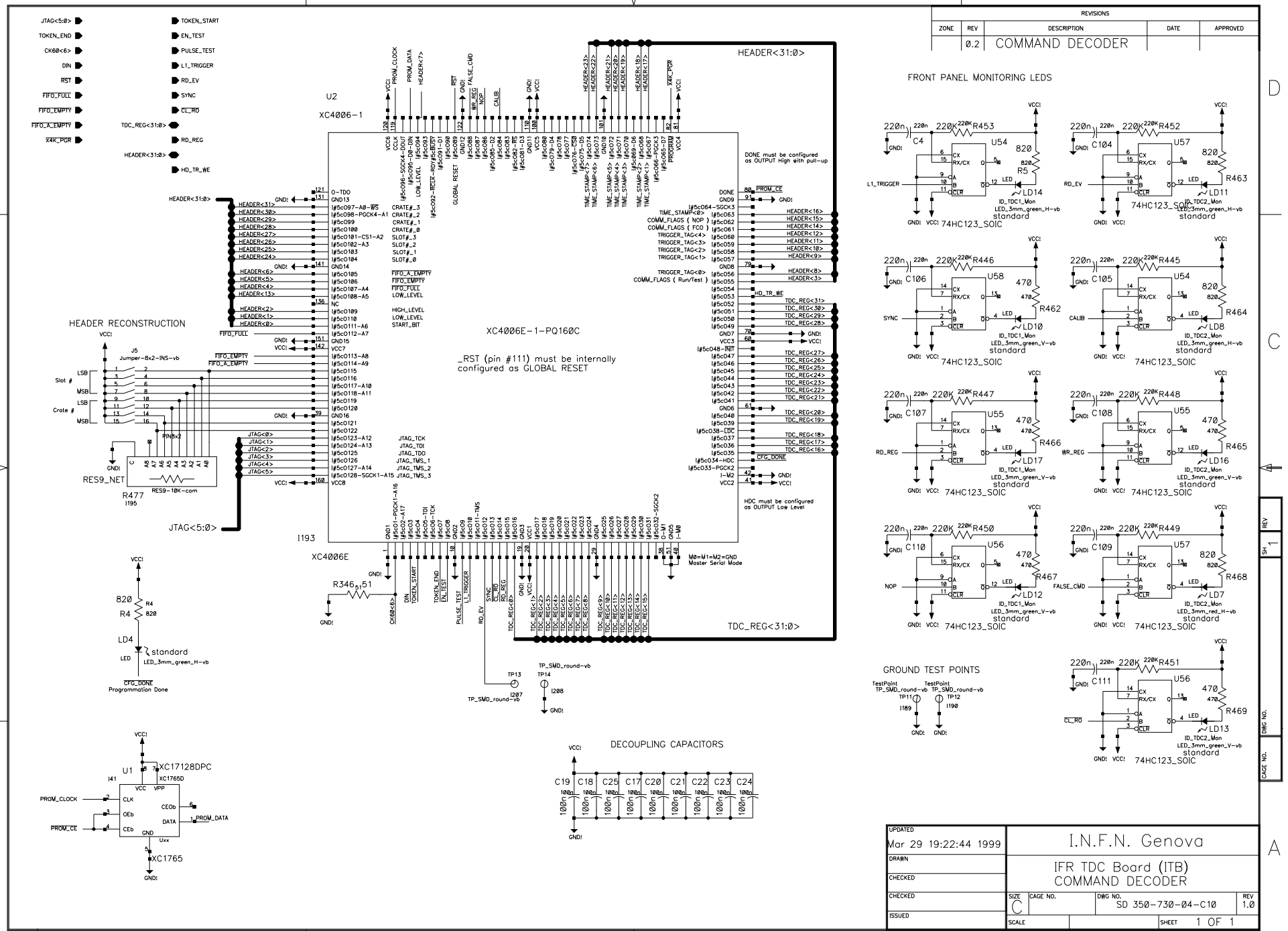
JTAG<5:0>
TOKEN_END
CK60<6>
DIN
RST
FIFO_FULL
FIFO_EMPTY
FIFO_A_EMPTY
X4K_PGR
TDC_REG<31:0>
HEADER<31:0>
TOKEN_START
EN_TEST
PULSE_TEST
L1_TRIGGER
RD_EV
SYNC
CL_RO
RD_REG
HD_TR_WE
U2
XC4006-1
XC4006E-1-PQ160C
XC4006E
HEADER<31:0>
_RST (pin #111) must be internally configured as GLOBAL RESET
DONE must be configured as OUTPUT High with pull-up
HDC must be configured as OUTPUT Low Level
M0=M1=M2=GND Master Serial Mode
HEADER RECONSTRUCTION
RES9_NET
R477
I195
JTAG<5:0>
I193
R346
51
CFG_DONE
Programmation Done
U1
XC17128DPC
XC1765D
XC1765
I41
PROM_CLOCK
PROM_DATA
PROM_CE
DECOUPLING CAPACITORS
C19 C18 C25 C17 C20 C21 C22 C23 C24
100n
FRONT PANEL MONITORING LEDS
74HC123_SOIC
standard
GROUND TEST POINTS
TP_SMD_round-vb
TP11
TP12
TP13
TP14
I189
I190
I207
I208
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
0.2
COMMAND DECODER
UPDATED
Mar 29 19:22:44 1999
DRAWN
CHECKED
CHECKED
ISSUED
I.N.F.N. Genova
IFR TDC Board (ITB)
COMMAND DECODER
SIZE
C
CAGE NO.
DWG NO.
SD 350-730-04-C10
REV
1.0
SCALE
SHEET
1 OF 1
REV
SH 1
DWG NO.
CAGE NO.