RPC97

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Data Acquisition System for RPC detector at BaBar

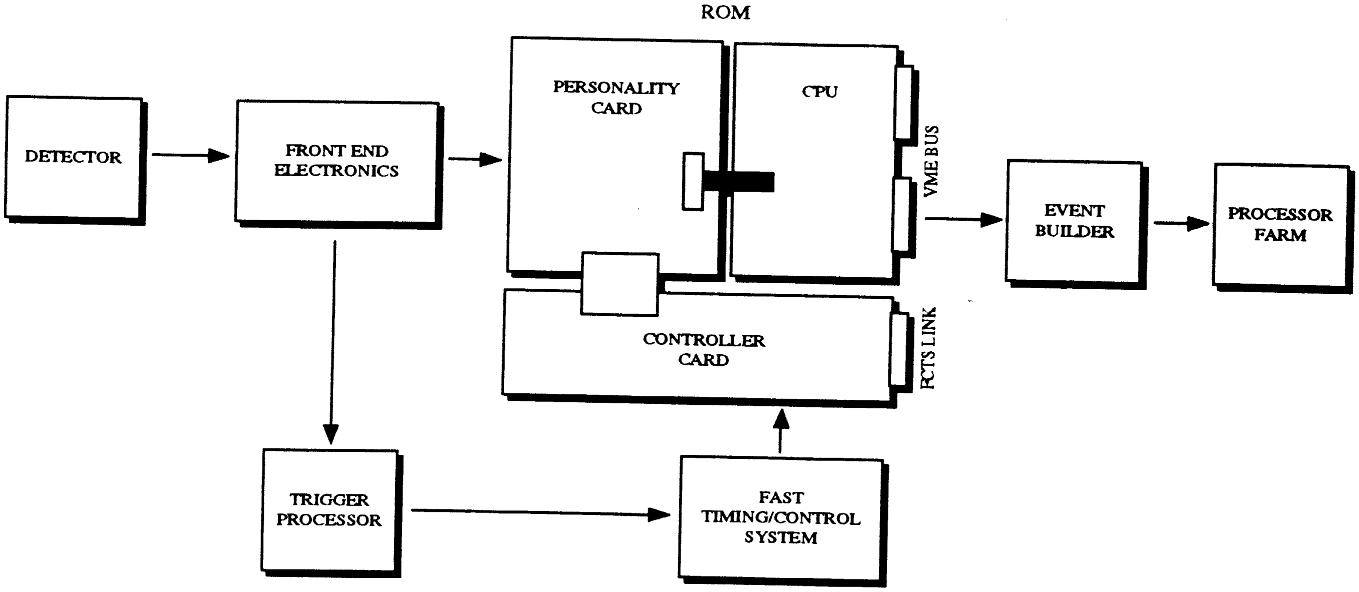
Summary:

- **The Babar data acquisition system**
- **The IFR data acquisition system:**
  - **FEC**
  - **IFB**
  - **ICB**
  - **ITB**
  - **PDB**
  - **ICC**
- **Results of test on prototypes**
- **Conclusions**

The BaBar DAQ system

Requirements

- PEP-II beam crossings occur at a rate of $238 MHz$, which from the point of electronics is essentially continous.
- Design Luminosity of $3 \times 10^{33} cm^{-2} s^{-1}$ to be upgraded to $10^{34} cm^{-2} s^{-1}$.
- Rate of all physics processes to be recorded is expected to be $100 Hz$.
- No losses due to deadtime, machine background and electronic noise.



Main Features

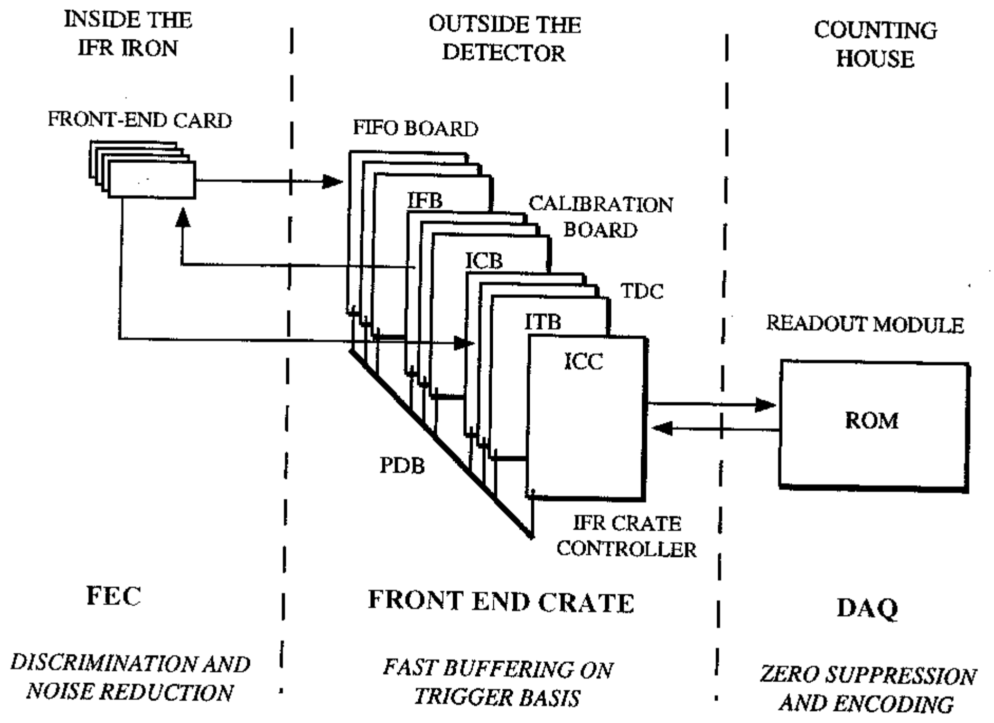
- Large buffering very close to Front-End to avoid deadtime losses due to trigger latency.
- Distributed CPU to handle large volume of data.
- Common architecture of online processors to minimize the overall software and hardware maintenance and improve reliability: ROM.

The IFR DAQ system

Requirements

- Digital information from strips.
- Large volume of data (~ 51000 strips).
- Trigger latency of 12 μs.
- Large buffer.
- Low cost and high reliability since FEC will be accesible only exceptionally.

IFR Electronics Architecture



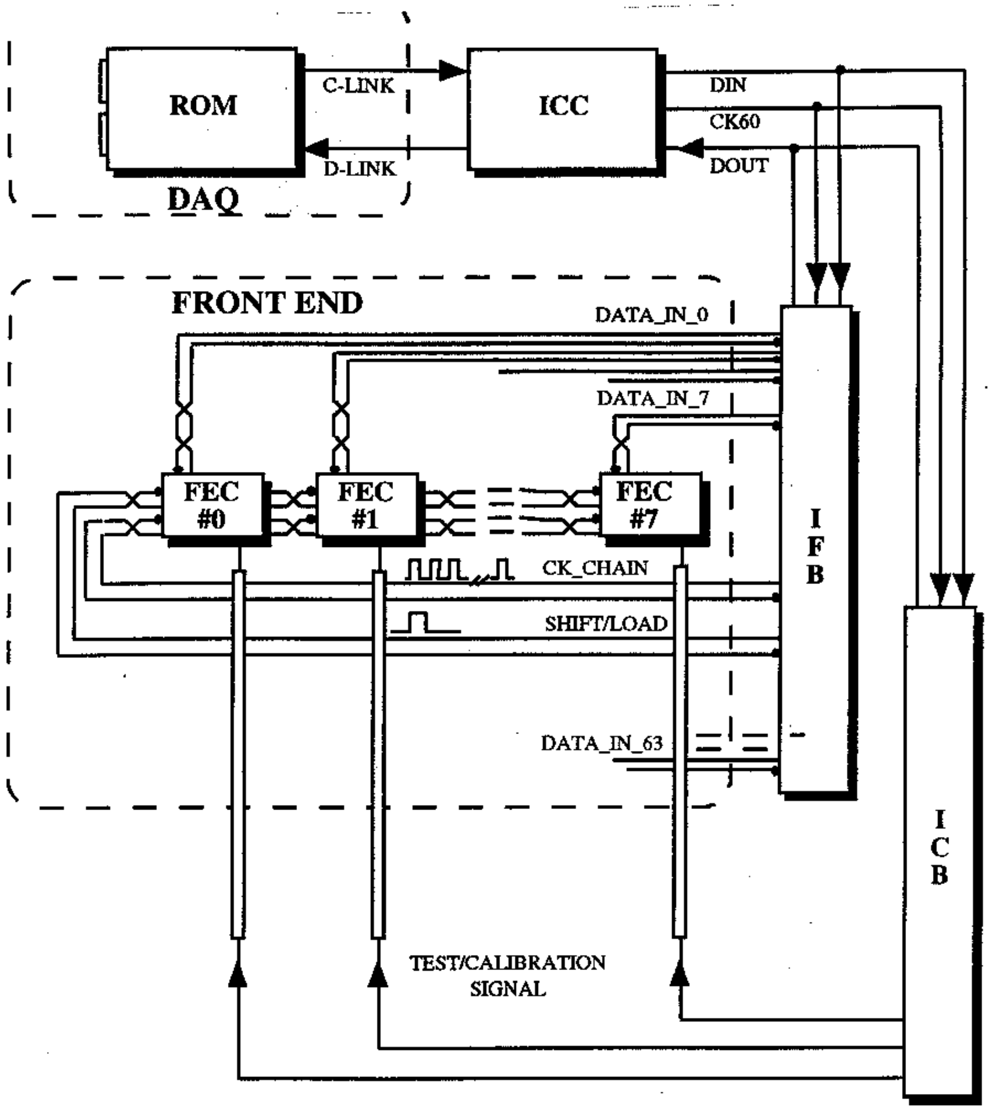


Fig. 1 - FIFO Board (IFB) inside the IFR Electronics System.

The Chosen Architecture

- Front-End Cards to discriminate induced signals of 16 fired strips and to produce a Fast-Or signal to be used for time measurament ($\sim$ 3200).
- FIFO Board to store data waiting to be read by DAQ system (56).
- Calibration Board to perform continuos test of FEC (20).
- TDC board to measure the arrival time of events using the Fast-Or signal of FEC (36).
- All these boards will be hosted in 8 custom crates with a point-to-point backplane to distribute fast commands and collect data at the system frequency of $60MHz$.
- The connection between the custom crate and the main DAQ board (ROM) will be assured by the Crate Controller using a optical fiber link (G-link).

The BaBar Online Protocol

The Run-Time (Global) Commands

- L1 Trigger Accept: it is the 12 μs latency level-1 trigger, IFB sends the signal to FECs immediately and receives the data to be stored in the FIFO togheter with Time Stamp. Many L1 Accept can be issued by ROM if enough memory is avaible in the IFB.
- RDE (Read Event): this comand provokes the trasmission of data from IFB to ROM via G-Link. The command is issued by the ROM only if there is memory available on the ROM.
- CALIB: The Calibration strobe is used to send test signals to FEC during calibration run.
- CLEAR: reset FIFO pointers and their content is lost. No effect on time registers.
- SYNC: Reset of the time registers incremented by system clock and used to produced Time Stamp. FIFO content is unaffected.
- NOP: the command is decoded although no operation is required, a bit will be written on next event header.

The Front-End Card (FEC)

The Main Features of FECs are:

- Large amplification input stage.
- Fixed threshold.
- Test input used in connection with ICB.
- Trigger latency and noise rejection logic(MACH 210AQ-15JC).
- Fast-Or (PALCE16V8Q-10JC).

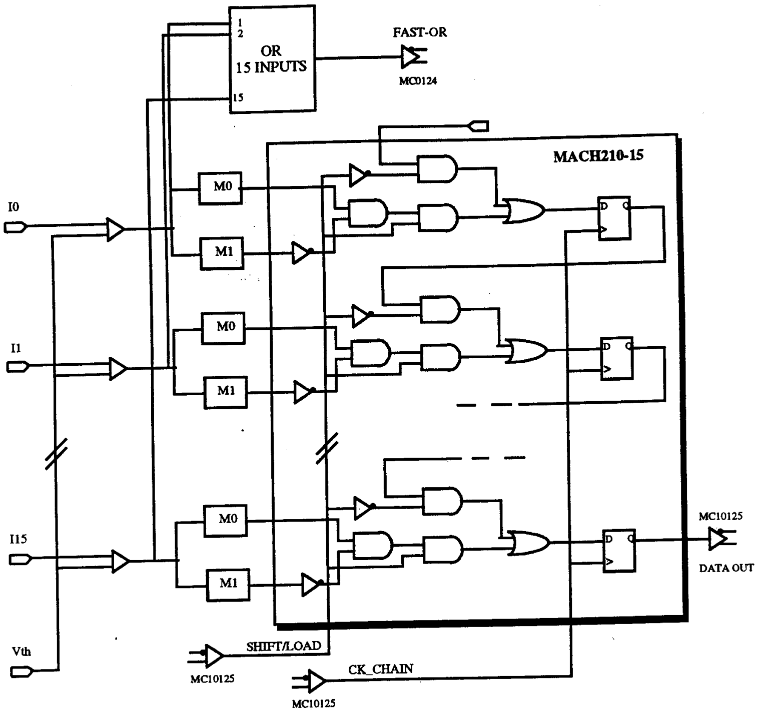
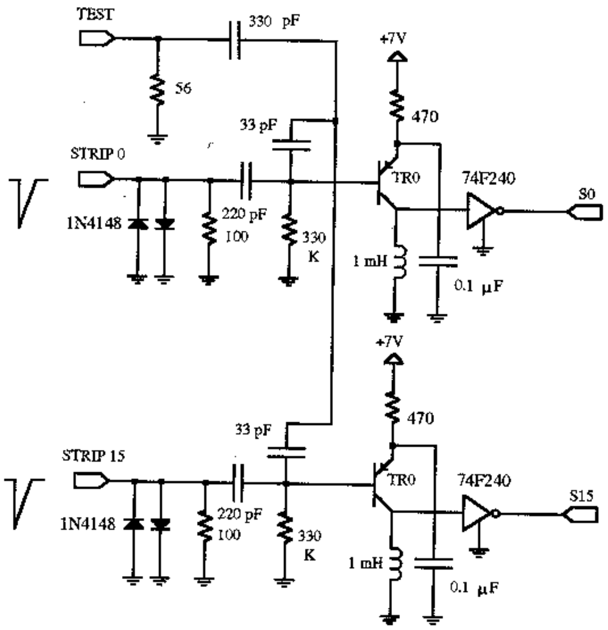
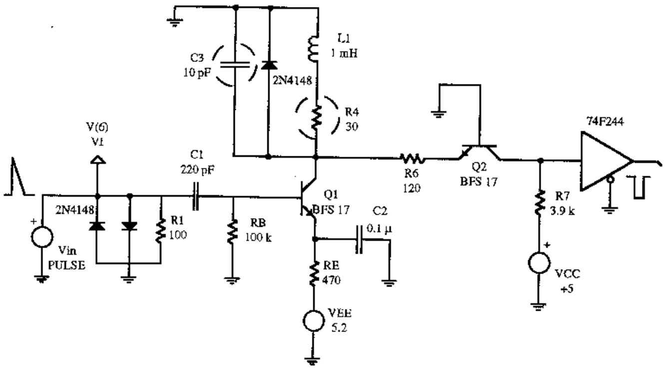


Figure 3 - FEC functional block diagram.

The FEC Schematics





The IFR FIFO Board (IFB)

Functional Overview

- Parallel readout of 64 FECs sending 16 clock signal at $15 Mhz$ to be ready in less then 1.5 μs.
- Large Buffer ($1KB$) to keep events untill DAQ can read them.
- No sparsification of data to achieve good reliability and semplification of the design.
- Complete decoding of Babar Run-Time commands and sub-system commands:

  WRD (Write IFB FIFO): to load 64 bits test pattern.

  RDF (Read IFB FIFO): to read the test pattern.

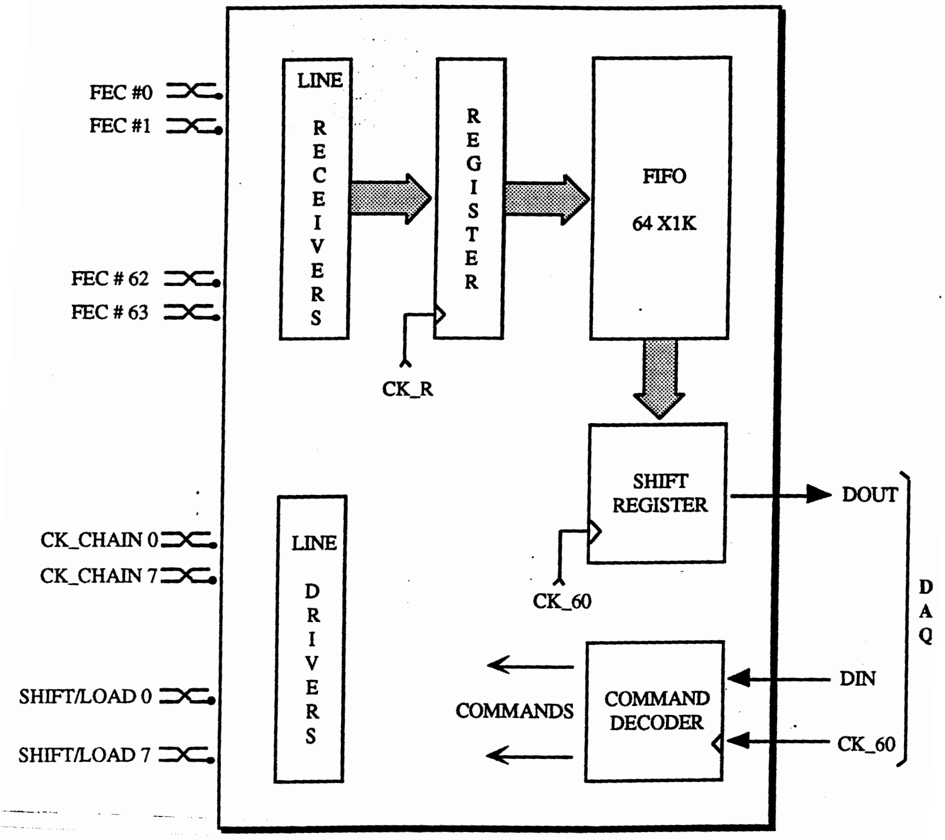


Fig. 2 - The principal components of the IFR FIFO Board (IFB).

The IFR Calibration Board (ICB)

Functional Overview

- It sends test signals to a selected number of FEC (up to a maximum of 196) when a CALIB command is received. During a calibration run, after this command a L1 Accept and a RDE command are issued to read-back the calibration data.
- Test signal can be shaped both in width and in amplitude.
- Sub-System Commands:

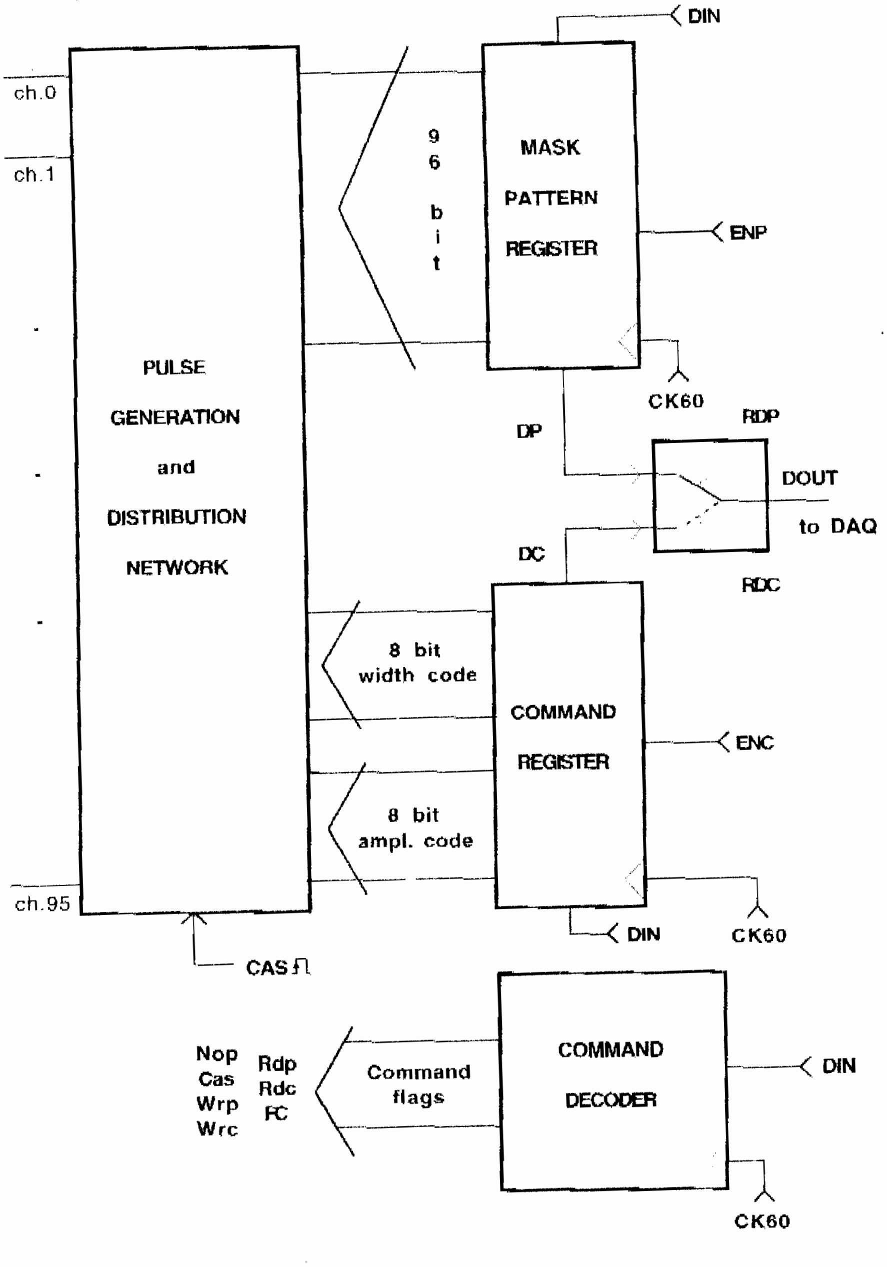
  WRP:Write bit pattern to select FEC.

  RDP:Read bit patter.

  WRC:Write command register, 8 bit for width, 8 bit for amplitude.

  RDC:Read command register.

ICB Block Diagram



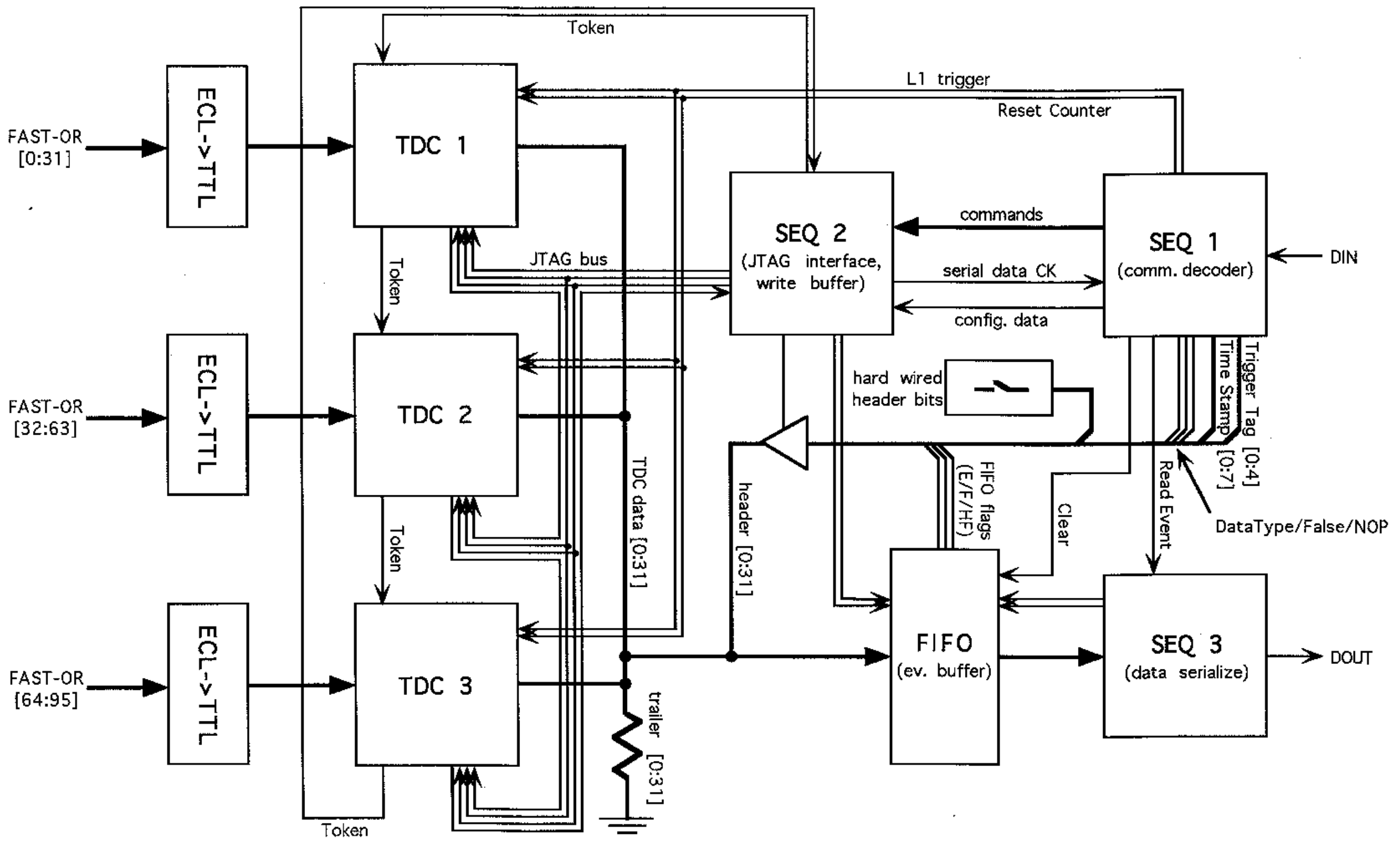
The IFR TDC Board (ITB)

Functional Overview

- The board is based on a new 32-channel TDC designed at CERN for LHC detectors. At 60Mhz frequency the chip can measure a minimal time bin size of $0.5ns$, in this TDC a self calibrating scheme is implemented by using voltage controlled delay elements as part of a Delay Locked Loop (DLL). The chip can be programmed to run in many different ways and can be easily adapted to measure the bunch crossing time in BaBar.
- The input signals are the Fast-Or of 96 Front-End Cards.
- A large event buffer is available in the chip to handle the trigger latency.
- On arrival of L1 Accept command data are selected according to the trigger time and stored on external FIFO until RDE command arrives.
- Sub-System Commands:

  CALIB-2 Strobe to sent a test pulse to all TDCs' input pins.

  CONFIG is used to set the configuratin mode for data taking or calibration mode.


Token
L1 trigger
Reset Counter
FAST-OR [0:31]
ECL->TTL
TDC 1
SEQ 2 (JTAG interface, write buffer)
commands
SEQ 1 (comm. decoder)
DIN
serial data CK
config. data
JTAG bus
Token
hard wired header bits
FAST-OR [32:63]
ECL->TTL
TDC 2
Trigger Tag [0:4]
Time Stamp [0:7]
TDC data [0:31]
header [0:31]
FIFO flags (E/F/HF)
Clear
Read Event
DataType/False/NOP
Token
FAST-OR [64:95]
ECL->TTL
TDC 3
FIFO (ev. buffer)
SEQ 3 (data serialize)
DOUT
trailer [0:31]
Token

The Point-to-point Distribution Board (PDB)

The backplane fo FEE crates

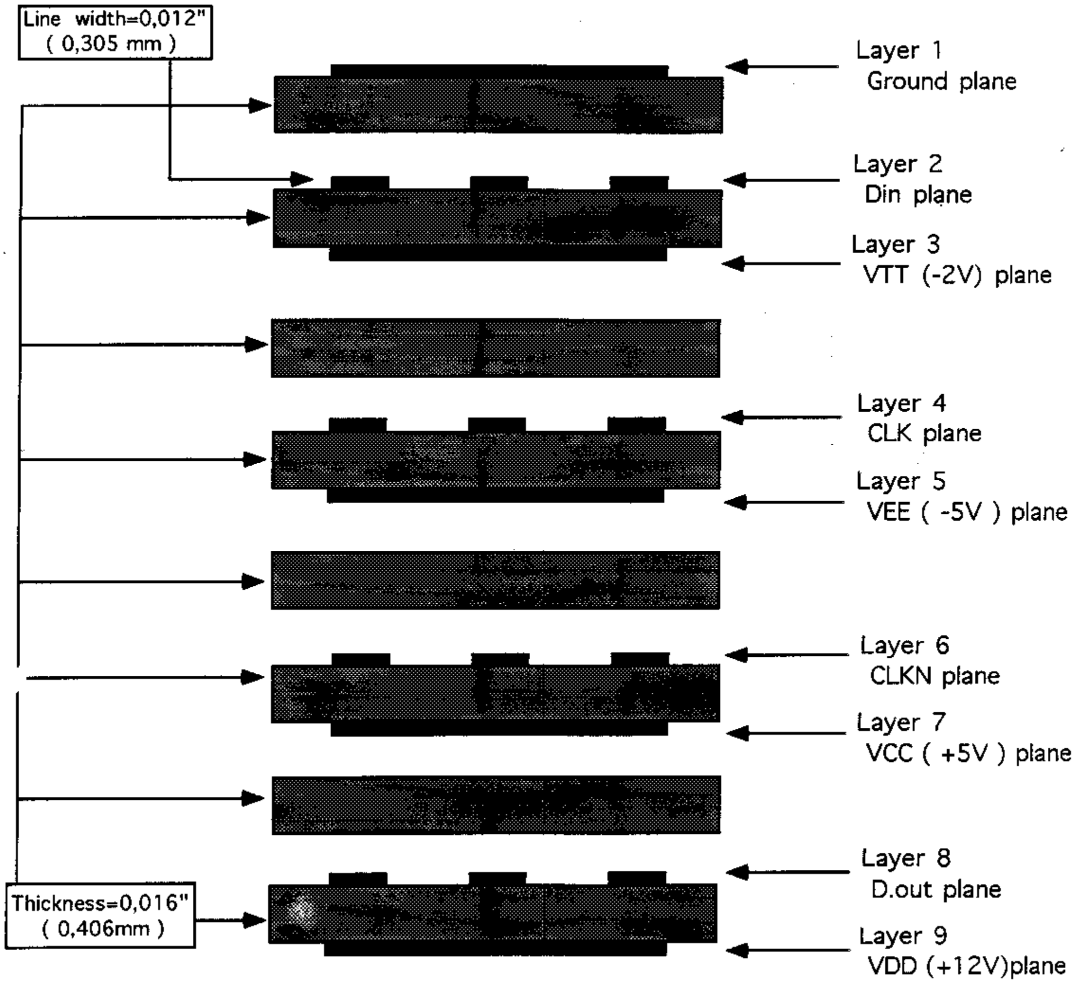
- In BaBar all the DAQ system is synchronized on a 59.5MHz frequency, the global commands must be delivered and the data collected using this frequency. All the IFR boards (IFB, ICB, ITB) are located in a special crate and speak with the Crate Controller through the PDB.
- From a mechanical point of view, the PDB is a 21 slots standard VME backplane which connects point-to-point 16 boards to the crate controller using the J2 connector. The 4 free slots can be used only to give power to extra boards.
- Signals are trasmitted with TTL single-ended technology.
- The backplane is a 9 layers vetronite board built with STRIPLINE structure.
- Technical specification:

  controlled impedance 50Ω
  Cu line thickness 35 μm
  fiberglass type FR4
  propagation delay 2.16ns/ft
  dielectric const. 4,5

Structure IFR-PDB

<< STRIPLINE >>

Lines that require controlled impedance are placed on layers 2, 4, 6 and 8. The other planes are used for gnd and low voltage.



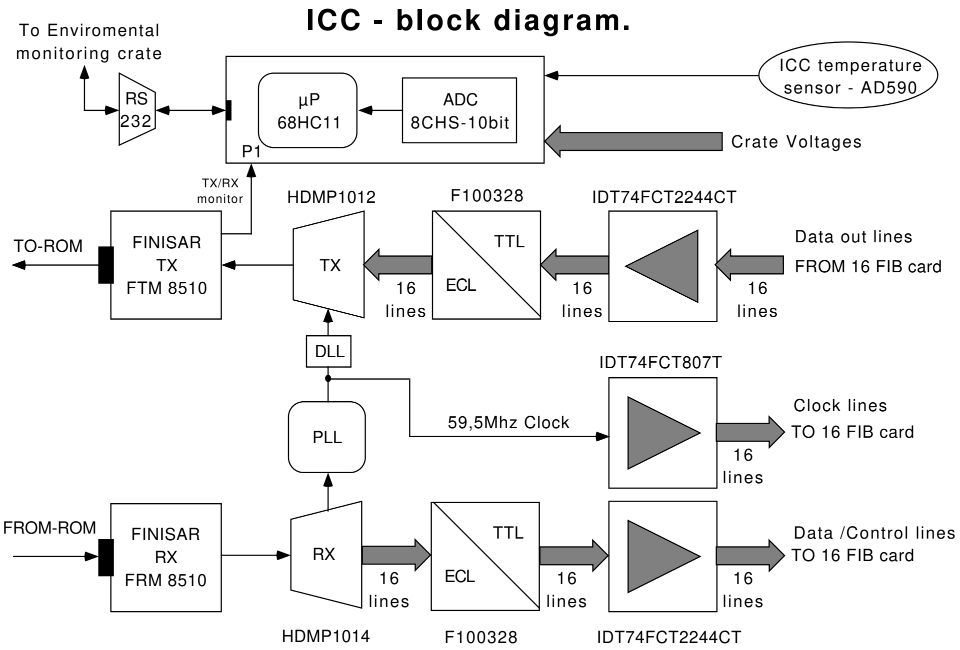
Copper lines thickness = 35 μm
Fiberglass FR4 - Dielectric costant = 4,5
Typical propagation delay = 2,16 ns/ft

■ = copper ▨ = fiberglass

The IFR Crate Controller (ICC)

Functional Overview

- The ICC distributes the sytem clock ($59.5 MHz$) and the global commands to the IFR boards and receives their data.
- It is connected to the Read-Out Module via Optical Fiber (G-Link)
- A microController (MC68HC705X32CFU) is used to monitor the status of the optical transmitter (FINISAR) and to read the temperature inside the crate. Monitor data are transmitted using a CAN-Bus port.



ICC - block diagram.

Results on Prototype Boards

Status of Hardware prototypes

- The FECs have been used in Frascati during the chamber production test and in SLAC in another IFR test station. All boards are built and ready to be installed inside the iron togheter with RPC chambers.
- The PDB, ICC, IFB and ICB prototype boards are built
- Stand-alone bench test gave good results.
- A DAQ prototype test is done using an old version of ROM to send data to the IFR electronic crate with PDB + ICC and IFB.
- The test, using $59.5 Mhz$ clock, has shown a very good performance of all the boards according to specifications.
- The design of TDC board is in progress.

Conclusions

The RPC chambers are installed in BaBar.

New front-end electronics has been designed.

All FECs are built and ready for installation.

IFB,ICB,ICC,PDB prototypes are built.

The test showed very good performace of the boards.