DATA ACQUISITION SYSTEM FOR THE RPC DETECTOR OF BaBar EXPERIMENT

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ABSTRACT

Resistive Plate Chamber (RPC) has been chosen as active detector to equip the Instrumented Flux Return (IFR) of the BaBar experiment. The new design of the Front-End electronics realizes a compromise between the large number of channels (50,000) and the cost of the project. The different components will be described and the results of the first prototypes presented.

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1. Introduction

The BaBar detector has been designed to study the CP violation asymmetries in the decays of B^0 mesons. The experiment will be carried out at the PEP-II accelerator at Stanford Linear Accelerator Center (SLAC).

The physics program is very rich and includes also the determination of the CKM matrix elements, the B^0 rare decays and the Charm and Tau physics [1]. The construction of the experiment and of the beam are in advanced phase and the first collisions are foreseen in Summer 1999.
The muon detector makes use of the Flux Return of the Solenoid equipped with Resistive Plate Chambers (RPC).
The IFR group has built and installed in the detector more than 800 chambers. Before the shipment to SLAC all the chambers was tested in the INFN laboratory in Frascati for gas leaks, and HV. The measurement of HV plateau and of various efficiencies[2] were done during a cosmic rays test.

The Data Acquisition system (DAQ) is one of the key part of any high energy experiment, it must guarantee the collection of the events selected by the trigger system. It must also provide calibration, monitoring and debugging facilities. The architecture chosen by BaBar is fully pipelined in both the trigger and the data flow paths. As a result the system is nearly deadtime free at background levels up to ten times the rate give by machine simulation.

2. The IFR Data Acquisition System

The IFR Data Acquisition system must satisfy the requirements of the general system and, at the same time, try to realize the compromise between the large number of strips ($\sim 50,000$) used to read the RPC, and the cost of the electronic. Since the Front-End electronics is installed very close to the detector, not easily accessible, the read-out design must be also very reliable. To achieve this goal and to fulfill the BaBar requirement on the DAQ speed, a mixed parallel-serial readout has been chosen.

A high speed clock ($59.5 MHz$) will be used to synchronize the flow of data and to control, reset and throttling of data.

The IFR DAQ system, shown in Fig[1], can be divided in three parts:

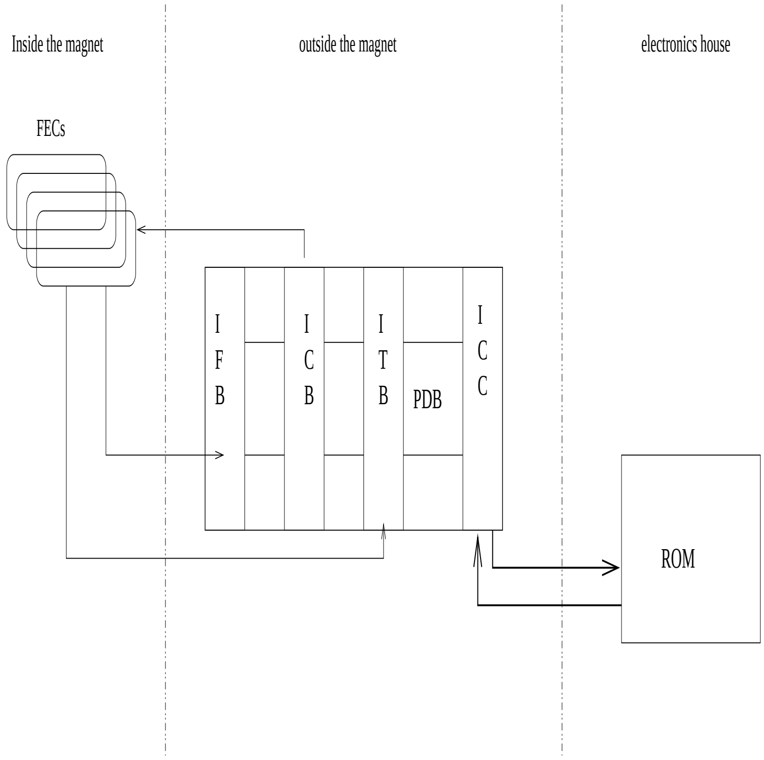

Fig. 1. IFR Data Acquisition System

- The Front End Cards (FEC) discriminate the strip signals and store the data during the trigger latency. Most of them are installed, together with the RPC, inside the iron slabs. A small part of them, when not enough space is avaliable, are hosted in special minicrate located outside the iron.
- The intermediate step is the readout crate, eight of them are distributed around the detector. In this crate there are three kinds of IFR boards, the FIFO board (IFB) where the digital strips data are kept until the DAQ is ready to read them. The TDC board

(ITB) is connected to the Fast-OR output of the 16 channels of the FEC. This signal is sent to multihit TDC and used to measure the time of RPC hits. The third board, Calibration board (ICB), is used to send test signal to the FEC input stage to check the threshold and their status.

A dedicated Crate Controller (ICC) is used to connect the crate to the Electronic House via the optical link. Inside the crate a custom point-to-point backplane (PDB) is installed, all these electronic boards have been designed to operate at the BaBar sytem frequency of $59.5MHz$.

- The last part of the IFR DAQ system is the Readout Module (ROM). This is the standard BaBar DAQ board used by all the detectors and located in the electronic house. It is connected to the crate through an high speed data link (G_link) used to transmit data on optical fiber.

In this report the different components of the IFR DAQ system will be described and the results of the first prototype will be presented. In table[1] the total number of IFR DAQ board is shown:

Table 1. IFR DAQ boards

DAQ Crate	8
ICC	8
IFB	56
ICB	20
ITB	36

3. The Front End Card (FEC)

The RPC is a low noise detector with a good signal to noise ratio, producing fast (rise time 2-4 ns) and hefty signals (of the order of 300mV). These characteristics allow the use of cheap electronics with a fixed threshold. FEC input stage (see block diagram in Fig[2]) is connected directly to the strips and operates continuously, each strip acts as a transmission line with a discriminator at the end.

The FEC takes into account also the trigger latency of $11.5 \pm .5\mu s$, the digital signal is fed into a dual bank of monostables which enables

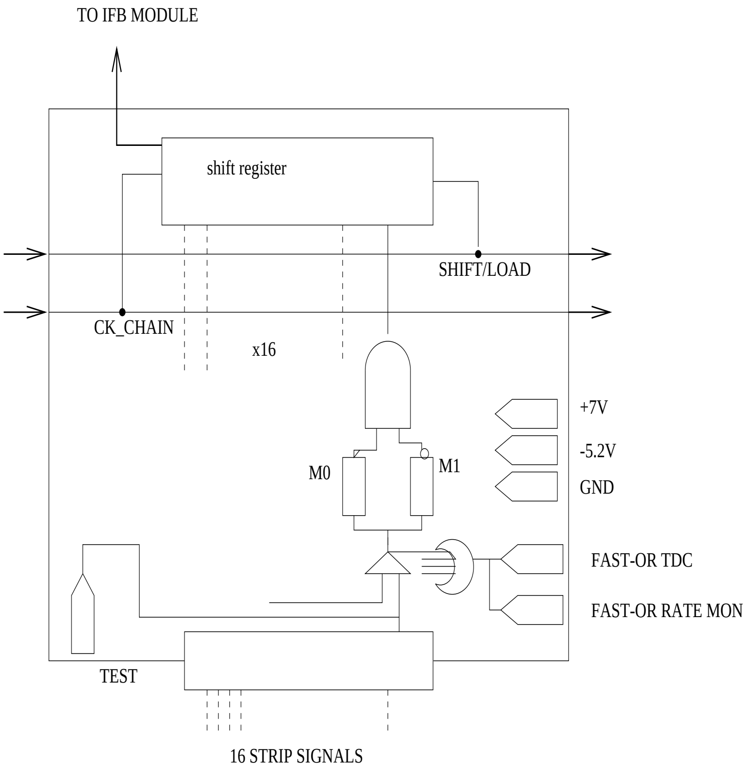

Fig. 2. ICC block diagram

the data collection only during the trigger time window of $1\mu s$. This method produces also a strong reduction of the detector noise.
On the occurrence of the trigger, a Shift/Load signal and a sequence of 16 clock pulses are sent by the IFB to the FEC. The Shift/Load signal loads the pattern into a shift register and the clock pulse shifts the 16 strips data out of the board. The FIFO board reads 64 FEC's in parallel. To test the functionality of the front end it is possible to inject a pulse into the input stage of the transistor simulating an hit on all the 16 channels.

4. The Point-to-Point Distribution Board (PDB)

The design of this backplane requested a special care to guarantee the delivery of signals and clock at $59.5Hz$ within the requirements of

the BaBar DAQ system. The "stripline" technology (Fig[3]), with 9 layers, was chosen after a successful test on a prototype board, all lines have controlled impedance (50Ω).
The Point-to-point Distribution board is a 21 slot backplane for standard 6U Eurocard crate, 17 of them are used by the readout boards, 4 are reserved to power IFR trigger boards. Signals are located on J2 connector, row A and C are for signals, row B is for power and ground. The first position is for the ICC. Each board is connected to the ICC via 3 lines for single-ended signals, data-in, data-out and the clock, all lines have the same length (14.8" $\pm$ .1") to minimize the skew between them. Line terminations on the PDB can be chosen to be resistive or AC coupled.

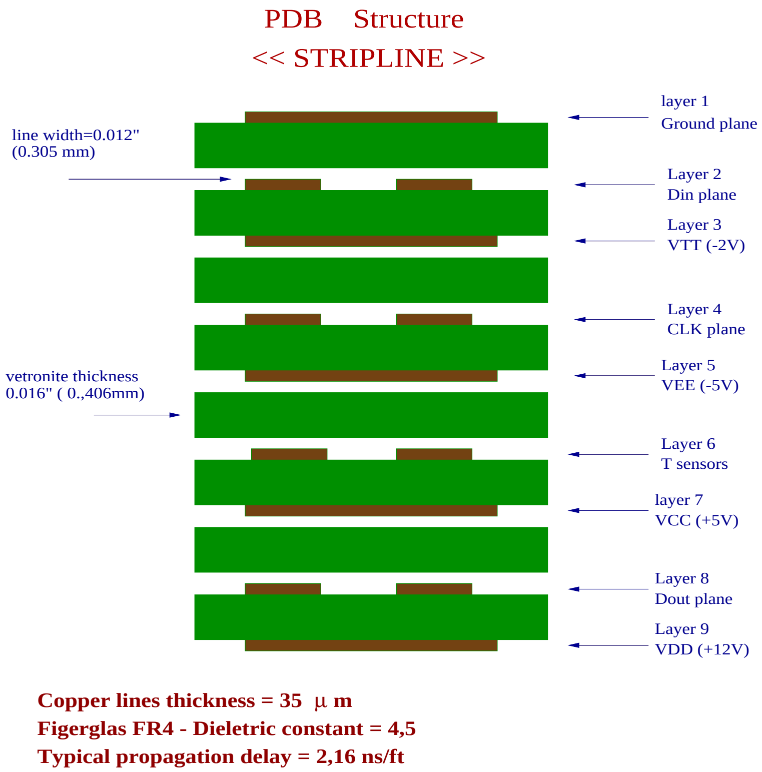

Fig. 3. Point-to-Point Distribution Board

5. The IFR Crate Controller (ICC)

The ICC must guarantee clock and the data delivery to the 16 boards with a jitter less than $\pm 0.5ns$. Unfortunately the use of high performance clock drivers does not guarantee free trouble operation. Only careful board layout and consideration of system noise issue can guarantee reliable clock distribution.
The block diagram of the ICC is shown in Fig[4]. The FINISAR transceiver is the physical interface with the optical link. It is a low cost and high reliability data link up to $1.5Gbits/s$ for application less than a kilometer in length.
The HP chips (HDMP-12, HDMP-14) are used to serialize/deserialize the data, they also perform clock and data recovery, frame synchronization, error recovery and link state monitor.
The clock, received at the exit of the HDMP-1014 receiver, is reshaped in a PLL and then distributed to the 16 boards after been synchronized with the data. The same clock, delayed to wait the data coming from IFR boards, is used to send back data to the ROM.
In the ICC a microntroller (MC68HCX32CFU) monitors the status of the FINISAR modules and reads the temperature inside the crate. The chips provides an external connection with the CAN bus driver, this technology has been chosen by the experiment to communicate the slow control data.

6. The IFR FIFO Board (IFB)

The IFB (Fig[5]) reads data from 64 FEC's, store data until DAQ is ready for the event readout.
After receiving a L1T command (Trigger), the IFB starts a serial data transfer from the FEC's (by means of Shift/Load and Clock signals).
Incoming data are stored in the IFB FIFO's dimensioned to allocate up to 56 complete event fragments (each fragment consists of 1024 bits correspondig to as many strips).
On the arrival of RDE command (Read Event) data are extracted from the FIFO and sent to the ROM. According to the BaBar protocol, two more global commands must be decoded by the boards: the SYNC command used to resynchronize the Time Stamp of the board, and the

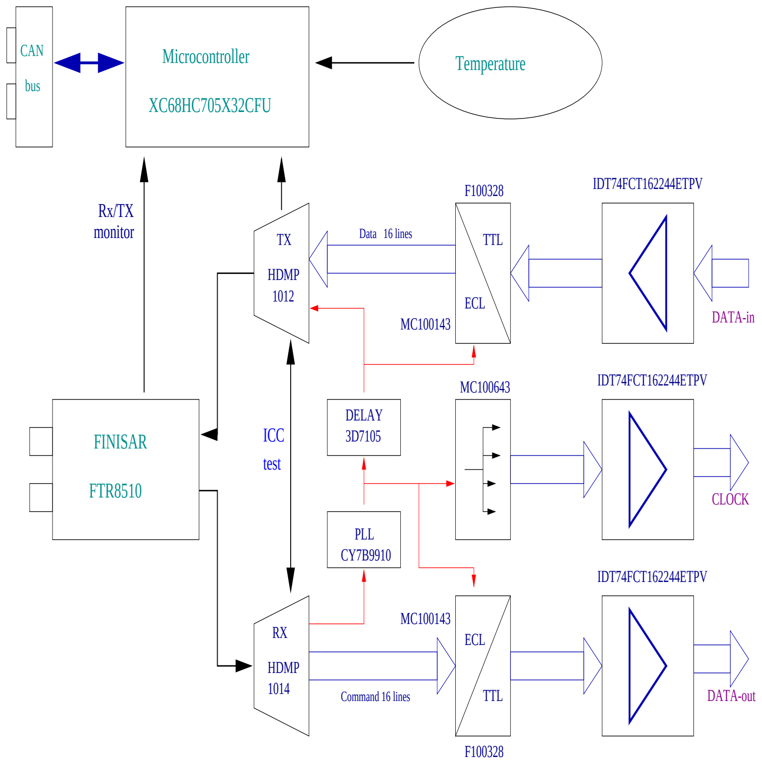

Fig. 4. ICC block diagram

CLEAR command resetting the FIFO pointers.
For debugging purpose two specific commands have been implemented to write 64 bits test pattern (WRF) in the FIFO and to read them back (RDF).

7. The IFR Calibration Board (ICB)

The Calibration board (Fig[6]) will be used to monitor and debug the FEC's. Each board has 96 output channels; the signal generated can be programmed both in shape and amplitude using a specific command (Write Control Register, WCR). Positive or negative polarity can be chosen using the same command.

A further specific command (Write Pattern Register, WPR), containing a 96 bit mask, selects the FEC's to be pulsed.

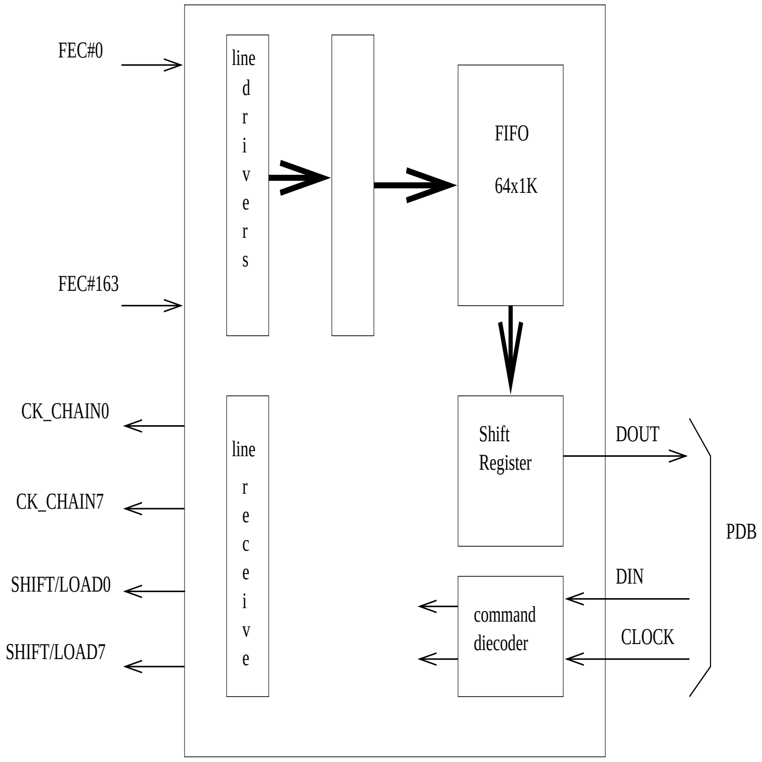

Fig. 5. IFB block diagram

Whenever a Calibration Strobe command (CAS) arrives, the ICB injects a test pulse in the Front-End electronics. The BaBar DAQ system assures a L1T command following at exact $11.5\mu s$ the CAS one. In this way the Trigger latency is preserved and the front-end electronics can be read as during normal data taking.

8. The IFR TDC Board

The TDC board will exploit the excellent time resolution of the RPC's to determine the bunch crossing time of the beam.
The TDC chips, designed at CERN ([3]) as general purpose converter, can operate in many different configurations. These chips have a large memory able to store the ungated input of the FEC's until the trigger arrives. The data selected according the trigger latency and its time

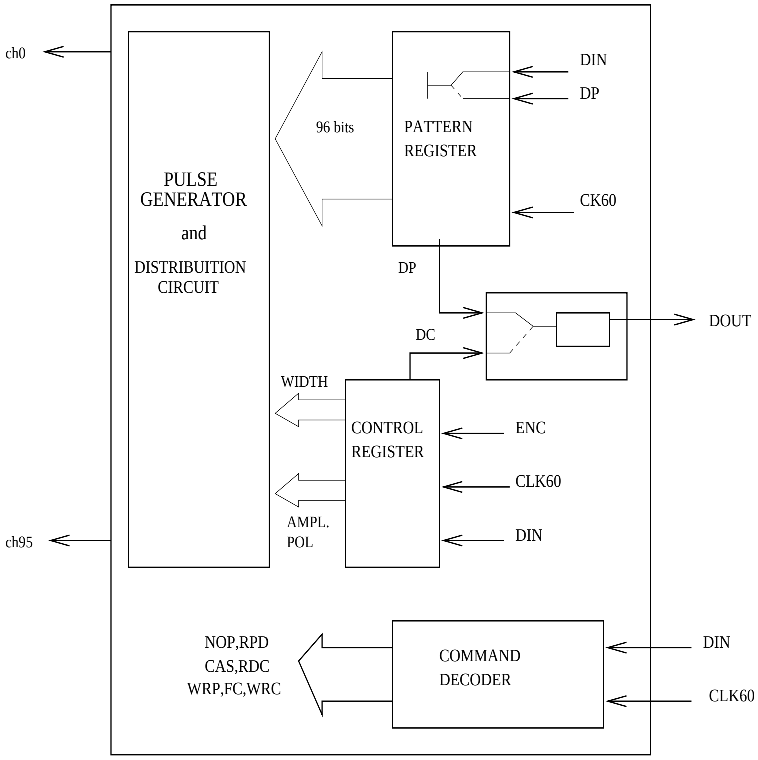

Fig. 6. ICB block diagram

window, are copied in the external large FIFO until the DAQ asks for them. A powerful programmable device (XILINX 4006) will take care of decoding the protocol global and subsystem commands. In order to deliver the system clock to the TDC chips with a jitter lower than $200ps$ and a duty cycle between 45% and 55%, the signal will be re-shaped in the PLL just after being received. The TDC configuration will be loaded (and checked) with specific command by writing (and reading) configuration registers. The block diagram is shown in Fig[7].

9. Results from Prototype Tests

A test bench shown in Fig[8] has been arranged and used to test the prototypes of readout boards. The same setup will be utilized to validate the final production. It consists of 4 minicrates with 16 FECs

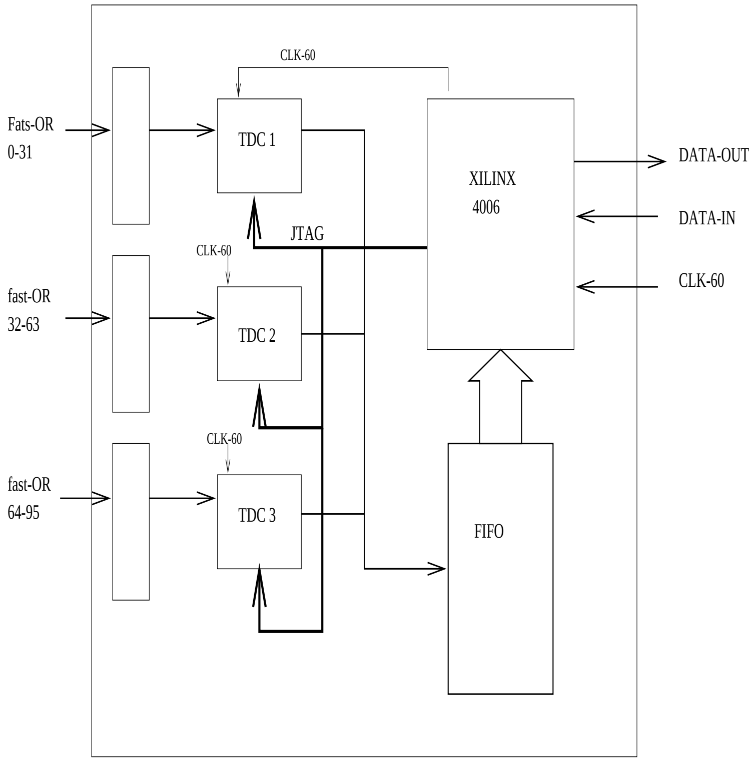

Fig. 7. ITB block diagram

each, one crate with 1 ICC, 4 IFB and 1 ICB. The data are read into the ROM via 40m optical fibre and stored in UNIX station. A second ICC is used close to the ROM, as personality board, to allow the connection with the optical link.
During normal test the calibration signal is sent from the ICB to the FEC's, after a trigger latency of $11.5\mu s$, the FEC's are read and data is sent into the IFB. The RDE command enables the transport of the data from the IFB to the ROM.
With this test it is possible to check the correct performaces of all the boards and their synchronization with the system frequency of $59.5MHz$. Last point verified is the correct operation of the G_link in the IFR DAQ

environment.

10. Conclusions

The prototypes of all the IFR board needed for the data acquisition system are built. Each board has been tested in stand-alone mode to check its compatibility to the BaBar DAQ system.
In a complete test of IFR DAQ system all boards have shown no problems and the procedure to test the final production is found.

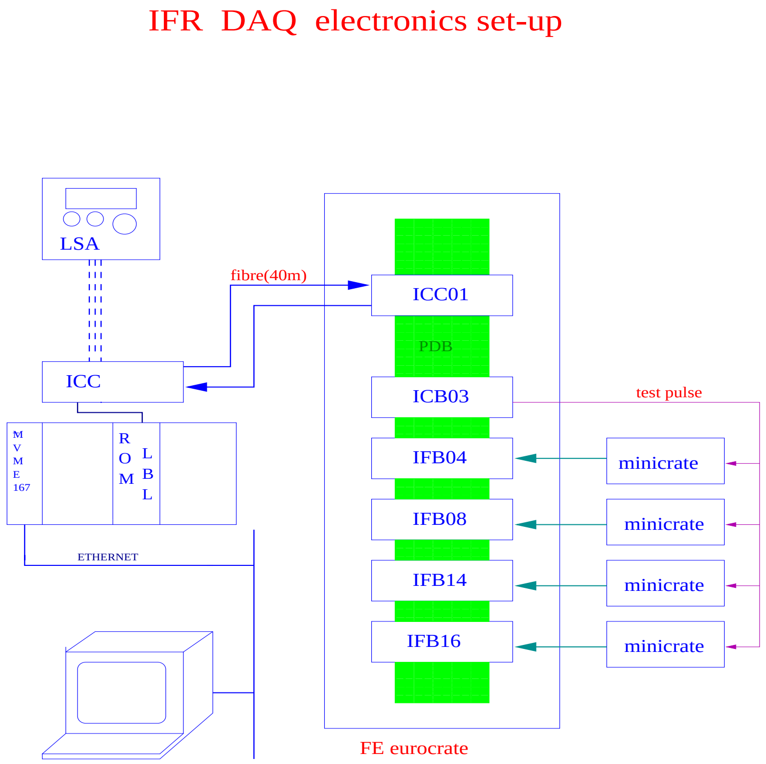

Fig. 8. DAQ IFR test bench.

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12. References

1. Paper contributed by D. Piccolo to these proceedings.
2. Paper contributed by A. Calcaterra to these proceedings.
3. J.Cristiansen, *32 Channel general purpose Time to Digital*, CERN/ECP-MIC,http://pcvlsi5.cern.ch:80/MicDig/jorgen/tdc32_ma.pdf.