BaBar IFR
TDC System Description

Preliminary

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1 Introduction

The good time resolution of the RPC detector can be used to measure the time of all the events with particles crossing the IFR. In previous experiments (L3) a time resolution of 1.5ns has been measured. In the BaBar experiment this information can be used to identify the bunch crossing time which will help to speed up the tracking.

This document is a preliminary presentation of the TDC Boards which is under study at Genoa and has been prepared for the CDR+PRDR of the project.

2 Requirements

The ITB must be able to recognize the bunch of the event.
The ITB must decode the Run-Time command.
The ITB must adhere to the BaBar transmission protocol.
The ROM module must be able to monitor, debug the ITB and must be able to enable/disable channels.

3 System Description

The RPC signals are produced in two orthogonal planes of strips, the total amount of 42000 strips is used to readout the whole detector. The building blocks of the DAQ system are the Front-End Cards (FEC) which are used to digitize the information of the strips, each FEC reads 16 strips. The FEC are located very close to the detector inside the iron of the magnet return yoke. When a trigger is received the digital information is transmitted to the FIFO Boards. On each card a Fast-OR signal of the 16 strips is also provided. We propose to use this signal as input to a TDC system to perform the time measurement. The total amount of tdc channel needed is 2615 (one for each FEC), in Fig 1 a block diagram of the Readout chain is shown.

In order to fit the new TDC board in the actual design of the IFR DAQ system some constrains have to be satisfied. The IFR readout is made of 8 FE crates, 4 for the barrell electronics and 2 for each endcap. In these crates we mount the electronics to collect the digital information from the FEC. The crates can host up to 16 slave boards plus one crate controller according to the Glink protocol (not VME crates). The actual readout scheme foresees the installation in the crates of 5-6 IFB and 5-6 ICB plus 1 ICC. So the amount of free slots in each crates is limited at 3-4, the total number of IFR cards or boards is shown in table 1.

In order to fulfill the previous constrains we have started the design of a IFR TDC board with 96 channel, for a total 28 of boards .The actual project is based on a 32 channel chip designed at CERN by the microelectronics group (J.Cristiansen) for LHC application.

4 TDC chip description

The TDC manual can be found at the address http://pcvlsi0.cern.ch/publi-by-project.thml .

Board	Quantity
strip	42000
FEC	2615
IFB	42
ICB	42
ITB	28
ICC	8
FE Crates	8
ROM	8
DAQ VME Crate	1

Table 1: IFR Electronic Boards

Here we describe only the most important feature of this chip. It is a CMOS custom circuit using the basic gate delay as the base for the time measurement. In this tdc a self calibrating scheme is implemented by using the voltage controlled delay elements as part of a Delay Locked Loop (DLL).The fine time measurement from the DLL is extended to a 21 bit dynamic range by a 16 bit coarse time counter.

Each channel consist of two time register where the measurement are stored until they can be written in a common on chip 256 word deep event buffer.The measurement stored in the on-chip event buffer can be passed in a trigger matching function to select the event related to the trigger. The events selected can be passed to a 32 words deep read-out FIFO. Another 8 word deep FIFO is available on the chip to store triggers coming in a short time interval. A time trigger latency and a time window of programmable sizes are available for the trigger matching to accomodate the time spread of hits related to the same events.

4.1 Technical Specification

Number of channel	32+1 common start
Clock frequency	30 to 60 MHz
Time Bin size	0.78 ns at 40MHz
	0.52 ns at 60MHz
Differential non linearity:	Max = $\pm$0.16ns,RMS=0.071ns,at 40MHz
	Max = $\pm$0.13ns,RMS=0.063ns,at 60MHz
integral non linearity:	Max = $\pm$0.23ns,RMS=0.11ns,at 40MHz
	Max = $\pm$0.28ns,RMS=0.13ns,at 60MHz
time resolution :	0.29 ns at 40 MH
	0.20 ns at 60 MHz
Difference betw chan:	Max one time bin
variation with T :	Max one time bin
Dynamic range:	21 bit
Double pulse resolution:	10 ns
Absolute max hit rate:	fclock/4
Events buffer size:	256
Read-out buffer size:	32
Trigger buffer size:	8
Power supply voltage:	4.75 - 5.25
Temperature Range :	-40 80
Hit input threshold voltage:	standard TTL

5 ITB description

The card proposed for BaBar is based on 3 chips, 96 channels.The block diagram is shown in Fig 2.

. The ungated ECL signal coming from the FAST-OR must be converted to TTL to be used as input to TDC. The TDC will use the System frequency at 59.5MHz as input frequency and will work in the multi-hit mode (no start channel used). The SYNC signal of the protocol will be used to reset all the time counters of the TDC (no action on the DDL). The L1 trigger and the related time stamp are the information needed to perform the trigger matching, having programmed the right trigger latency and time window.

To read-out the three chips on a common bus a simple token ring read-out protocol is available on the chips, the operation can be started by the Read-Event command. A FSM (PLD) can handle the operation.

A important a part of the chip is the JTAG interface which can be used to program the chip (start-up procedure), to monitor and to debug this devices. In order to handle this complex operation we plan to use a microcontroller as interface between the command of the BaBar protocol and the chip. A Programmable Logic Device (PLD) is needed to decode the command of the BABar protocol and to produce the fast control signal and the detector local commands.

6 Interface to DAQ

6.1 Global and Subsystem commands

The Fast Control commands will be used in the ITB in the following way:

L1T: to start selectig readout of event-FIFO
SYNC: as a reset of the time counters
READ-EVENT: to start the readout cycle
CALIB: ....

The Board must decode the Run-Time commands according to the BaBar protocol. Some Non-Run Time Commands must be defined to control and monitor the TDC. The operation mode of the chip can be loaded from the microcontroller as start-up procedure, we only need to monitor the condition.

The following commands will be defined:

1) READ-STATUS,code xxxx, data 5 bits, to read the error status bits.

2) READ-CONTROL,code xxx, data 33 bits, to read the enable/disable registers.

3) WRITE-CONTROL, code xxx, data 33 bits, to write the enable/disable register.

4) READ-SETUP, code xxx, data 127 bits to read set-up registers which are set by microcontroller

5) READ-BSCAN, code xxx, data 89 bits, to read the boundary scan register.

The CAEN produced a VME board (V667) with 2 TDC (64 channels). We bought this module to get experience on this TDC, to learn how to program the chip and to project the new IFR board. In future the same module can be used as set-up to debug problems on the chip, in fact the CAEN board foresees a complete set of commands which allow a complete test the chip. On the ITB we will implement only the minimum amount of command to work with, if a major problem appears we can dismount the chip and debug it on the CAEN board.

6.2 Data Words

The data word is made of 32 bit and is organized in the following way :

bit 0-4 Vernier Counter
bit 5-20 Coarse counter
bit 21-25 channel number
bit 26-27 chip number
bit 28 error bit (it's the OR of 5 error conditions)
bit 29-31 board number

6.3 Feature Extraction

The readout of the TDC chip is based on trigger time matching and the length of the events is not fixed as for the IFB board. Since the TDC board will be read together with the FIFO board, the IFR event will be of variable length, so we have to define a unique trailer for the full events. The Header event will contain information like event counter, type of data (calib/data) time stamp had also some geographic information.

7 Calibration and Monitor

A possible scheme for calibration foresees the use of the ICB signal. In the chip it is possible to program channel adjustment constant, this makes the program running on DAQ board simpler and faster.// Work on calibration is still in progress.

8 Schedule

See WBS

9 Cost

See WBS

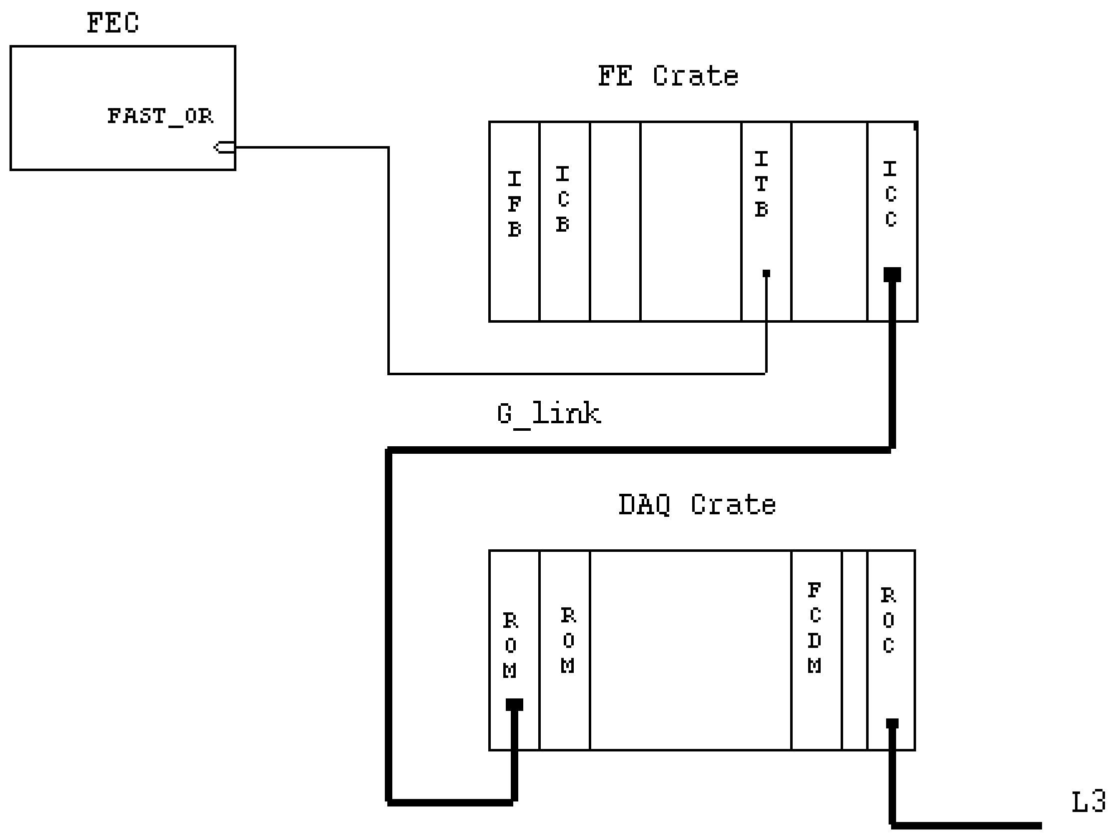

Figure 1: FIG 1 The Layout of TDC Readout.

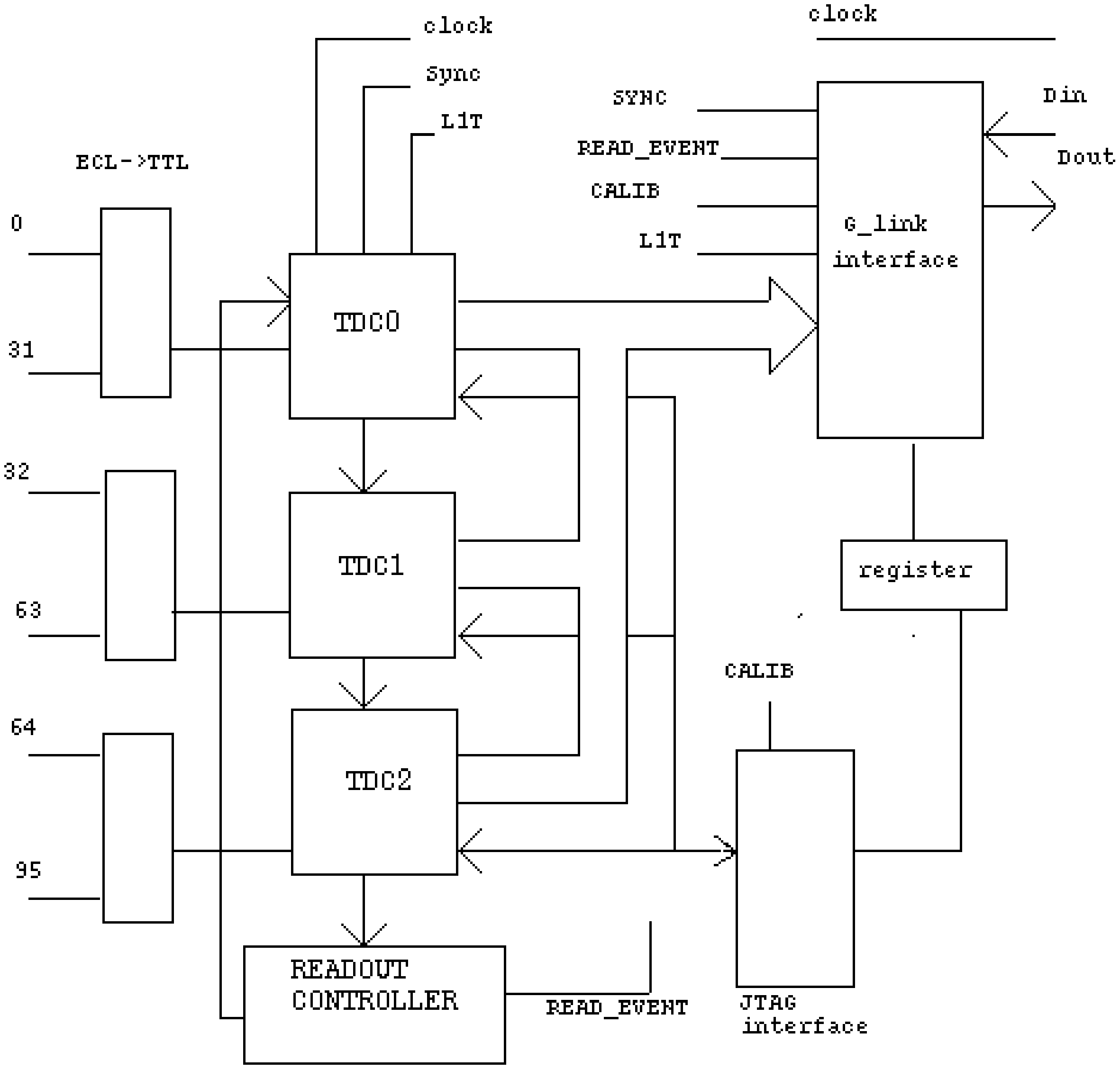

Figure 2: Fig 2. The Block Diagram of the ITB Module