Front End Analogue Electronics

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Input Signal Comparator Preamplifiers Simulations

06-Mar-01



Input Signal from PMT

| Rise/fall time: | 1ns. |
|-------------------------|--|
| Width: | 5ns. |
| Mean Period: | 1μ s. |
| Peak Period: | 10ns. |
| PMT Gain (very conserva | ative) : |
| | 3x10 ⁵ . (Q=4.8x10 ⁻¹⁴) |
| Peak current from PMT: | 7μ Α. (I=Q/T) |



Current Preamplifier

Preamplifier Gain: ~10. Bandwidth: ~100Mhz. Low input impedance. Low power consumption. We choose current preamplifier because: natural consequence for the anode signal. more easier to have low input impedance. reduced voltage swings reduces cross-channel coupling. We made 3 designs in current mode. All with VDD=3.3V and VBIAS= 2V.



CMA Preamplifier



A variation of the input current change the source voltage of the input transistor **I0** producing a current at the drain node which is mirrored to the output branch. Low Zin= 1/gm0. High Zout=1/gds5. Gain=10. Bandwidth=120Mhz. **Two additional MOS** for test.



MA Preamplifier



A more simple design . Only current mirror. (only 2 MOS). **Bandwidth=** 250Mhz. Gain=10. Increase Zin. Same power.



WMA Preamplifier



We use Wilson current mirror. Bandwidth= 85Mhz. Increase power. Gain=10. Zin like CMA. Increase Zout.

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Comparator

Double hit resolution:10ns.Threshold current:20μA.Output Level compatible with standard cells CMOS.Power available for channel:1mW.Current discriminator has a higher precision and
lower current consumption than voltage
discriminator.We always used Analog Artist (Cadence) for all
simulations .

Classic Comparator

The keys element are I12 (NMOS)and I17 (PMOS) (next slide). They form a source follower input stage. First stage gives the ability of applying feedback to the gates. To achieve sufficient gain for amplifying small voltage variations at the input stage node, positive voltage feedback from a CMOS inverter is used.

This design involves low delay times and low input impedance.

In the design DIFF is the input current resulting from the subtraction of a reference current (threshold mirrored) from the output preamplifier current.



euso clossic schematic : Feb 19 09:57:42 2001



 Period:
 50ns.

 Steady power:
 280.63 μW
 (85.05 μA)

 Impulsive power:
 618.4 μW
 (187.85 μA)

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New Comparator

Increase speed for very low input current.
Key element is MOS I24 (diode connected) to provide the voltage drop between first 2 MOS.
Simulations show there are many stages. It means much power consumption.

 Period:
 50ns.

 Steady power:
 409.53 μW
 (124.1 μA)

 Impulsive power:
 1033.89 μW
 (313.3 μA)







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CompaIta

Quite similar to classic comparator.

Compared to classic comparator, two transistors have been introduced at the second stage. They operate in the diode configuration to shift down the gate voltage of I17 and shift up the gate voltage of I12 (compared to the output voltage).

We have lower delay times and more or less the same power compared classic comparator.

The output signal presents higher rise and fall times.







 Period:
 50ns.

 Steady power:
 306.77 μW
 (92.96 μA)

 Impulsive power:
 476.85 μW
 (144.5 μA)

Power Consumption

| Comparator | Background Power (1 μs) (average) | Back + Signal Power (10ns) (average) |
|------------|---|--|
| Classic | 280.4 μW | 470.51 μW |
| New | 402.16 μW | 691.73 μ W |
| Compaita | 300.59 μW | 412.01 μW |



Test Chip Plans

We want to do test about several possible configurations, putting together the three preamplifiers with the three comparators.

In this way, we have 9 various channels to put in the analogue part of the chip. So we choose the best one after the physical test.

However we add also the preamplifiers and the comparators stand alone so we can measure their performance.



