

EUSO CHIP STATUS REPORT

EUSO electronics meeting 5-6 March 2001 - GENOVA

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- Architecture of EUSO chip **PERSEO**
- Technology and tools
- Prototype test chip
- Future plans

PRELIMINARY SPECIFICATIONS FOR THE EUSO FRONT END CHIP

- ✓ Reference document: “AIRWATCH FROM SPACE”
- ✓ 64 channels chip. Mapping one to one with the R5900-M64 PMT anodes
- ✓ On chip circular memory buffer
- ✓ Serial interface for working parameters configuration
- ✓ Power budget: about 1 mW/ch
- ✓ Single photon double pulse resolution: ≈ 10 ns (≤ 20 ns)

SINGLE CHANNEL LOGIC

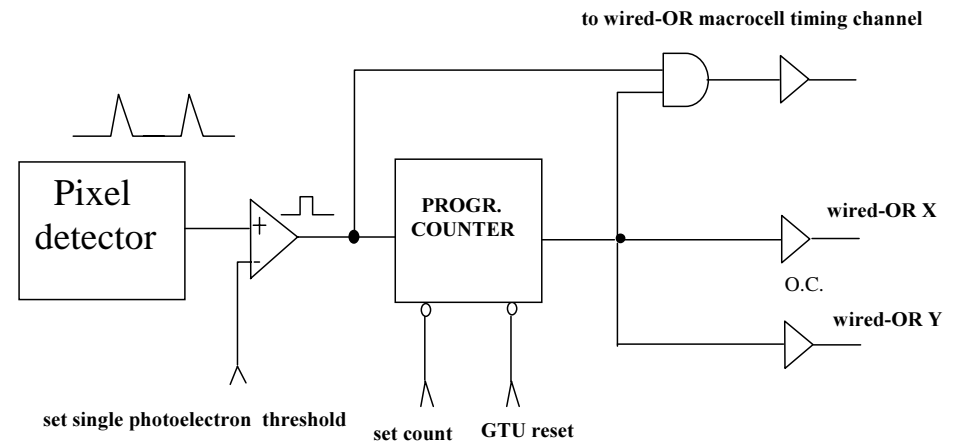
Mask after the discriminator
to disable noisy pixels

8 bit programmable down counter
with async reset/reload
 $T_{ck} = 10 \text{ ns}$

Outputs to generate row
column and timing signals

Possibility to have a low resolution
timing information (50-100 ns)

Additional outputs for local trigger logic?



PERIPHERY LOGIC

SRAM memories to store
rows, column
(and timing) data

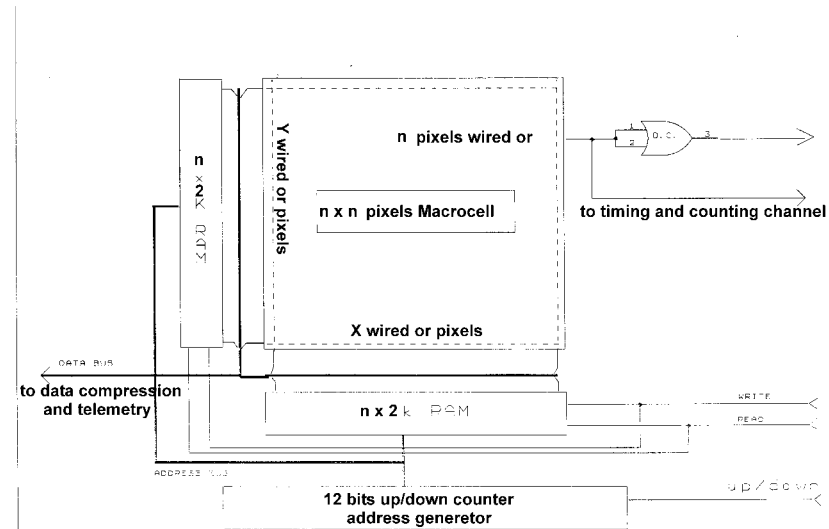
Address generator:
UP/DOWN counter

Bus steering logic for reading/
writing memories

High speed timing output

The global OR can be done with the last dynode signal, using
a 65th channels identical to the others (more or less).

Local trigger logic ?



TECHNOLOGIES AND TOOLS

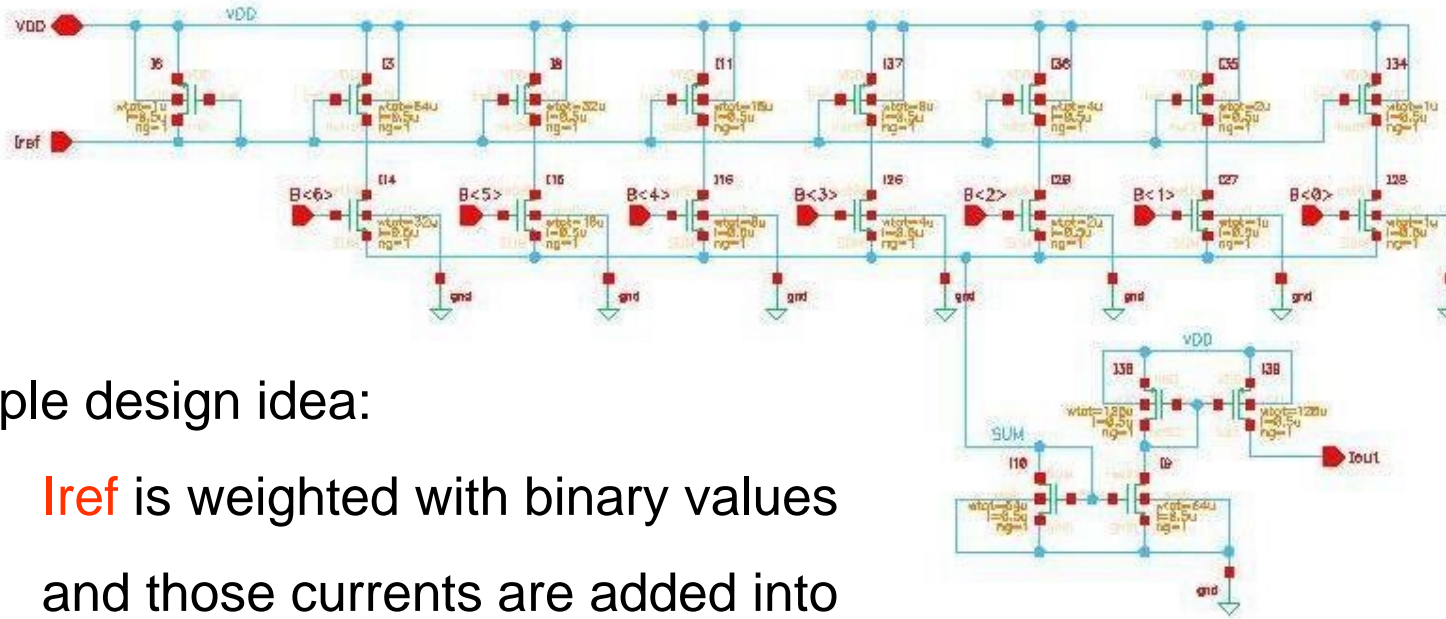
- ✓ AMS 0.35 μm , 2 Poly 3 Metal 5V I/O, available through EuroPractice
chosen for the test chip and suitable for the final chip
design care for Latchup and SEE problems
- ✓ IBM 0.25 μm , 1 Poly 5 Metal 2.5V I/O, available through RAL
RAD hard standard cell library
design rules for RAD hard analog circuits (enclosed gate MOS)
used by CERN groups for LHC experiments

Both technologies have design kits for CADENCE v 4.4.3,
Synopsys, Verilog, Spectre (AMS), Hspice

PROTOTYPE TEST CHIP

- ✓ Test of different kinds of preamp-discriminator pairs (Fabio).
- ✓ Test of voltage and current reference circuits.
- ✓ Test of current output DAC used to set up thresholds and biases.
- ✓ Test of a simple serial interface to load configuration parameters.
- ✓ Test of small parts of single cell digital circuits (counter, comparator, ...) in order to see how to integrate full custom analog cells with standard cell library blocks.
- ✓ If we'll have time we'll try to put in also some of the periphery logic (SRAM, address generators, ...)

FIRST 7 BIT DAC DESIGN



✓ Simple design idea:

I_{ref} is weighted with binary values
and those currents are added into
the **SUM** node if the corresponding
 $B<i>$ is active

✓ Layout care for maintain linearity

SIZE, CONDITIONS AND COSTS

- ✓ Expected pin count: ≈ 80 pins
- ✓ Expected area: $\approx 3 \times 3 \text{ mm}^2$ (pad limited)
- ✓ Deadline for MPW submission: 6 June 2001
- ✓ Delivery of 10 untested prototypes after 13 weeks
- ✓ Silicon cost: 590 Euro/ mm^2 , minimum 12 $\text{mm}^2 \Rightarrow \approx 7100$ Euro
- ✓ Package cost (84 pin JLCC): 56 Euro $\times 10 = 560$ Euro
- ✓ Total cost: ≈ 7700 Euro

PLANNING

- ✓ Schematics ready by 15 March
- ✓ Layout of single cells ready by 30 April
- ✓ Full layout ready by 15 May
- ✓ DRC, LVS and backannotation by 20 May
- ✓ GDS II files ready by 6 June ← DEADLINE
- ✓ Design and fabrication of chip test board in June and July
- ✓ Chips back to Genova by 10 September
- ✓ First chip turned on by 11 September

OPEN QUESTIONS

- ✓ Electronics working conditions: temperature range ?
- ✓ Power budget for the front end: still 1 mW/ch ?
- ✓ ...