Rework of flip chip bonded radiation pixel detectors

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Abstract

In this paper, some practical aspects of reworking flip chip hybridized pixel detectors are discussed. As flip chip technology has been advancing in terms of placement accuracy and reliability, large-area hybrid pixel detectors have been developed. The area requirements are usually fulfilled by placing several readout chips (ROCs) on single sensor chip. However, as the number of ROCs increases, the probability of failure in the hybridization process and the ROC operation also increases. Because high accuracy flip chip bonding takes time, a significant part of the price of a pixel detector comes from the flip chip assembly process itself. As large-area detector substrates are expensive, and many flip chip placements are required, the price of an assembled detector can become very high. In a typical case, there is just one bad ROC (out of several) on a faulty detector to be replaced. Considering the high price of pixel detectors and the fact that reworking faulty ROCs does not take much longer than the original placement, it is worthwhile to investigate the feasibility of a rework process.

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1. Introduction

One way to build large-area hybrid pixel detectors is to place several readout chips on a single sensor. The probability of soldering flaws or malfunction of the readout chips (ROCs) increases as the number of chips increase on the sensor. Radiation detectors may become inoperative due to thermally induced damage during the assembly process, poor solder interconnections, or erroneous handling of components. The manufacturing costs of operational or inoperational detectors are the same and therefore there is an interest to repair faulty detectors by replacing chips that operate outside the specifications.

2. Overview of flip chip process

VTT normally uses wafers, that have been tested (probed) by the customer, and they will be run through the bumping and bonding process [1]. To optimize the flip chip conditions, solder is used on both parts to be bonded, and both the readout and the sensor wafers go through essentially the same process. Most (2/3) of the solder volume is electroplated on the readout side, and 1/3 on the sensor side (Fig. 1). After the bumping process, readout wafers are thinned and polished. Before flip chip bonding, the wafers are diced, and the integrity of bumps is inspected visually. Only chips that have passed the customer’s wafer-level electrical tests are used for flip chip assembly (known good die).

Flip chip and rework operations are done with Suss Microtec FC150 flip chip bonders, and the so-called Universal Bonding Arm (UBA) is used. Due to the small size of the bumps and a large chip size, the components must be levelled (i.e., adjusted parallel) first, and then aligned before the bonding cycle. If the components are not adjusted parallel, the bonding force will be distributed unevenly over the chip, and the most compressed bumps will create solder bridges (electrical shorts) with the neighboring bumps.

A thermocompression process is used for tack bonding, where the bumps are compressed and mechanically locked
to one another. After all of the ROCs have been placed on the sensor, the detector goes into assembly reflow. The solder bumps are reflowed in a formic acid/Ar ambient, which creates strong and oxide-free bump bonds.

3. Rework considerations

The rework of flip chip bonded pixel detectors comprises six steps (Fig. 2), in which the faulty ROC is removed from the sensor and a new ROC is hybridized in its place.

There are several important aspects related to rework:

1. None of the bumps should come off with Ni under bump metal (UBM) from either side, because the corresponding pixels would be lost in the final detector.

2. Creation of shorts is possible when making the initial contact between the bonding arm and the chip to be removed. The risk can be minimized by programming the right range of temperatures on the chuck and the arm.

3. Handling of detectors must be very gentle. Any hits or drops might result in an increased leakage current in the sensor. A maximum limit for leakage current is typically specified for good detectors.

4. Rebonding might be problematic if the detectors have been handled outside a clean room. All dirt on the surfaces of the parts to be hybridized will reduce the accuracy of the new flip chip placement.

The removal of chips is the most critical step in the rework process. Therefore, issues related to the chip
removal phase are dealt with in more detail in the following subsections.

3.1. Bump strength

Some wet etching solutions, as used for etching the sputtered Cu, tend to underetch the bump base. The mechanical strength of a bump is inversely proportional to the square of its diameter. The underetching becomes worse when the wafer size gets larger, and it is usually worst at the perimeter of the wafer. It is desirable that the same rework process can be used for all rework candidates. Therefore, the strength of bumps will become a critical issue, because the bumps have to stand a certain tensile stress during the removal of the ROC. If too many bumps come off with the UBM metals from sensor, the detector will be ruined. Spray (spin) etching and dry etching processes are desirable due to less underetching.

3.2. Division of solder volume

Solder partitioning can be varied by adjusting temperatures separately on the chuck and the arm during the chip removal phase. Temperature ramps and pulling rates can be programmed on the flip chip bonder. When a ROC is pulled away from the detector, the solder will be strained from the hotter side.

In the chip removal phase, most of the total solder volume is intentionally pulled away with the ROC, leaving only a little solder on the sensor substrate. In this respect, the uneven division of the solder volume between the readout and sensor chips favours the rework purposes, enabling similarly bumped ROCs to be used for both initial detector assembly and rework. In addition, it has been observed, that it is worthwhile to leave some solder on the Ni pads of a sensor to improve wetting. If only a small amount of solder is left on the sensor, the bonding of the new readout chip should be easy, because the risk of creating short circuits is minimized.

3.3. Rebonding

After the ROC removal, the detector will be taken into reflow in order to reduce the surface oxides of solder and to get hemispherical bumps (Fig. 3). The goal is that the bump structure of the sensor resembles the original state (Fig. 1) after the bumping process.

After the reflow, a new ROC will be bonded on the detector and the assembly run through reflow. The bonding of new ROCs should work well if the surfaces are clean, enabling an easy parallelism adjustment between the chip and the sensor.

4. Rework results

The rework data presented in this paper, are from the production of ALICE ‘ladder’ pixel detectors. Each ALICE detector consists of five ROCs bonded onto a silicon sensor chip. On each ROC, there are about 8200 SnPb solder bumps, which have a nominal diameter of 30 μm [2].

4.1. Before rework

After the assembly at VTT, the ALICE detectors were sent to CERN for electrical and radiation tests [3]. The test data used in this paper covered 445 detectors. 343 detectors were within and 112 outside the spec, giving a flip chip production yield for ALICE detectors of 77% (Fig. 4). The most typical reasons for failure in detector operation were too high a leakage current, too many bad bump bonds within the bump array of a ROC, and malfuntioning.
ROCs. The bad bump bonds refer to the shorts and/or open bump contacts.

It was decided that it was worthwhile to rework a maximum of two chips out of the five in an ALICE ladder detector. Three or more chip replacements would have required more work than building a completely new ladder from scratch. Sensors with an excessive leakage current were not reworked. 74 detectors satisfied the rework conditions above, which was 17% of the total amount. In case of reworked detectors, 1 or 2 chips were replaced, and the detectors were sent to CERN for retesting.

4.2. Rework yield

After retesting the 74 reworked detectors, the number of ladders within spec increased by 62 units (from 343 to 405). In Table 1, chip-level and ladder-level rework yields are given. Two yield numbers have been calculated, because in some cases two readout chips were replaced on the detector. Fifty-nine ladders had only one ROC replaced; 53 were successes, and 6 were failures. Fifteen ladders had 2 ROCs replaced; 12 were successes, and 3 were failures (only one ROC of the replaced two failed in each). For the chip-level yield, all individual successful replacements have been counted. This is to give a generic estimate that can be used for various numbers of ROCs. The ladder-level yield takes also into account the cases where only one out of the two replacements was successful. In some cases a successful ROC replacement led to a situation where one of the original ROCs or the sensor chip degraded, and therefore 12 of the reworked detectors remained outside the spec.

5. Conclusions

The successful establishment and realization of a rework process increased the overall yield of ALICE flip chip production from 77% to 91%, and a significant amount of material and money was saved. Rework works well if the failure type in the detector is bump bond related, or the ROC is malfunctioning. Rework is a cost-efficient way to increase the yield of flip chip process, when underfills are not used.

References