Flip chip bumping technology—Status and update

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Abstract

Flip chip technology is a key driver for new complex system architectures and high-density packaging, e.g. sensor or pixel devices. Bumped wafers/dice as key elements become very important in terms of general availability at low cost, high yield and quality level. Today, different materials, e.g. Au, Ni, AuSn, SnAg, SnAgCu, SnCu, etc., are used for flip chip interconnects and different bumping approaches are available. Electroplating is the technology of choice for high-yield wafer bumping for small bump sizes and pitches. Lead-free solder bumps require an increase in knowledge in the field of under bump metallization (UBM) and the interaction of bump and substrate metallization, the formation and growth of intermetallic compounds (IMCs) during liquid- and solid-phase reactions. Results of a new bi-layer UBM of Ni–Cu which is especially designed for small-sized lead-free solder bumps will be discussed.

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1. Introduction

Assembly and packaging technology continue to change rapidly. In the last decade packaging has changed from simple single-die packaging to a complex system integration technology which represents an integral prerequisite for the manufacturing of new electronic products. Assembly and packaging needs are driven by market application requirements as well as silicon technology. Cost will drive technology trade-offs for all market segments. System in Package (SiP) technology has rapidly evolved from specialty technology used in a very narrow set of markets to a broad market base. The primary driver for SiP technology has been the need for more compact, more highly integrated electronics.

Permanently growing integration density and increasing complexity of integrated circuits lead to further reduced I/O pitches. A general roadmap, forecasted by ITRS [1], of selected parameter for devices (memory, µP and ASICs) regarding I/O counts, pitch frequency and power dissipation is presented in Table 1.

The selection of the interconnection technology for a specific application depends on topological, electrical and thermal considerations as well as reliability requirements, manufacturing and testing issues. The application of chip and wire bonding, which is the most commonly used interconnection technology today, is limited in terms of high I/O number, pad configurations and smallest pitches.

Flip chip (FC) technology offers several advantages especially for high dense interconnects because the whole chip surface may be used for a large number of I/O pads in area array configuration. Shortest interconnection lengths result in excellent electrical performance of interconnects as well.

2. Flip chip and bumping technologies

FC technology in contrast to chip and wire needs an additional process on wafer and/or substrate level—the bumping [3-5]. Depending on the selected joining process different bump configurations are used (Fig. 1). An overview about currently used bump metallization for different applications is given in Table 2.

For the metallization of the I/O pads, different bumping techniques have been developed. The most important are evaporation, electroplating, mechanical stud bumping and solder paste printing on wettable metallization like Ni/Au, as well as solder dispensing, immersion and solder transfer
techniques. Each technique meets different requirement in terms of bump sizes, pitches, metallization, etc. Solder paste printing meets the requirement regarding low cost but this process is limited to minimal bump pitches of 150 μm today.

Wafer bumping by electroplating however, has the largest potential for realizing highest I/O densities with a pitch range from 200 to 25 μm. It is particularly suited for high volume production of bumped wafers at a high-quality standard. As the value of wafers increases, the relatively high processing costs are less and less perceptible.

The realization of bumps using electroplating can be divided into fundamental process steps, which are sputter-etching of the plating base, photoresist patterning, electroplating, differential etching, and, if required, a final solder reflow as shown in Fig. 2.

The selection of the suited bump metal and under bump metallization (UBM) depends mainly on the assembly process, the allowed joining temperature, the melting point of the solder, the integrity of the interfaces between the bump and the adjoining bond pad metallization, the bumping process compatibility and reliability requirements.

To preserve the structural integrity of all assembly parts, the temperature hierarchy in the package processing must be taken into consideration as well. All bump variations listed above are well established on 4"–8" wafers at Fraunhofer IZM and available for specific customer requests.

3. Bumping process by electroplating

Typically, circuit device wafers have aluminum alloy pads and an inorganic (e.g. SiO₂, Si₃N₄, SiON) or organic passivation opened over the pads. InP or GaAs semiconductors for photonic and RF applications are using gold pads.

By an initial sputter-etching step, the wafer surface is cleaned of contamination and metal oxides. After back-sputtering an adhesion layer of Ti:W(N) with a thickness of 100–230 nm is sputtered on the whole wafer, followed by a second layer of either 300 nm Cu or 200 nm Au as a plating base. The specific addition of nitrogen (N₂) during deposit of Ti (5 wt%) W (95 wt%) enhances the diffusion-barrier property. A Ti:W(N)/Au bump structure on aluminum pads has shown no degradation after annealing at 400 °C (1 h). With optimized sputter conditions, a low-stress deposition and a good homogeneity of layer thickness are achieved without any damage of CMOS structures [2].

Spin coating is used to deposit the high-viscous photoresist onto the wafer in the desired layer thickness.
Layers of more than 45 μm can be realized by multi-spin coating with a good thickness homogeneity on all standard wafer sizes (4″–8″). The used positive resist (AZ series) system shows a high transparency in the near UV spectrum, therefore a high depth-to-width aspect ratio and steep slopes of the generated structures are possible even in thick films.

To dry the spin-coated resist film it is prebaked before printing. Then the wafer is aligned and exposed in the pad regions, which later will be covered by the bump structures. The exposed areas dissolve during the development in an alkaline fluid and the resist pattern appears. A final postbake is made to stabilize the photoresist for the following electroplating process. Especially for fine pitch
bumping, a fine-tuning of the exposing, developing, and baking procedures is inevitable to get a high lithographic yield. Besides the resist patterning, another important aspect for the suitability of the photoresist system for bumping is an easy removal after the metal deposition. The bump metallurgy must not be corroded by the remover, and mechanical damage must absolutely not occur due to a swelling effect of the resist, which is not given by all resist systems.

Today a number of commercial electroplating baths for different metals are available. The bath chemistry must be compatible to the photoresist system and should be insensitive to out-bleeding. Exceptionally cleaned make-up ingredients ensure deposits with a high purity and consequently well-defined electrical and mechanical properties. For solder bumping, a low co-deposition rate of organics is required to guarantee a low volume of out-gassing during the reflow and bonding process. For this reason, relatively matt depositing electrolytes with a small amount of organic additives are preferred. Furthermore, the deposits have to show a well-defined bump shape and solder-alloy composition, low internal stress, non-porosity, as well as a negligible number of defects caused by dendrite formation, pittings or particle encapsulation. These attributes as a whole have to be adjusted by a suitable combination of all relevant deposition parameters like concentration of electrolyte components, current density and agitation strength. In particular cases, the optimization depends on the specific pattern layout as well.

Figs. 3 and 4 show plated Au bumps and fine pitch solder bumps.

4. Bump reliability

The demand for Pb-free and high-density FC interconnection technology is growing rapidly. Lead-free FC solder joints require an increase in knowledge in the field of UBMs, solder materials, board metallization as well as in the interactions between these elements. Common UBMs have been tested with various lead-free solder systems to study the formation and growth of intermetallic compounds (IMCs) during liquid and solid-phase reactions [3]. Due to a high rate of IMC formation related to the consumption of the UBM these UBMs are often not recommended for lead-free applications at elevated tem-
perature (150 °C) for devices with small solder joints. For such applications it would be advantageous to use UBM showing a limited formation of IMCs at the interface UBM/solder to maintain the plasticity of the interconnect and the adhesion of the UBM to the diffusion barrier. A number of different UBM–solder configurations (e.g. Cu–PbSb60, Cu–SnAg, NiV/Cu–SnAg, Cr–Cu/Cu–SnAg, TiW/NiV) are investigated and results are reported in Refs. [4,5].

There are several possibilities to slow down the process of formation of IMCs occurring during liquid- and solid-phase reactions between UBM and lead-free solder. Materials showing slower formation of IMCs than others may be chosen as UBM as it is true for Ni in comparison to Cu. In this case the process of UBM consumption is slowed down but it is not stopped. The problem that a Ni UBM tends to detach easily from the diffusion barrier layer after its total consumption due to IMC growth remains.

The lifetime of a single-layer UBM (e.g. Cu) can be prolonged by increasing the thickness of the UBM. It is also possible to use alloy solders slowing down the UBM consumption as well. As the control of a multi-component bath for electroplating is difficult it is not opportune to electrodeposit Sn–Ag–Cu alloys as solder material.
A bi-layer Ni/Cu UBM for small-sized lead-free solder-bumps was investigated to stabilize the formation of IMC and to increase the bump reliability.

Fig. 5 shows cross-sections prepared from bumps after the chips had undergone thermal aging at 150 °C (1000 h) with UBM 1 (1.5 μm Ni/150 nm Cu) and UBM 2 (1.5 μm Ni/500 nm Cu). For UBM 1 a consumption of UBM was observed during solid-phase reaction connected to a growth of interfacial IMCs between UBM and solder. For UBM 2 no changes were observed at the interface UBM/solder.

Fig. 6 shows both UBMs after liquid-phase reaction at 250 °C for 90 s (reflow conditions). Using UBM 1 a (Ni,Cu)₃Sn₄ layer is formed in the early state of liquid-phase reaction. Solder is in contact to the Ni layer initiating and allowing further growth of a Ni₃Sn₄ or (Ni,Cu)₃Sn₄ formation.

In the case of UBM 2 a thin (Cu,Ni)₆Sn₅ layer covering the Ni layer is suitable to prevent the formation of Ni₃Sn₄. A closed layer of (Cu,Ni)₆Sn₅ is formed and prevents the consumption of the Ni layer of the bi-layer UBM. The Cu layer serves as sacrificial layer forming (Cu,Ni)₆Sn₅ IMCs during reflow. This (Cu,Ni)₆Sn₅ IMC layer is suitable to block interdiffusion between Ni and the solder during solid-state aging.

Liquid-phase reaction for both UBM constructions compared to Ni were also studied up to total duration of 900 s (Fig. 7). A 1.5 μm thick electroplated Ni UBM is already consumed after 900 s and spalls into the solder. With UBM 1 the appearance and growth of Ni₃Sn₄ IMCs were observed. UBM 2 withstands multiple reflow up to a total time of 900 s where only a slight degradation of the UBM becomes visible [6,7].

6. Summary

Electroplating for bump formation is the technology of choice for high-density FC applications with a high yield. With this technology different solder compositions and metal structures can be realized. Compared to solder paste printing, pitches of approx. 150 μm (state-of-the-art), bump sizes of 10 μm diameter and 20 μm pitch are currently seen as a limitation for electroplating. Sensitive areas on device wafers (e.g. sensors) can be protected by a temporary layer during bump processing.

Small-sized solder bumps (diameter < 20 μm) need an improved UBM construction. For lead-free solders (SnAg, SnCu, Sn) an UBM stabilization effect can be achieved by an adjusted bi-layer UBM of Ni–Cu.

Lead-free bumps with AuSn are well suited for flux-free FC assembly especially for photonic and RF applications [8]. This process can be easily implemented with electroplating as well. High stand-off bump construction (e.g. pillar bumps) at fine pitch can only be realized by electroplating. New bump construction (e.g. 3-axes compliant bumps) and nano-interconnects are under development for TCE matching chip-substrate and low-temperature assembly.

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