

# GETTING STARTED WITH MULTICHASSIS SYNCHRONIZATION USING THE NI PXI-6653 AND THE NI PXI-4472

The NI PXI-6653 Timing and Synchronization Module enables you to pass PXI timing and triggering signals between two or more PXI chassis. This module is especially useful for synchronizing acquisitions involving large numbers of NI PXI-4472 modules. Tight multichassis synchronization guarantees simultaneous sampling and minimal interchannel phase mismatch in high-channel-count systems.

This document describes three typical hardware configurations where the NI PXI-6653 (NI 6653) enables synchronization for NI PXI-4472 (NI 4472) Dynamic Signal Acquisition (DSA) modules located in multiple PXI chassis. The necessary hardware, signal connections, and example code are described for each configuration.

NI highly recommends that you thoroughly review the *Theory of Operation: Synchronizing Data Acquisition Across Multiple NI 4472 Modules* section before running the application examples or starting your application development. Although this document includes code snippets and provides a cursory discussion of some software functions, it is not intended to be a software user manual or reference manual. The main goal of this section is to familiarize you with the NI 4472 synchronization signals and with how the NI 6653 hardware can extend this synchronization beyond a single PXI chassis. After familiarizing yourself with the concepts described here, move on to the LabVIEW or C example programs before beginning your software development.

The *NI PXI-6653 User Manual*, NI-VISA documentation, and MXI-3 documentation might be useful to you as you read this document. These documents can be downloaded from [ni.com/manuals](http://ni.com/manuals).

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December 2002  
323403A-01

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# Conventions

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The following conventions are used in this document:

<>

Angle brackets that contain numbers separated by an ellipsis represent a range of values associated with a bit or signal name—for example, DIO<3..0>.

»

The » symbol leads you through nested menu items and dialog box options to a final action. The sequence **File»Page Setup»Options** directs you to pull down the **File** menu, select the **Page Setup** item, and select **Options** from the last dialog box.

◆

The ◆ symbol indicates that the following text applies only to a specific software version or a specific hardware configuration.



This icon denotes a note, which alerts you to important information.



This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Safety Information* section of *Chapter 1, Installation*, of the *NI PXI-6653 User Manual* for precautions to take.



This icon denotes a tip, which alerts you to advisory information.

**bold**

Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names and hardware labels.

*italic*

Italic text denotes variables, emphasis, a cross reference, or an introduction to a key concept. This font also denotes text that is a placeholder for a word or value that you must supply.

monospace

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames and extensions, and code excerpts.

**monospace bold**

Bold text in this font denotes the messages and responses that the computer automatically prints to the screen. This font also emphasizes lines of code that are different from the other examples.

*monospace italic*

Italic text in this font denotes text that is a placeholder for a word or value that you must supply.

MSVC

Refers to Microsoft Visual C++ development software.

NI 4472	This phrase refers to the NI 4472 for the PXI bus.
NI 6653	This phrase refers to the NI 6653 for the PXI bus.
PC	Refers to the IBM PC/XT, IBM PC/AT, and compatible computers.
PCI	Peripheral Component Interconnect—a high-performance expansion bus architecture originally developed by Intel to replace ISA and EISA.
PCI machine	This phrase refers to a desktop PC with a PCI slot.
PXI	A rugged, open system for modular instrumentation based on CompactPCI, with special mechanical, electrical, and software features. The PXI bus standard was originally developed by National Instruments in 1997, and is now managed by the PXI Systems Alliance.

## Theory of Operation: Synchronizing Data Acquisition Across Multiple NI 4472 Modules

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The following sections provide low-level background information about the electrical signals needed to tightly synchronize NI 4472 modules. The *Synchronizing Signals for Multiple NI 4472 Modules in a Single Chassis* section describes the signals required to synchronize an acquisition when all NI 4472 modules reside in the same PXI chassis. No NI 6653 is required in this case. The *Using the NI 6653 to Route Synchronization Signals Between Multiple Chassis* section discusses synchronization where NI 4472 modules are physically located in two or more PXI chassis. In a multichassis system, two or more NI 6653 modules generate and route the necessary signals to synchronize all NI 4472 channels in the system. The NI 6653 Driver Software package includes application examples that address three multichassis cases.

### Synchronizing Signals for Multiple NI 4472 Modules in a Single Chassis

This section describes the synchronization between NI 4472 modules housed in a single PXI chassis. This section introduces three signals: the oversample clock, the SYNC pulse, and the acquisition start trigger. The *Using the NI 6653 to Route Synchronization Signals Between Multiple Chassis* section frequently refers to these signals.

### Delta-Sigma ADCs and the Oversample Clock

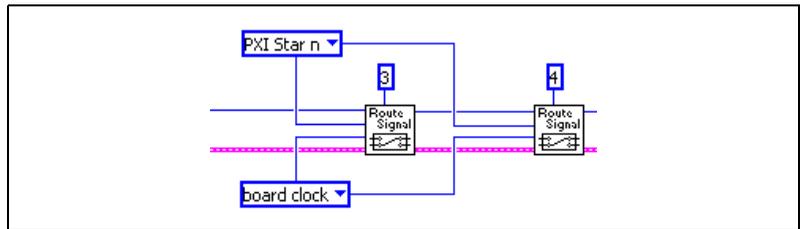
The 24-bit A/D converters (ADCs) employed on the NI 4472 belong to a class of components called *delta-sigma* (or  $\Delta\Sigma$ ) ADCs. The advantages of delta-sigma components as compared to other digitizers include high

dynamic range, excellent linearity, and digital filtering to remove aliased frequency components from the data.

Most ADCs, including the successive approximation ADCs used in many data acquisition (DAQ) devices, are timed by a *sample clock*. This clock is simply a digital pulse train that drives the acquisition. In most cases, a rising edge on the sample clock signal starts a conversion. When an ADC is timed by a sample clock, the acquisition rate is equal to the frequency of the sample clock. For example, a 10 kHz sample clock produces a 10 kS/s acquisition rate.

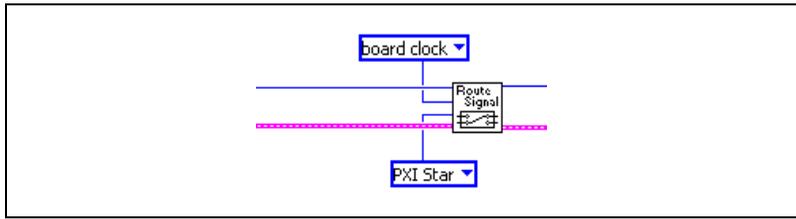
One distinguishing feature of delta-sigma converters, including those on the NI 4472, is that they use an *oversample clock* to drive the conversion. As the name implies, the physical frequency of the oversample clock signal is greater than the sample rate. When a single NI 4472 acquires data, the high-frequency oversample clock is locally generated by a Direct Digital Synthesis (DDS) chip on the device. If two or more NI 4472 modules are run in a single PXI chassis, they must share the oversample clock to provide a tightly synchronized acquisition.

When sharing this clock, one module becomes the “clock master,” and the other modules become the “clock slaves.” The clock master module must be placed in Slot 2 of the PXI chassis. The clock master uses the DDS chip to produce the oversample clock and drive its own acquisition. The clock master also exports the oversample clock to the PXI star trigger bus. Figure 1 shows a LabVIEW code snippet that illustrates how to export the oversample clock to a clock slave module in PXI Slots 3 and 4.



**Figure 1.** Exporting the Oversample Clock to PXI Star

You now order each clock slave device to import the oversample clock from PXI\_Star to drive its ADCs. Figure 2 shows the LabVIEW code snippet for this operation.



**Figure 2.** Importing the Oversample Clock to Drive Slave ADCs

On the NI 4472, the ratio between the oversample ( $f_{os}$ ) clock and the sample rate ( $f_s$ ) can have one of two possible values, depending on the sample rate. Table 1 shows the possible values.

**Table 1.** Relationship Between the Sample Rate and Oversample Clock

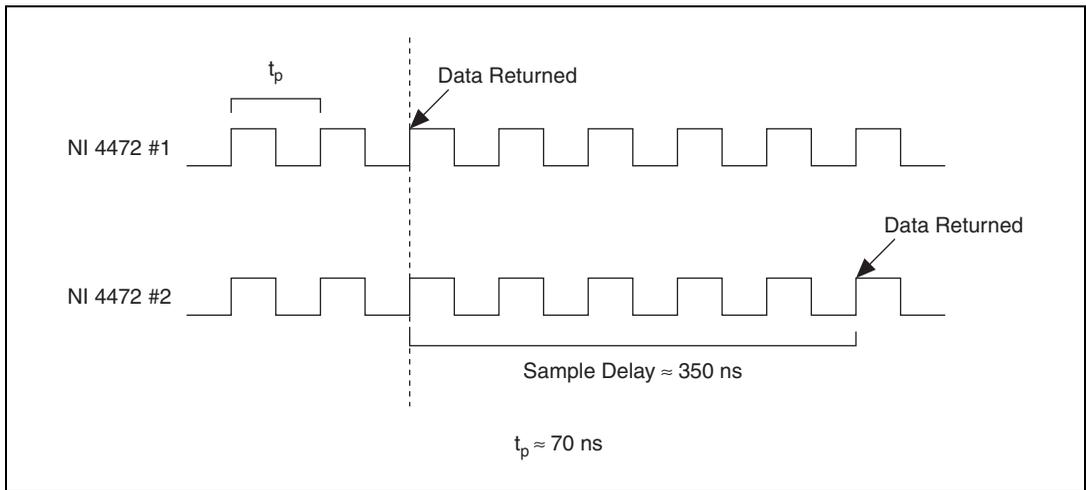
Sample Rate	Oversample Clock
$f_s \leq 51.2 \text{ kS/s}$	$f_{os} = 256 \times f_s$
$f_s > 51.2 \text{ kS/s}$	$f_{os} = 128 \times f_s$

The highest possible oversample frequency for the NI 4472 occurs at either  $f_s = 51.2 \text{ kS/s}$  or  $f_s = 102.4 \text{ kS/s}$ . In both cases, the oversample rate is slightly faster than 13.1 MHz.

Most delta-sigma converters, including those on the NI 4472, require a very steady frequency for the oversample clock. The DDS chip on the NI 4472 has good frequency characteristics and easily fulfills this need. However, arbitrarily changing frequencies, such as those from tachometers, generally do not work well with delta-sigma ADCs. For this reason, the NI 4472 and other National Instruments DSA products do not support external clocking from arbitrary signal sources. This constraint also applies when you use one or more NI 6653 modules for synchronization with NI 4472 devices.

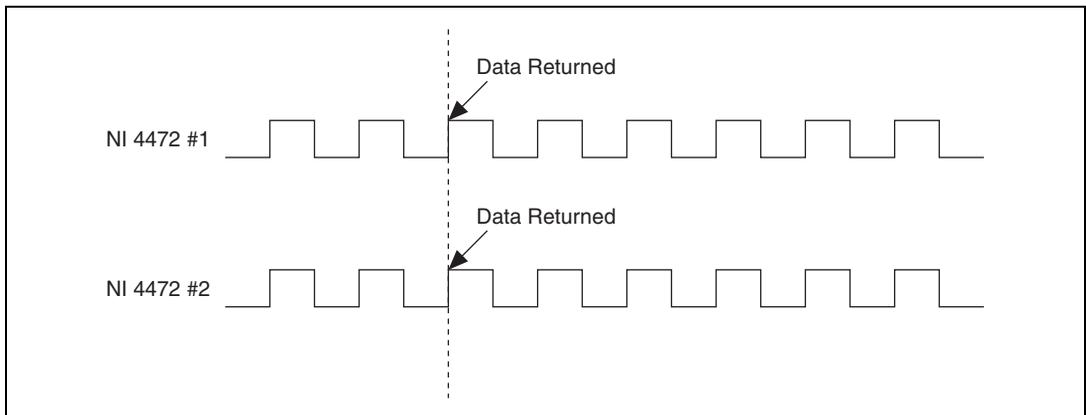
## The NI 4472 SYNC Pulse

As discussed in the [Delta-Sigma ADCs and the Oversample Clock](#) section, the oversample clock is many times faster than the actual acquisition rate of the NI 4472. Using the concepts described in that section, you can share the oversample clock between two or more NI 4472 modules. This sharing guarantees that both modules sample at the same frequency and that there will be no drift between their acquisitions. However, oversample clock sharing does not guarantee that the samples on both modules are acquired at exactly the same time. Figure 3 illustrates the oversample pulse trains on two NI 4472s sampling at 102.4 kS/s. In this example, there is a delay between acquisition samples of five oversample intervals, or about 350 ns. This delay may be any value up to a whole sample interval, which is about 10  $\mu\text{s}$  at this acquisition rate.



**Figure 3.** Sample Delay Between NI 4472 Modules After Receiving a Shared Oversample Clock

The solution to the clock-delay issue is to configure the master device to issue a SYNC pulse before the acquisition. The clock master sends a single active-low, or inverted, pulse on the PXI\_Trig5/RTS15 line, the dedicated line for the SYNC pulse. The ADCs in the clock master and clock slaves receive this pulse nearly simultaneously. The SYNC pulse forces all the ADCs to a reset state, emptying their digital filters and synchronizing their clock dividers. After exiting the reset state, all NI 4472 modules in the chassis run at the same frequency and have minimal phase difference between sample clocks. Figure 4 illustrates how this technique minimizes the sample delay.



**Figure 4.** NI 4472 Modules with Shared Oversample Clock Using the SYNC Pulse

The NI 4472 cannot acquire data while it is in the reset state that occurs immediately after it receives the SYNC pulse. During this period, the ADC returns only zeros. The length of the reset period  $T_{\text{reset}}$  (in samples) is a function of sample rate. Table 2 shows the possible lengths of the reset period.

**Table 2.** Reset Period as a Function of Sample Rate

Sample Rate	Reset Period ( $T_{\text{reset}}$ )
$f_s \leq 51.2 \text{ kS/s}$	$T_{\text{reset}} = 8,960 \text{ samples}$
$f_s > 51.2 \text{ kS/s}$	$T_{\text{reset}} = 17,920 \text{ samples}$

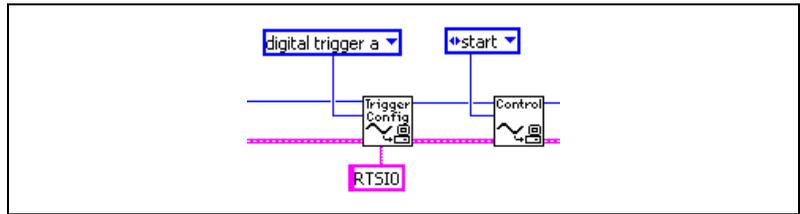
When all NI 4472s are housed in a single chassis, the SYNC pulse is automatically handled by NI-DAQ, the NI driver software for DAQ hardware. Therefore, you do not need to make an explicit software call to generate or route the SYNC pulse. However, you must make specific calls to the NI 6653 modules in all chassis to properly generate and route the SYNC pulse when configuring a multichassis system. These calls are discussed in the [Using the NI 6653 to Route Synchronization Signals Between Multiple Chassis](#) section.

## The Acquisition Start Trigger

After sharing the oversampling clock and issuing the SYNC pulse, the ADCs on every NI 4472 in the system run in lock-step. At this point, the only remaining task is to synchronize the beginning of the data acquisition on each NI 4472.

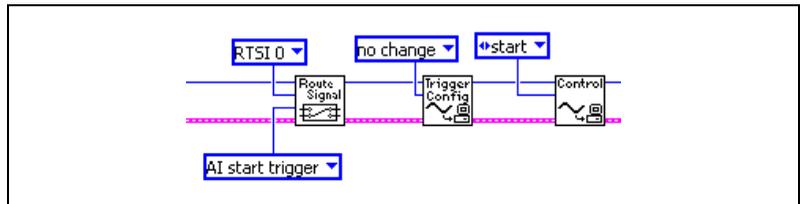
In the [Sharing the Oversample Clock Between Chassis](#) section and the [Sharing the SYNC Pulse Between Chassis](#) section, clock master and clock slave modules were discussed. Because the oversample clock is carried on the PXI star trigger bus, the clock master module must always reside in Slot 2. This concept of master and slave devices is also useful when discussing the acquisition start trigger. Exactly one module should be the “trigger master,” while all the other NI 4472 modules are “trigger slaves.” However, the trigger master can reside in any PXI slot; it is not limited to Slot 2. Therefore, the clock master and trigger master are not necessarily the same module.

First, configure all the trigger slave NI 4472 modules to start their acquisitions on a digital trigger from a PXI\_Trig/RTSI line. You can choose PXI\_Trig<0..4>/RTSI<0..4> for the start trigger; the choice of PXI\_Trig0/RTSI0 line for this example is arbitrary. Figure 5 shows how to wire a trigger cluster to the AI Start VI to accomplish this task.



**Figure 5.** Starting the Acquisition on a Trigger Slave

Next, direct the trigger master to export a pulse to PXI\_Trig0/RTSIO when it begins acquiring. This pulse, in turn, triggers all the slaves. Figure 6 shows the LabVIEW code snippet used to configure the trigger master.



**Figure 6.** Routing the Start Trigger and Starting the Acquisition on the Trigger Master

The code in Figure 6 uses immediate software triggering for the trigger master NI 4472. However, you could easily change the triggering parameters on the trigger master AI Start VI to use external digital or analog triggering.

## Using the NI 6653 to Route Synchronization Signals Between Multiple Chassis

The [Synchronizing Signals for Multiple NI 4472 Modules in a Single Chassis](#) section discussed why the oversample clock, SYNC pulse, and acquisition start trigger are necessary and addressed the software calls needed to share these signals between NI 4472 modules residing in a single PXI chassis. This section explains how the NI 6653 enables you to expand the channel count of your system by sharing these same three signals among multiple chassis.

### Sharing the Oversample Clock Between Chassis

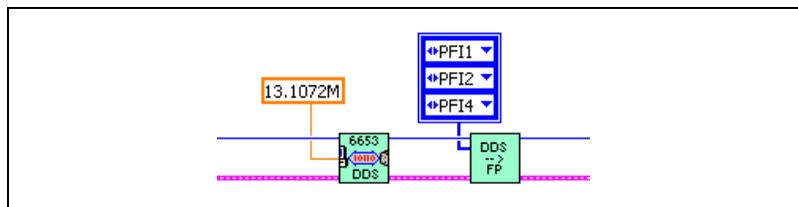
In a single-chassis synchronized DSA system, the clock master NI 4472 generates the oversample clock and distributes it to the clock slave modules. When the DSA system consists of multiple PXI chassis, the NI 6653 in the master chassis generates the oversample clock and distributes it to all the NI 4472 modules. Thus, every DSA device in a multichassis system is a clock slave; you do not define a clock master NI 4472.

First, consider a system with either two or three chassis where each chassis contains an NI 6653 in Slot 2 and several NI 4472 modules. One NI 6653 is defined as the “NI 6653 master.” This module uses its DDS chip to generate the appropriate oversample clock. The NI 6653 master is also responsible for distributing the oversample clock to all the other “slave” chassis. Each NI 6653 (both master and slave) must route the oversample clock to the PXI backplane so that it can drive the ADCs on the NI 4472 modules housed in the chassis. Refer to Figure 16 for an illustration of the hardware setup for this configuration.

In this diagram, the NI 6653 in the top chassis is the master, while the NI 6653 modules in the other two chassis are slaves. The master connects to both slaves. Notice that the master includes one cable that “loops back” to itself. This loopback guarantees that the oversample pulse train travels over a similar path before reaching the PXI star trigger bus on both backplanes. As the pulse travels along the coaxial cable and through the circuitry on the NI 6653, it creates a significant propagation delay. The loopback minimizes this timing difference and ensures symmetry between the paths to the backplane of each chassis.

The code snippet shown in Figure 7 programs the master NI 6653 to generate a frequency of 13.1072 MHz, the oversample frequency corresponding to an NI 4472 sampling rate of either 51.2 kS/s or 102.4 kS/s. The code then routes the signal to three front panel pins: **PFI 1**, **PFI 2**, and **PFI 4**. **PFI 1** is connected to **PFI 0**, while **PFI 2** and **PFI 4** connect to the NI 6653 modules in the second and third chassis, respectively. *PFI* stands for Programmable Function Interface. These pins are discussed in more detail in the *NI 6653 User Manual*.

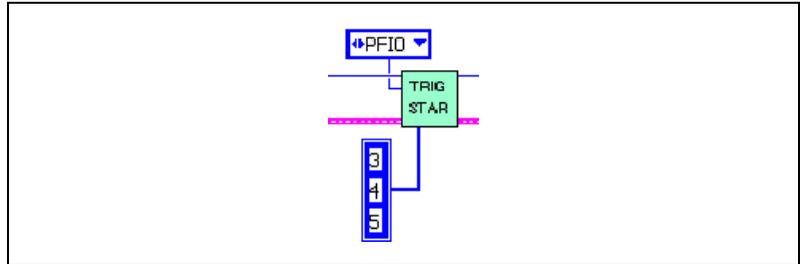
Refer to the *NI PXI-6653 User Manual* for a description of the NI 6653 front panel.



**Figure 7.** Generating and Routing the Oversample Frequency

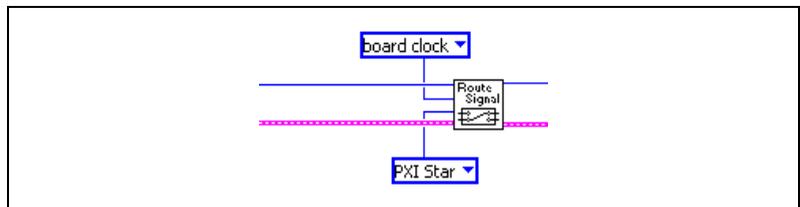
Next, both the master and slave NI 6653 modules must import the oversample clock signal on PFI0 and route it to the appropriate PXI star trigger lines. This routing is an asynchronous operation. *Asynchronous routing* means that the signal follows a short path from the PFI input to the PXI star trigger bus and that the NI 6653 hardware does not actively adjust

the phase or timing of the signal. The code shown in Figure 8 routes the oversample clock from PFIO to NI 4472 boards in Slots 3 through 5.



**Figure 8.** Routing the Oversample Clock Using the PXI Star Trigger Bus

All NI 4472 modules in the system then import this oversample clock from their local PXI star lines. The LabVIEW code snippet used to import the clock is shown in Figure 9.



**Figure 9.** Importing the Oversample Clock from PXI\_Star

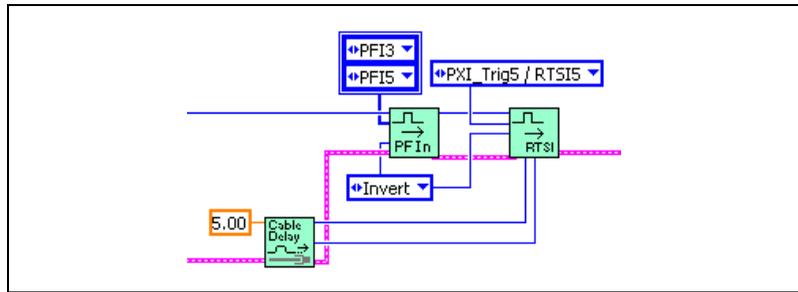
## Sharing the SYNC Pulse Between Chassis

The SYNC pulse is an active-low signal on PXI\_Trig5/RTSI5 that resets the internal clock dividers in the NI 4472 ADCs and minimizes phase mismatch across devices. When all NI 4472 modules are in a single chassis, NI-DAQ automatically handles the SYNC signal. In a multichassis DSA system; however, you must include code to explicitly handle the SYNC pulse using the NI 6653.

The master NI 6653 is responsible for issuing the SYNC. This signal is an active-low pulse, so the NI 4472 ADCs reset when they receive a falling edge on PXI\_Trig5/RTSI5.

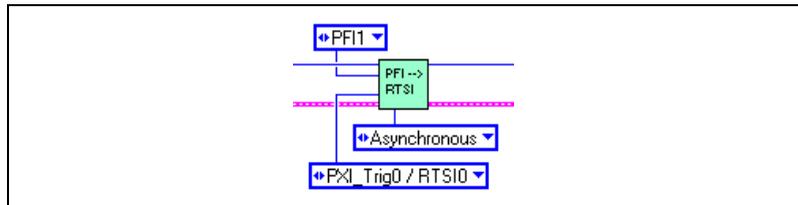
Unlike the oversample clock, all the generation and routing of the SYNC is performed synchronously with the oversample clock. This synchronous routing means that the edges of the SYNC pulse precisely line up with the edges of the oversample clock. Synchronous routing allows the NI 6653 in the master chassis to issue the SYNC directly to PXI\_Trig5/RTSI5 without requiring a loopback scheme like that of the oversample clock. Instead, the master NI 6653 actively delays the pulse based on the cable length between chassis. The code snippet in Figure 10 prepares the master to issue the

SYNC pulse to PFI3 and PFI5 (physically cabled to **PFI 1** on the two slave chassis) and to the local PXI\_Trig5/RTS15 line. The code includes delay on the master to compensate for propagation delay through 5 m of coaxial cable.



**Figure 10.** Compensating for Propagation Delay on the SYNC Pulse

Each slave NI 6653 then routes the incoming SYNC pulse on PFI1 to the PXI\_Trig5/RTS15 line as shown in Figure 11.



**Figure 11.** Routing the SYNC Pulse



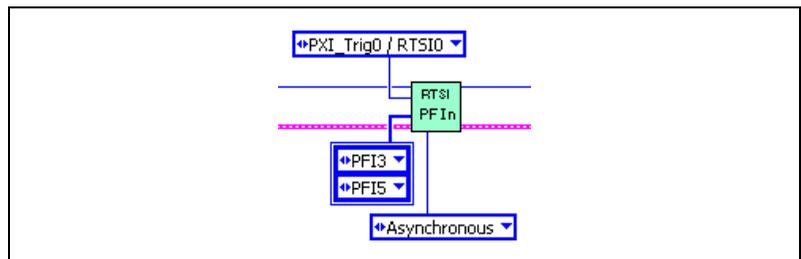
**Note** The previous code snippets illustrate how to set up the routing for the NI 4472 SYNC pulse. They guarantee that when the pulse is generated, it propagates with minimal skew to all the NI 4472 modules in the system. A subsequent subVI that is not shown in the code snippets actually issues the SYNC pulse.

## Sharing the Acquisition Start Trigger Between Chassis

The last signal you must pass between chassis is the start trigger, used to initiate the NI 4472 acquisition. Unlike the oversample clock and the SYNC pulse, the trigger is actually generated by an NI 4472, not by the NI 6653. The trigger master (in this case, the NI 4472 that generates the trigger signal) can be any NI 4472 residing in the master chassis. As with the single-chassis case, this trigger master can initiate a system acquisition based on an immediate software trigger or an external digital or analog trigger.

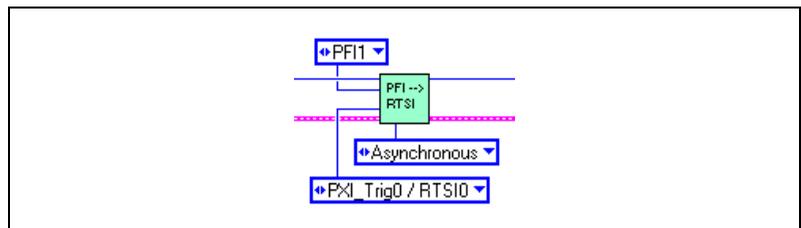
The start trigger signal is passed asynchronously. Asynchronous routing means that there is no compensation for cable propagation time between master and slave chassis. However, the timing requirements for the start trigger are less stringent than those for the SYNC signal. As long as the start trigger arrives within the same sample clock (not oversample clock) interval on each chassis, the acquisition remains tightly synchronized. This interval is 10  $\mu$ s or longer, and signal integrity would become a limiting factor in this synchronization scheme before you could use enough cable for the asynchronous trigger delay to become significant. Thus, start trigger propagation delay will not result in measurement errors over the cable lengths supported by the NI 6653.

As in the single-chassis case, the trigger master NI 4472 exports the start trigger signal to PXI\_Star0/RTSIO (here again, the choice of PXI\_Trig/RTSI line for passing the trigger is arbitrary). This trigger starts the acquisition on all NI 4472s in the master chassis. The NI 6653 in the master chassis is then responsible for asynchronously routing the start trigger from PXI\_Trig0/RTSIO to its front panel pins **PFI 3** and **PFI 5**. These same pins were earlier used to propagate the SYNC pulse. Figure 12 shows the LabVIEW code snippet used to export the start trigger signal.



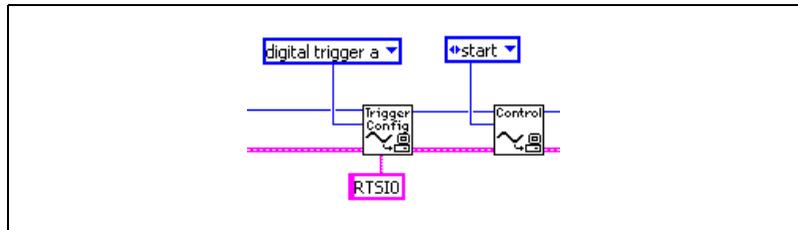
**Figure 12.** Asynchronously Routing the Start Trigger to the PFI Pins

Each slave NI 6653 then routes the incoming pulse on **PFI 1** to PXI\_Trig0/RTSIO. Again, this operation is performed asynchronously. Figure 13 shows the code snippet you need to route the signal.



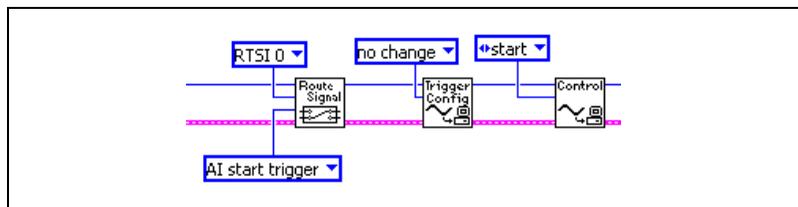
**Figure 13.** Routing the Incoming Start Trigger to RTSIO/PXI\_Trig0

With respect to the acquisition triggering, the NI 4472 modules operate exactly as they do in a single-chassis synchronized system. The slaves digitally trigger from PXI\_Trig0/RTSI0. Figure 14 shows the LabVIEW code snippet that you can use to digitally trigger from PXI\_Trig0/RTSI0.



**Figure 14.** Digital Trigger from RTSI0/PXI\_Trig0 on Trigger Slave

The master exports its start trigger signal to PXI\_Trig0/RTSI0. This operation is shown in Figure 15.



**Figure 15.** Exporting a Start Trigger to RTSI0/PXI\_Trig0 on Trigger Master

In this case, the master starts with an immediate software trigger. However, you could easily modify the parameters for the AI Start VI on the master to enable external digital or analog triggering.

## Installing the Software

The software package that ships with the NI 6653 provides the following items:

- NI 6653 and NI 4472 LabVIEW example code. Three high-level examples are provided to give you a starting point in using the NI 6653 to synchronize data acquisition across multiple PXI chassis. These examples illustrate the following three common use cases:
  - NI 4472s in two or three chassis controlled by one CPU (either an embedded PXI controller or desktop PC connected using a MXI-3 cable)
  - NI 4472s in more than three chassis (up to 48) controlled by one CPU
  - NI 4472s in two chassis, each controlled by its own CPU

- NI 6653 and NI 4472 LabWindows™/CVI™ and MSVC example code. Two high-level examples are provided for LabWindows/CVI and MSVC:
  - NI 4472 modules in two chassis controlled by one CPU (either an embedded PXI controller or desktop PC connected using a MXI-3 cable)
  - NI 4472s in multiple chassis (up to 48) controlled by one CPU

Refer to the `Readme.htm` file on the CD that shipped with the NI 6653 for complete directions on installing the NI 6653 Driver Software package.



**Note** It is important that you install the NI 6653 Driver Software package as well as the NI-DAQ driver (to control the NI 4472 modules) and the NI-VISA driver before you install any of the PXI modules.

## Unpacking

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The NI 6653 is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge can damage several components on the module.



**Caution** *Never* touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by holding a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do *not* install a damaged module into the computer.

Store the NI 6653 in the antistatic package when not in use.

## Installing the PXI Modules

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The following instructions are general installation instructions. The *What You Need to Get Started* section for each configuration provides information about where the modules should be installed.

To install the PXI module, complete the following steps:

1. Power off the PXI chassis.
2. Remove the filler panel for an unused PXI slot.



**Note** The NI 6653 is typically installed in Slot 2. All the examples that ship with the NI 6653 are written assuming the module is installed in Slot 2 and will not work otherwise.

3. Touch a metal part of the chassis to discharge any static electricity.
4. Insert the module into the PXI slot. Use the injector/ejector handle to fully insert the device into the slot.
5. Screw the device front panel to the front panel mounting rail of the chassis.

The PXI module is now installed.

## Verifying the Hardware

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Complete the following steps to install and verify the NI 6653 and NI 4472 hardware:

1. Power off the system and install the hardware as desired.
2. Power on the system.
3. Launch Measurement & Automation Explorer (MAX) after system startup.
4. Expand the tab in MAX labeled **Devices and Interfaces**.
5. You should see one entry under this tab for each NI 4472. Right-click each device and select **Test Panel**. Use the test panel to verify that you can successfully communicate and acquire data with each device.
6. Under **Devices and Interfaces**, you should see entries for one or more PXI buses. MAX should display one entry for each PXI chassis or bus segment that contains one or more NI 6653 modules. Expand each bus tab to view the individual entries for the NI 6653 modules. Write down the NI-VISA descriptors for all NI 6653 modules in the system.
7. Determine the physical location of each NI 6653 in your system. The physical location refers to the PXI chassis and slot number. MAX should recognize each NI 6653 and give you a VISA Instrument Descriptor of the form **PXI<sub>n</sub>PCI Bus : : n<sub>PCI Device</sub> : : INSTR**. MAX does not explicitly list the chassis and slot locations for these devices. However, the following guidelines instruct you on how to map each instrument descriptor for the NI 6653 to a physical instrument location.
  - Devices in the PCI bus segment closest to the CPU (whether an embedded PXI Controller or a desktop connected with a MXI-3

cable) have the lowest bus number. In all PXI chassis except the NI PXI-1006, there is only one bus segment per chassis. Thus, each module in these chassis has the same value for  $n_{\text{PCI Bus}}$ . The PXI-1006 chassis has three bus segments, increasing in bus number from left to right. In a system with a PXI controller, the first bus segment is usually numbered 0. In a MXI-3 system, it has a higher number, usually 1 or 2.

- Within a particular bus segment, the values for  $n_{\text{PCI Device}}$  decrease from left to right. Given these two rules, it is straightforward to map every NI 6653 instrument descriptor, the combination of  $n_{\text{PCI Device}}$  and  $n_{\text{PCI Bus}}$ , to a physical chassis and slot location.

The following steps walk through how to determine the instrument locations of the devices in your system.

- The first step is to locate the instrument descriptor with the lowest value for  $n_{\text{PCI Bus}}$ . If multiple devices have the same (and lowest) value for  $n_{\text{PCI Bus}}$ , select the one with the greatest value for  $n_{\text{PCI Device}}$ . This device is closest to the CPU. If the system includes MXI-3 and a desktop, this device is in the leftmost slot in the chassis that is connected directly to the computer.
- Next, map any instrument descriptors that are in the same bus segment. Notice that the device numbers decrease by one with each additional slot to the right.
- Finally, continue mapping any NI 6653 modules in additional bus segments. In general, you should not have more than one NI 6653 per chassis with the possible exception of the first chassis.

Table 3 provides an example for using VISA instrument descriptors to derive the physical location for all NI 6653 modules in the system. This example is based on a system with four NI PXI-1006 chassis controlled by a MXI-3 linked desktop.

**Table 3.** Example Configuration: Four-Chassis System Controlled by a MXI-3-Linked Desktop

Chassis Number	Chassis Type	MXI-3 Connections	NI 6653 Locations
First chassis	NI PXI-1006	CPU (Desktop PC), second chassis	Slot 2 Slot 3
Second chassis	NI PXI-1006	first chassis, third chassis	Slot 2
Third chassis	NI PXI-1006	second chassis, fourth chassis	Slot 2
Fourth chassis	NI PXI-1006	third chassis	Slot 2

MAX shows the following instrument descriptors for the five NI 6653 modules in the system:

- **PXI2::14::INSTR**
- **PXI2::15::INSTR**
- **PXI5::15::INSTR**
- **PXI8::15::INSTR**
- **PXI11::15::INSTR**

The following steps show how the instrument mapping scheme would apply to this example.

- a. First, locate the descriptor with the lowest bus number and greatest device number—**PXI2::15::INSTR**. This descriptor must map to the leftmost device in the chassis connected to the PC. This is the Slot 2 board in the first chassis.
- b. Next, locate any other modules with the same bus number. This example returns only one—**PXI2::14::INSTR**. Thus, this module must be in Slot 3, the one directly to the right of Slot 2.
- c. Now consider the next smallest bus number. In this case, the next smallest bus value is 5, and the instrument descriptor is **PXI5::15::INSTR**. This descriptor refers to the module in Slot 2 of the second chassis. Because the first chassis is an NI PXI-1006, there are actually *three* bus segments separating this module from the previous two. Thus, the bus number in this segment (5) differs from the bus number from the previous two modules (2) by 3.

Similarly, you can map the remaining descriptors, **PXI8::15::INSTR** and **PXI11::15::INSTR**, to the NI 6653 modules in Slot 2 of the third and fourth chassis, respectively.

Table 4 shows the instrument descriptor map for the system.

**Table 4.** Instrument Descriptor Map for Four-Chassis, MXI-3 Linked Example

<b>Physical Location of NI 6653</b>	<b>Instrument Descriptor</b>
Slot 2 in First Chassis	PXI2::15::INSTR
Slot 3 in First Chassis	PXI2::14::INSTR
Slot 2 in Second Chassis	PXI5::15::INSTR
Slot 2 in Third Chassis	PXI8::15::INSTR
Slot 2 in Fourth Chassis	PXI11::15::INSTR



**Tip** Understanding this relationship ensures that you can enter the correct instrument descriptors to describe the master and slave NI 6653 modules in your software.

# Configuring the Chassis

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The following sections provide information for configuring the hardware for three use cases:

- [Configuration #1: Two or Three Chassis with Synchronized Acquisition and One CPU](#)
- [Configuration #2: Four or More Chassis with Synchronized Acquisition and One CPU](#)
- [Configuration #3: Two Chassis with Synchronized Acquisition and Two CPUs](#)

Determine which of these configurations you will use, and refer to that section for more information.



**Note** The following system configurations use 1 m SMB-SMB cables for sharing clock and trigger signals between chassis. You can use longer cables if desired; refer to the *NI 6653 User Manual* for the maximum cable length specifications. However, to attain the tightest possible synchronization, it is important that you maintain equal length for all cables in the system and compensate for cable propagation delays in your software.

## Configuration #1: Two or Three Chassis with Synchronized Acquisition and One CPU

This configuration enables synchronization between NI 4472 modules housed in two or three PXI chassis. It assumes that only one CPU controls the acquisition. The CPU can be either a desktop PCI machine with a MXI-3 link or an embedded PXI controller in the master chassis.

LabVIEW, LabWindows/CVI, and MSVC example programs are provided for this configuration. The LabVIEW example supports either two or three chassis. The LabWindows/CVI and MSVC examples support only two chassis.

### What You Need to Get Started

To set up and use Configuration #1, you need the following items:

- Two or three PXI chassis



**Note** The chassis containing either the embedded controller or the desktop MXI-3 link is referred to as Chassis #1. The other chassis are referred to as Chassis #2 and Chassis #3 (if a third chassis is present). In the remainder of this section, the number of chassis present is called  $N$ .

CPU

The CPU can be an embedded PXI controller running Windows 2000/XP, or it can be a desktop computer running Windows 2000/XP with an installed PCI-to-PXI MXI-3 kit. Either a copper or fiber-optic MXI-3 connection can be used for the desktop-based solution. The controller or MXI-3 link should be installed in Slot 1 of Chassis #1.

One NI 6653 per PXI chassis

Install one NI 6653 in Slot 2 of each chassis.

One or more NI 4472 per PXI chassis

Place the NI 4472 modules in any available PXI slot that is numbered 3 to 15.



**Note** Do *not* install the NI 4472 in Slots 16, 17, or 18 of the NI PXI-1006 chassis. You cannot route the oversample clock to those slots.

( $N - 1$ ) SMB-210 cables

One 1-meter SMB-200 cable

( $N - 1$ ) PXI-to-PXI MXI-3 kits

You should install a MXI-3 PXI module in Slot 1 of Chassis #2 (and Chassis #3, in a three-chassis system). Either fiber-optic or copper MXI-3 connections may be used.

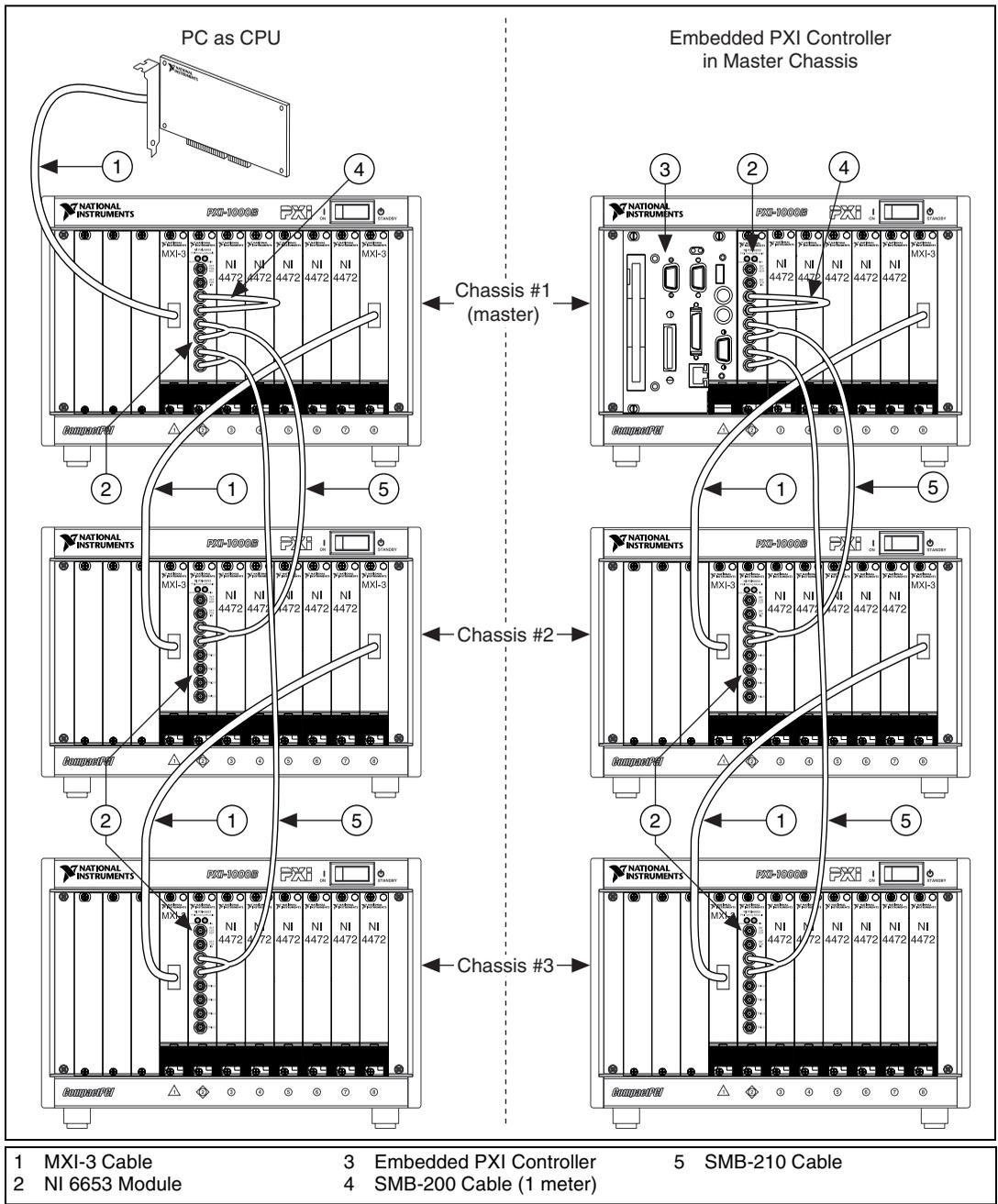
You should also install MXI-3 PXI modules in any available slot, *except* Slot 2, of Chassis #1 (and Chassis #2), with Slot 8 being the designated slot throughout this document.

One 1 kHz sine source (function generator), for testing phase match between chassis.



**Note** The function generator is not required, but it is highly recommended for testing purposes.

Refer to Figure 16 for an illustration of the two configurations for a three-chassis synchronized acquisition using the NI 6653 and the NI 4472.



**Figure 16.** Three Chassis with Synchronized Acquisition (with either a PC or an Embedded PXI Controller)

## Connecting the MXI-3 Devices

Referring to Figure 16, complete the following steps to connect the MXI-3 devices:

1. If you are using a desktop computer, install a MXI-3 cable to connect the PCI MXI-3 device to the PXI MXI-3 module in Slot 1 of Chassis #1.
  2. Connect the MXI-3 module in Slot 1 of Chassis #2 to the MXI-3 module in Slot 8 of Chassis #1.
- ◆ Three-chassis system only
3. Connect the MXI-3 module in Slot 1 of Chassis #3 to the MXI-3 device in Slot 8 of Chassis #2.

Refer to the *Set Up Your PXI-MXI-3 System* document, which is included with the MXI-3 kit or available for download from [ni.com/manuals](http://ni.com/manuals), for further details.

## Connecting the NI 6653 Devices

1. Use an SMB-200 cable to connect **PFI 0** to **PFI 1** on the NI 6653 of Chassis #1. This cable loops back to connect two external pins on the same device.
  2. Use an SMB-210 cable to connect **PFI 2** and **PFI 3** on Chassis #1 to **PFI 0** and **PFI 1** of Chassis #2, respectively.
- ◆ Three-chassis system only
3. Use an SMB-210 cable to connect **PFI 4** and **PFI 5** of Chassis #1 to **PFI 0** and **PFI 1** of Chassis #3, respectively.

## Connecting the NI 4472 Devices

Connect the external sine signal to a single input channel on one NI 4472 in each chassis. The same signal should be fed to each chassis to measure the phase mismatch and to verify that the synchronization is within specifications. The synchronization is configured and verified in the *Configuring and Running the Software Example* section.

## Configuring and Running the Software Example

1. After the hardware has been configured, launch MAX. Verify that all NI 4472 modules are recognized and properly functioning and that the NI 6653 modules are recognized.
2. Refer to the Instrument Descriptor Map from step 7 of the [Verifying the Hardware](#) section.

3. Refer to the *Running the Example Programs* section of the `readme.htm` file for information on launching the example code.
4. Examine the output of the software to verify synchronization between chassis. The phase mismatch between any two channels in the system should be less than 0.1 degree for a 1 kHz input signal.

## Configuration #2: Four or More Chassis with Synchronized Acquisition and One CPU

This configuration enables synchronization between NI 4472 modules housed in four or more PXI chassis. Like the previous configuration, this configuration assumes that only one CPU controls the acquisition, so there is no separate embedded PXI controller for each chassis. This CPU may be either a desktop PCI machine with a MXI-3 link or an embedded PXI controller.

LabVIEW, LabWindows/CVI, and MSVC examples are provided for this configuration.

### What You Need to Get Started

To set up and use Configuration #2, you need the following items:

- Four or more PXI chassis



**Note** The chassis containing either the embedded controller or the desktop MXI-3 link is referred to as Chassis #1. The other chassis are referred to as Chassis #2 through Chassis #*N*. In the remainder of the section, the number of chassis present is called *N*.

- CPU

The CPU can be an embedded PXI controller running Windows 2000/XP or a desktop computer running Windows 2000/XP with a PCI-to-PXI MXI-3 kit. Use either a copper or a fiber-optic MXI-3 connection for the desktop-based solution. Install the controller or MXI-3 link in Slot 1 of Chassis #1.

- Several NI 6653 modules

You will need one module per chassis, plus an additional module for every three chassis after the first three chassis. Table 5 shows the relationship between chassis and modules.

**Table 5.** Number of Chassis and Required Number of NI 6653 Modules

Number of PXI Chassis	Number of NI 6653 Required
4	5
5	6
6	7
7	9
10	13

Install one NI 6653 in Slot 2 of each chassis. Install the remaining NI 6653 modules in the leftmost available slots in the first chassis (Slot 3, Slot 4, and so on).

- One or more NI 4472 modules per chassis

Place the NI 4472 modules in any of the available PXI Slots numbered 3 through 15.



**Note** Do *not* install the NI 4472 in Slots 16, 17, or 18 of the NI PXI-1006 chassis. You cannot route the oversample clock to those slots.

- $(N - 1)$  SMB-210 cables
- One 1-meter SMB-200 cable
- $(N - 1)$  PXI-to-PXI MXI-3 kits

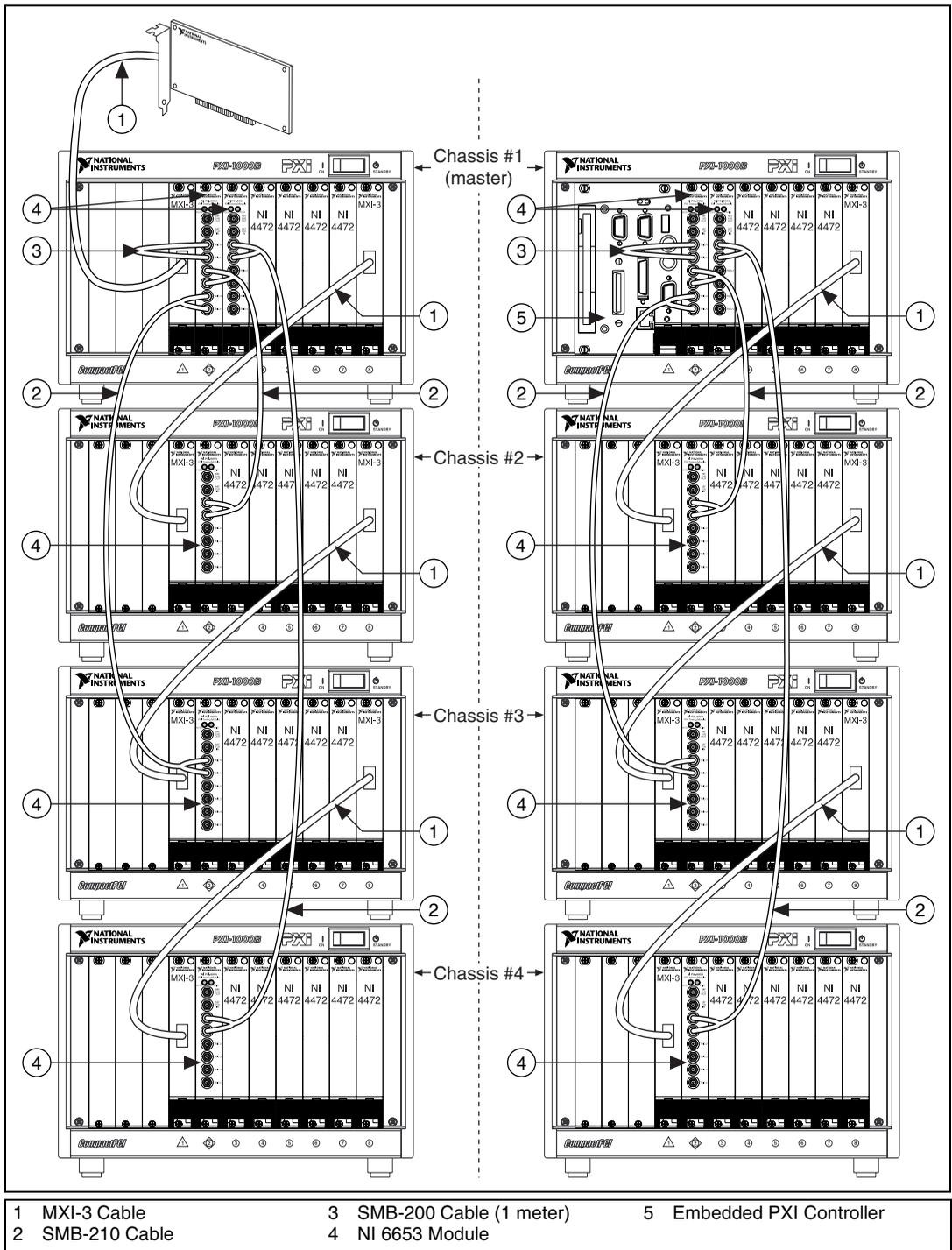
Install a MXI-3 PXI device in Slot 1 of each chassis except for Chassis #1. Then install a MXI-3 PXI device in any available slot of Chassis #1 through Chassis  $(N - 1)$ . This slot is designated as Slot 8 for the remainder of this document.

- One 1 kHz sine source (function generator), for testing phase mismatch between chassis



**Note** The function generator is not required, but it is highly recommended for testing purposes.

Refer to Figure 17 for an illustration of the two configurations for a four-chassis synchronized acquisition using the NI 6653 and the NI 4472.



**Figure 17. Four Chassis with Synchronized Acquisition**

## Connecting the MXI-3 Devices

Referring to Figure 17, complete the following steps to connect the MXI-3 devices:

1. If you are using a desktop computer, use a MXI-3 cable to connect the PCI MXI-3 device to the PXI MXI-3 module in Slot 1 of Chassis #1.
2. Connect the MXI-3 module in Slot 8 of Chassis #1 to MXI-3 module in Slot 1 of Chassis #2.
3. Daisy-chain all remaining chassis. Start by connecting the MXI-3 module in Slot 8 of Chassis #2 to the MXI-3 module in Slot 1 of Chassis #3. Continue until each chassis is connected with a MXI-3 cable to Slot 1 of the next chassis.

Refer to the *Set Up Your PXI-MXI-3 System* document, which is included with the MXI-3 kit or available for download from [ni.com/manuals](http://ni.com/manuals), for further details.

## Connecting the NI 6653

1. Use an SMB-200 cable to connect **PF10** to **PF11** on the NI 6653 in Slot 2 of Chassis #1. This cable “loops back” to connect two external pins on the same device.
  2. Use an SMB-210 cable to connect **PF12** and **PF13** on the NI 6653 in Slot 2 of Chassis #1 to **PF10** and **PF11** of Chassis #2, respectively.
  3. Use an SMB-210 cable to connect **PF14** and **PF15** on the NI 6653 in Slot 2 of Chassis #1 to **PF10** and **PF11** on Chassis #3, respectively.
  4. Use an SMB-210 cable to connect **PF10** and **PF11** on the NI 6653 in Slot 3 of Chassis #1 to **PF10** and **PF11** of Chassis #4, respectively.
  5. Follow the instruction that applies to your system:
- ◆ Five or more chassis system only  
Use an SMB-210 cable to connect **PF12** and **PF13** on the NI 6653 in Slot 3 of Chassis #1 to **PF10** and **PF11** of Chassis #5, respectively.
  - ◆ Six or more chassis system only  
Use an SMB-210 cable to connect **PF14** and **PF15** on the NI 6653 in Slot 3 of Chassis #1 to **PF10** and **PF11** of Chassis #6, respectively.
  - ◆ Seven or more chassis system only  
A seven-chassis system requires three NI 6653 modules in the first chassis. The previous steps have detailed all cable connections for the first two NI 6653 modules in the master. The connections for the third NI 6653 in the master chassis are identical to those for the second, except that they pertain to an additional one to three slave chassis. This

configuration can be extended for up to 16 NI 6653 modules in the master chassis, yielding a potential maximum of 48 chassis containing NI 4472 modules.

## Connecting the NI 4472 Devices

Connect the external sine signal to a single input channel on one NI 4472 in each chassis. The same signal should be fed to each chassis to measure the phase mismatch and to verify that the synchronization is within specifications. In the *Configuring and Running the Software Example* section, synchronization is configured and verified.

## Configuring and Running the Software Example

1. After the hardware has been configured, launch MAX. Verify that all NI 4472 modules are recognized and functioning properly and that the NI 6653 modules are recognized.
2. Refer to the *Running the Example Programs* section of the `readme.htm` file for information on launching the example code.
3. Examine the output of the software to verify synchronization between chassis. The phase mismatch between any two channels in the system should be less than 0.1 degree for a 1 kHz input signal.

## Configuration #3: Two Chassis with Synchronized Acquisition and Two CPUs

This configuration enables synchronization between NI 4472 modules housed in two PXI chassis. It assumes that each PXI chassis is equipped with its own CPU. The same software can be used with two separate desktop PCs, each controlling a single chassis using MXI-3 instead of embedded PXI controllers.

LabVIEW examples are provided for this configuration.

## What You Need to Get Started

To set up and use Configuration #3, you need the following items:

- Two PXI chassis
- CPUs

Each PXI chassis should contain an embedded PXI controller running Windows 2000/XP. Alternately, two MXI-3-linked desktop PCs running Windows 2000/XP could control the two chassis.

- Two NI 6653 modules  
Install one NI 6653 in Slot 2 of each chassis.
- One or more NI 4472 modules per chassis  
Place the NI 4472 modules in any of the available PXI Slots numbered 3 through 15.



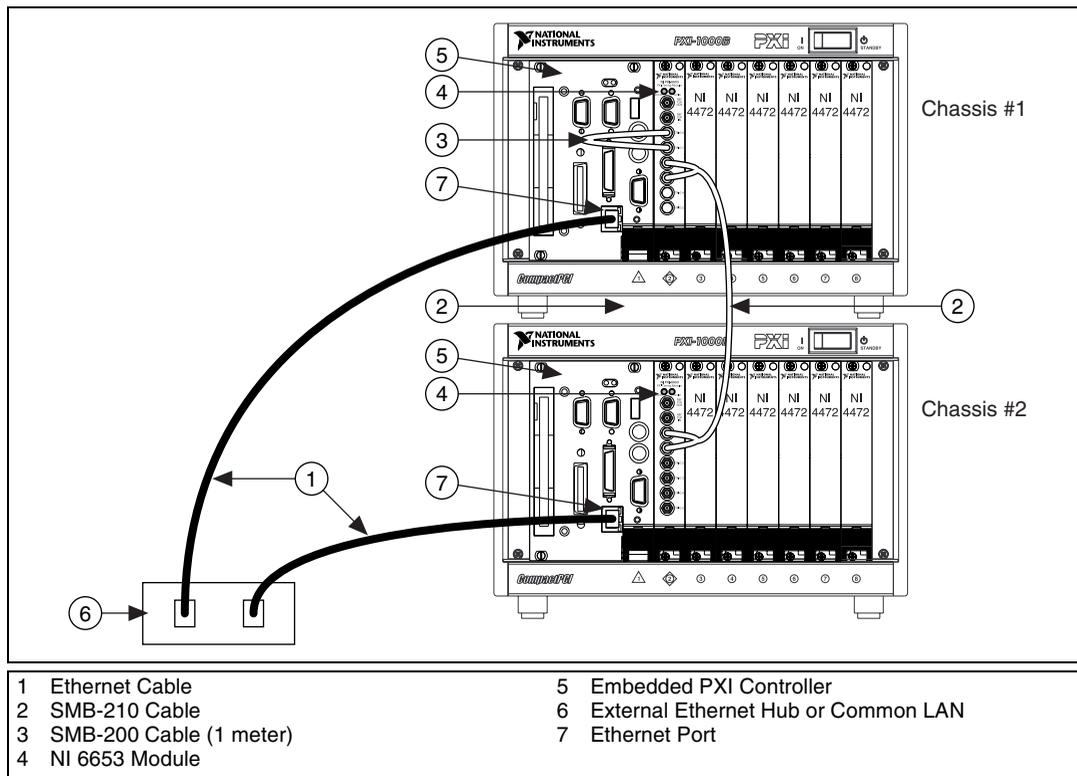
**Note** Do *not* install the NI 4472 in Slots 16, 17, or 18 of the NI PXI-1006 chassis. You cannot route the oversample clock to those slots.

- Two Ethernet ports  
If the PXI controllers or desktop PCs contain embedded Ethernet ports, these can be used without additional hardware. If you have controllers that do not contain built-in ports, such as the NI PXI-8170, install a PXI Ethernet card, such as the NI PXI-8211, in an available slot in each chassis.
- External Ethernet hub or common LAN  
You can use any setup that allows each chassis to communicate with the other chassis over the Ethernet.
- Two Ethernet cables
- One SMB-210 cable
- One 1-meter SMB-200 cable
- One 1 kHz sine source (function generator) for testing phase mismatch between chassis



**Note** The function generator is not required, but it is highly recommended for testing purposes.

Refer to Figure 18 for an illustration of the hardware configuration for two synchronized chassis, each controlled by its own CPU.



**Figure 18.** Two Chassis with Synchronized Acquisition and Separate CPUs (Embedded PXI Controllers)

## Connecting to Ethernet

All chassis should be connected to a common LAN or Ethernet hub.

## Connecting the NI 6653

1. Use a 1-meter SMB-200 cable to connect **PF10** to **PF11** on the NI 6653 in Slot 2 of Chassis #1. This cable connects two external pins on the same module.
2. Use an SMB-210 cable to connect **PF12** and **PF13** on the NI 6653 in Slot 2 of Chassis #1 to **PF10** and **PF11** of Chassis #2, respectively.

## Connecting the NI 4472 Modules

Connect the external sine signal to a single input channel on one NI 4472 in each chassis. The same signal should be fed to each chassis to measure the phase mismatch and verify that the synchronization is within specifications. The [Configuring and Running the Software Example](#) section describes the procedure to configure and verify synchronization.

## Configuring and Running the Software Example

1. After the hardware has been configured, launch MAX. Verify that all the NI 4472 modules in the first chassis are recognized and properly functioning and that the NI 6653 modules are recognized. Repeat this procedure for the second chassis.
2. Check that each controller can recognize and communicate with the others over the Ethernet.
3. Refer to the *Running the Example Programs* section of the `readme.htm` file for information on launching the example code.
4. Examine the output of the software to verify synchronization between chassis. The phase mismatch between any two channels in the system should be less than 0.1 degree for a 1 kHz input signal.

## Technical Support Resources

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### NI Web Support

National Instruments Web support is your first stop for help in solving installation, configuration, and application problems and questions. Online problem-solving and diagnostic resources include frequently asked questions, knowledge bases, product-specific troubleshooting wizards, manuals, drivers, software updates, and more. Web support is available through the Technical Support section of [ni.com](http://ni.com).

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### Worldwide Support

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If you have searched the technical support resources on our Web site and still cannot find the answers you need, contact your local office or National Instruments corporate. For telephone support in the United States, dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 61 2 9672 8846, Austria 43 0 662 45 79 90 0,  
Belgium 32 0 2 757 00 20, Brazil 55 11 3262 3599,  
Canada (Calgary) 403 274 9391, Canada (Montreal) 514 288 5722,  
Canada (Ottawa) 613 233 5949, Canada (Québec) 514 694 8521,  
Canada (Toronto) 905 785 0085, Canada (Vancouver) 514 685 7530,  
China 86 21 6555 7838, Czech Republic 42 02 2423 5774,  
Denmark 45 45 76 26 00, Finland 385 0 9 725 725 11,  
France 33 0 1 48 14 24 24, Germany 49 0 89 741 31 30,  
Greece 30 2 10 42 96 427, Hong Kong 2645 3186, India 91 80 4190000,  
Israel 972 0 3 6393737, Italy 39 02 413091, Japan 81 3 5472 2970,  
Korea 82 02 3451 3400, Malaysia 603 9059 6711,  
Mexico 001 800 010 0793, Netherlands 31 0 348 433 466,  
New Zealand 64 09 914 0488, Norway 47 0 32 27 73 00,  
Poland 48 0 22 3390 150, Portugal 351 210 311 210,  
Russia 7 095 238 7139, Singapore 65 6 226 5886,  
Slovenia 386 3 425 4200, South Africa 27 0 11 805 8197,  
Spain 34 91 640 0085, Sweden 46 0 8 587 895 00,  
Switzerland 41 56 200 51 51, Taiwan 886 2 2528 7227,  
United Kingdom 44 0 1635 523545