A PROGRAMMABLE CALIBRATING PULSE GENERATOR WITH MULTI-OUTPUTS AND VERY HIGH STABILITY

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Abstract- We present a very precise and stable pulse generator to be used for the calibration of an array of large mass bolometric detectors. The realized instrument is characterized by the presence of multi-outputs and is completely programmable in pulse width and amplitude. Triggering is allowed with a dedicated line. Although featuring ppm/OC stability, it was realized exploiting commercial devices, obtaining a very cheap solution.

I. INTRODUCTION

The first step towards the realization of the 1000 channels experiment CUORE (Cryogenic Underground Observatory for Rare Events) is starting. It consists of 62 large mass TeO$_2$ bolometric crystals, 790 g each [1]. The intention of the experiment is to study the neutrino-less double beta decay of $^{130}$Te contained as an isotope in the TeO$_2$ [2].

A bolometric crystal converts the energy released by the impinging particle in a temperature increase, that is readout by a thermistor glued on it. The developed signal is very slow, having a few Hz bandwidth, but at the same time the expected signal rate is very low, a few tens of mHz.

Bolometers are very resolving detectors [3], [4]. Our devices show an energy resolution that spread from 6 eVFWHM to 12 eV FWHM per gram of mass at 2.5 MeV of particle energy.

The experiment we are going to start must take data for at least two years. The stability of the energy conversion gain is of great importance. To calibrate, and maintain calibration with time of the whole array, a source of energetic particle cannot be left close to the measurement apparatus, for not increase the radioactive background. This asks for an alternative calibration supporting method to perform this action. The solution we have adopted is the injection of a small and short pulse of power across a small heating resistor glued on each crystal. The responsibility for the accuracy, precision and stability of the whole apparatus is of the heating resistor, for which we defer its description to [5], and to the pulse generator. The instrument we are presenting, although very stable, is obviously not an absolute reference and a periodical use of a source of particle should anyway be needed to re-calibrate the system.

In this paper we describe the solution adopted in the realization of a very stable, multi-channel outputs, reference, pulse generator. Results obtained will be shown in detail.

II. CALIBRATION PULSE GENERATOR SPECIFICATIONS AND PRINCIPLE OF OPERATION

The detector array is composed of a tower having 16 floors. On each floor 4 detector crystals are allocated. The heating resistors of every crystal that stay on a floor are all connected in parallel.

It is foreseen to send calibration signals in sequence, one floor at a time. The amplitude of the signal must be selectable to be able to calibrate each detector on its full dynamic range.

The acquisition system must decide when and to which floor to send the signals. The amplitude of the signal sent is also read back by the acquisition system. The ratio of the signal read at the output of the detector’s front-end, second stage and acquisition system chain and the signal sent is free or highly immune from any drift of any part of the chain.

The calibration signal is a square pulse having a width much shorter than the detector signal. For the detectors of CUORE the range is between 500 µsec and a few msec. The bolometers are sensitive to the energy developed across the heating resistor. The parameter of interest is the quantity $E_G = \frac{V_G^2}{t_W} R_H$ (µV), where $V_G$ is the pulse amplitude and $t_W$ its width. $E_G$ is an energy referred to 1 Ω. The heaters glued on each detector have resistance value ranging from about 50 KΩ to 100 KΩ. The calibrating signal should satisfy:

$$V_G = \sqrt{1.6 \times 10^{−19} \frac{R_H}{t_W} U_C(eV)};$$

where $R_H$ is the resistance of the heater, $U_C$ the wanted calibrating energy expressed in eV, and $(1-1/\alpha)$ a parameter that accounts for any amount of the given energy lost because of the thermal conductive path towards the heat sink due to the connecting wires. As an example considering an $\alpha$ factor of about 5, $R_H$ 100 KΩ and $t_W$ 1 msec, $V_G$ should range from 2.8 mV to 9 mV for energy calibration pulses from 100 KeV to 1 MeV.

The schematic that illustrates the principle of operation of the pulse generator is very simple and it is shown in Fig. 1. The concept is to deliver a voltage of a precise buffered
reference to the heater, when needed. The analog switch SW is used to absolve this task: by closing it for the required amount of time it allows energizing the heater. The schematic of the solution adopted minimizes as much as possible any drift or error that can be added to the system. The reference voltage is a commercial device that, as a standard characteristic, needs to be buffered for driving any kind of load. In our case the buffer gain $\beta$ is selectable, as explained in the following sections. To avoid any error due to the possible change with temperature in rise time or slew rate of the buffer itself, SW is used in such a way that the buffer output voltage remains constant and must only deliver the needed current when the system is fired. The only question to debate is the possible effect that can be induced by the charge injection of the switch with respect to the buffer capability. This problem and solution will be addressed in the following sections.

**III. SCHEMATIC OF THE CALIBRATING PULSE GENERATOR**

The pulse generator, Fig. 2, is split into two parts, according to the system requirements. The detector array is inside a refrigerator that is surrounded by a Faraday cage. The circuitry that generates the analog pulses, the analog-mixed boards of Fig. 2, is in a rack located on the top of the refrigerator, inside the Faraday cage. The ‘analog-mixed boards’ have a slow clock that is idle when not addressed. The main precise 10 MHz clock used to determine the pulse durations is always running for maintaining maximum stability. For this reason it is put outside the Faraday cage to minimize EMI interference. The ‘Analog-mixed boards’ communicate with both the oscillator card and the computer via two optical links.

In the following sub-sections we will describe in detail each of the blocks that compose the system of Fig. 2.

Let’s start to describe the ‘Analog-mixed boards’. Each of them are laid-out on a four layers Printed Circuit Board that measures $100 \times 220 \text{ mm}^2$ (standard Eurocard).

The general schematic of any realized ‘Analog-mixed board’, the core of the pulse generator, is shown in Fig. 3. The block ‘V-ref generator’ contains the voltage reference, a heavily low pass noise suppressor filter, and a buffer amplifier. Between this block and the output stage there is the ‘Amplitude selector’ block that allows attenuating the reference level to the wanted amplitude. This block determines the coefficient $\beta$ of Fig. 1. Every ‘Output stage’ block of Fig. 3 includes a switch SW of Fig. 1 and some additional circuit elements. Each ‘analog-mixed board’ has 4 ‘Output stages’ to serve 4 heaters. To feed the whole array 4 of such boards are therefore needed. A ‘Thermal compensation’ section is included for a fine adjustment of the

![Fig. 1: Very simplified schematic showing the principle of operation of the pulse generator.](image)

![Fig. 2: Complete schematic diagram of the pulse generator system.](image)

![Fig. 3: Complete schematic of the analog-mixed board. The clock generator is remote and communication is via optical fiber link.](image)
overall drift.

The ‘Selector’ block allows the acquisition system to read back some selected node voltages of the circuit.

A Complex Programmable Logic Device, CPLD, regulates the functional behavior of the board. It communicates with the computer via a fiber optic synchronic serial bus, buffered by the Digital trans/receiver block. From the computer it receives the commands to determine the pulse amplitude, the pulse width and which output to fire. The triggering of the signal is also generated by the CPLD after the external Clock signal is switched on.

Let’s explode now in more detail the main blocks.

A. The V-ref generator

The ‘V-ref generator’ is shown in Fig. 4. The Voltage reference is the 5 V generated by the LT1027 (Linear Technology). A heavy low pass filter, Rf-Cf, is connected at its output to attenuate the noise. Rf and Cf have been chosen to maintain completely negligible any possible effect of the leakage current of Cf.

The Operational Amplifier, OA, A1 TLE2071, buffers the output voltage.

The Trim input pin of the LT1027 is exploited to add a voltage Proportional to the Absolute Temperature, PTAT, of an amount dependent on the selection of resistors R1 and R2, on the basis of the voltage applied to the node A. Resistors R3 and R4 are fixed at the value of 5.1 KΩ. The PTAT voltage allows to compensate the thermal drift of this block, specified to be about ±2 ppm/°C (typical), and the following circuit elements, as will be illustrated in sub-section III. D.

![Fig. 4: Circuit schematic of the ‘V-ref generator’ block of Fig. 3.](image)

B. The Amplitude selector

The ‘Amplitude selector’ block circuit diagram is shown in Fig. 5. It consists of a very precise low drift R-2R Digital to Analog Converter, DAC, AD7545A from Analog Devices. The DAC input reference voltage is the output node A of Fig. 4. This DAC is not buffered internally, so we added the OA A2 to perform this action. The necessary feedback resistors for the inverting configuration of A2 are provided by the DAC itself. We have indicated the equivalent schematic of the DAC. Resistor RF is fully matched with any resistor combination RA, RB, that changes for every setting of the DAC. The resulted specified overall typical thermal drift is ±2 ppm/°C.

The output of A2 is inverted by A3 to have positive polarity at the output C, as required. Resistor RC and capacitance Cc add a small compensation to the buffering action of A3. The 2 inputs Bt and Ct allow to set an appropriate PTAT voltage for correcting the drift of the OAs A2 and A3, both part of a dual OP270 by Analog Devices.

![Fig. 5: Circuit schematic of the ‘Amplitude selector’ block of Fig. 3.](image)

C. Output stage

The ‘Output stage’ circuit is shown in Fig. 6. It consists of a resistive attenuating network that reduces the signal present at the input node C, connected to the corresponding output node C of Fig. 5, to the fraction required to produce across the heater resistor the needed calibrating power. Three different attenuation levels are selectable remotely by analog switches Atten.1 to Atten.3, ADG452 (Analog Devices). Whatever is the output selected, the output impedance is in any case close to 150 Ω. This attenuator is realized by using very stable and precise resistances [6] and has less than 1 ppm/°C drift, see following sub-section III. D.

In this stage the output pulse is created. In normal condition of operation switch Gnd is closed, switch Signal is open, and one of the switches Atten.i is closed. Therefore the output is at ground potential. This connection to ground is realized only with passive components, avoiding the presence of any possible DC offset. This condition is a very stringent requirement as any DC offset would generate a constant heat injection that should increase the detector temperature. Furthermore this solution allows a great suppression of cross-talk from any other, eventually, fired output.

If a pulse is to be given, the CPLD opens promptly the switch Gnd and closes the switch Signal of Fig. 6, for the amount of time, tw, needed to create the pulse. The output
node C of Fig. 5 is then connected to the OUT node of the 'Output stage' via the resistive attenuator, to feed the heater resistor at the appropriate voltage level. As soon as the pulse duration, \( t_W \), is finished the CPLD opens again the switch Signal and closes the switch Gnd to ground.

The analog switches Gnd and Signal work in anti-phase, minimizing any injection across \( R_{a1} \). Capacitance \( C_f \) is also added to filter any possible residual glitch. The output rise and fall time of the signal pulse are limited to about 900 nsec. An important consideration concerns the switch Signal, since its on-resistance may add a non-negligible drift. The analog switches used are the ADG452. Four switches are accommodated on a single integrated circuit. The on-resistance of any of these switches is about 6 \( \Omega \) at the supply voltage adopted (0, +10 V), and has a drift of about 3500 ppm/°C. The switch Signal has been actually implemented by putting the four switches of one ADG452 in parallel, obtaining the final value of 1.5 \( \Omega \). At first approximation the contribution to the drift coming from Signal is proportional to the ratio of its on-resistance and the output resistance \( R_{a1} \), 20 K\( \Omega \). The maximum effect to the output drift coming from the realized combination is about 0.26 ppm/°C.

**D. Thermal compensation**

The ‘Thermal compensation’ schematic diagram is in Fig. 7. It consists of an analog thermometer, the LM50B from National Semiconductors, connected to two buffer amplifiers for obtaining two voltages of opposite sign, proportional to temperature. The two voltages are able to compensate drift of any polarity. The LM50B generates a voltage linearly dependent on temperature having a slope of 10 mV/°C. Its output voltage has an offset of about 800 mV at 300 K. We cancel this offset with proper value of resistors \( R_{T1} \) and \( R_{T2} \), which scale \( V_{REF} \). This offset adjustment determines the feedback of A4 to have a voltage gain slightly larger than one. The final Pos.Tem. and Neg.Tem. slopes are about 12 mV/°C.

![Fig. 7: Thermal compensation circuit schematic.](image)

The Thermal Correcting nodes of the board can refer to one of the two outputs Neg.Tem. and Pos.Tem. via a selected series resistor as follows.

If \( V_{A1th} \), \( V_{DACth} \), \( V_{A2th} \) and \( V_{A3th} \) are the voltage drifts of node A of Fig. 4, the DAC of Fig. 5, and the two OAs \( A_2 \) and \( A_3 \) of Fig. 5, respectively, then at node C of Fig. 5 we expect a total voltage drift of:

\[
V_{Cth} = \frac{R_F}{R_A} (V_{A1th} + V_{DACth} - V_{A2th}) - \frac{R_F}{R_B} V_{A2th} - 2V_{A3th}
\]

(2)

The value of resistors \( R_A \) and \( R_B \) inside the DAC change for every selected value of the DAC output. This means that \( V_{Cth} \) is composed of the sum of 4 terms, the last 2 of which are not dependent on the value of the output voltage selected.

To determine the value of the compensation resistor \( R_1 \) of Fig. 4 and resistors \( R_{c1} \) and \( R_{G1} \) of Fig. 5 that should be connected to nodes Pos.Tem. or Neg.Tem. of Fig. 7, we adopt the following procedure. The voltage drift \( V_{Cth} \) is measured in 2 different working conditions for the DAC, putting the analog-mixed board inside an environmental chamber, and varying its temperature. The first measurement is performed when the DAC output is set at its maximum value. The voltage at node B of Fig. 5 is equal to:

\[
V_{B1th} = -\frac{R_F}{R_{AFS}} (V_{A1th} + V_{DACth} - V_{A2th}) + \frac{R_F}{R_{BFS}} V_{A2th} + V_{A2th}
\]

(3)

where \( R_{AFS} \) and \( R_{BFS} \) are the value that \( R_A \) and \( R_B \) of Fig. 5 have for this DAC setting. In the second measurement the DAC output is put at its minimum value, that coincides to the case \( R_A \) and \( R_B \) form an open circuit. In this situation we can make the following discriminations:

\[
V_{B2th} = V_{A2th}
\]

\[
V_{Cth} = 2V_{A3th} - V_{B2th}
\]

(4)

The DAC used is of R-2R type. When it delivers its maximum output, a factor of \( \gamma = 1/3 \) for the ratio \( R_F/R_{BFS} \) can be calculated. From the \( \gamma \) term and eqs.(3) and (4) we have all the necessary parameters to calculate the compensating resistors:

\[
V_{B1th} - V_{B2th} - \gamma V_{B2th} =
\]

\[
= -\frac{R_F}{R_{AFS}} (V_{A1th} + V_{DACth} - V_{A2th})
\]

\[
= \pm \lambda \frac{R_F}{R_{AFS}} V_{TH} \frac{R_2}{R_1} (R_2 + R_3) + 2R_2 R_3
\]

\[
V_{TH} = 12 \text{ mV/°C}
\]

(5)

The factor \( \lambda \left( -21.2 \times 10^{-3} \right) \) is the ratio between the voltage at node A and node T of Fig. 4, and \( R_3 \) is equal to \( R_4 \). The sign to be used in the above eq. determines if \( R_1 \) should be connected to Pos.Tem. or Neg.Tem. of Fig. 7. In a similar way we have:
\[ V_{B2h} = \pm V_{TH} \frac{R_e}{R_c + R_e}, \]
\[ V_{Cth} = \pm V_{TH} \frac{R_G}{R_G}. \]  

(6)

As can be observed the resistor values determined for the thermal compensation are not dependent on the code selected in the DAC. As a consequence, the compensation is effective above the full range of output voltages.

The compensation circuit realized has a large efficiency. In addition the drift present before compensation is already small. As a consequence, even a hypothetical, very far condition, 10% of compensation error due to device tolerance, aging, and so on, will result anyway in a final drift of less than 1 ppm/°C, well within the required specification.

Switch Signal of Fig. 6 has been shown to add a negligible contribution, ≤ 0.26 ppm/°C. The resistors used to implement the attenuator of Fig. 6 are very stable resistors [6]. We measured them in the temperature range 5 °C ÷ 40 °C. Results are shown in Fig. 8 and Fig. 9.

As can be seen from the histograms it was possible to select and match the attenuators needed with an accuracy close to 0.5 ppm/°C. Therefore we decided to not compensate also for the contribution to the overall drift coming from the network of Fig. 6, since already small enough.

All the calibrations have been done with a VT7004 by Vötsch environmental chamber and the Keithley 2700 multi-channel input 6 ½ digits Voltmeter. The temperature range considered for the test were the interval 5 °C ÷ 40 °C.

Fig. 8: Distribution of the measured drift of the 50 Ω resistors used for the attenuators of Fig. 6.

Fig. 9: Distribution of the measured drift of the 20kΩ resistors used for the attenuators of Fig. 6.

E. CPLD -Firmware

The description of the operation of the firmware of the system is based on the scheme of Fig. 2.

The ‘Clock generator card’ is used to generate the precise time reference for the construction of the analog pulse signals at the analog-mixed board outputs.

This circuit is based on a crystal oscillator module working at 10 MHz. The oscillator has a specified frequency stability of ±50 ppm over its 0-70 °C operating temperature range and for supply voltage in the range 5V±0.25V. A CPLD is present on this card to provide the communication with the other elements of the system.

The input and output communication signals are transmitted using Fiber Optic, FO, lines, that avoid ground loop and/or the conduction of EMI interference inside the Faraday cage. The operation of the circuit is very simple. The CPLD polls the Clock Request FO line and the Trigger Line. When both are found high a clock signal is generated, proportional to the 10 MHz oscillator, and sent at the Clock FO line. The period of the clock output was determined to be 100 μsec with 10% duty cycle, 10 μsec of pulse width. This clock signal terminates when the analog-mixed board completes the generation of the analog pulse. The analog-mixed board notifies this condition by clearing the Clock Request signal.

The analog-mixed board operation is as follows.

All its necessary settings come from a further CPLD, see also Fig. 3. The firmware of this CPLD has been developed using Very high speed Hardware Description Language, VHDL. In the VHDL description, two main blocks are implemented.

The first block, the bus manager, controls the FO lines synchronous serial bus, SDA and SCL, used to communicate with the acquisition system. It polls these synchronous serial bus signals and, when activated, de-serialize the data line to the 8 bits internal parallel bus of the analog-mixed board, or serialize the 8 bits internal parallel bus to the data line. Since
many analog-mixed boards compose the system, each analog-mixed board has its own address and the protocol of communication is addressable from the remote system.

The second block, the board manager block, has a double task. It allows the proper setting of the analog-mixed board on the basis of the pattern received remotely and provides the commands for the generation of the analog output pulses.

It needs four bytes to configure the analog-mixed board. The first byte is for the determination of the analog pulse width to be generated. The number stored in this cell gives the analog pulse width in units of 100 µsec. The pulse width can then be as long as 25.5 msec. A second byte contains the eight less significant bits of the twelve bits of the DAC. The third byte is divided in two parts, the four LSBs are the most significant bits of the DAC. Bits 5 and 4 select which of the four possible outputs of the board must be fired if Bit 6 is 0, otherwise (Bit 6 = 1) they address the selector of Fig. 3. The auxiliary analog output can be the reference voltage present at node A of Fig. 4 or the signal present at node C of Fig. 5. Bit 7 asks for the generation of the pulse when set equal to 1, if Bit 6 is 0. It is auto-cleared when the pulse is finished. The fourth byte is used to select the output attenuation of each of the four channels present on the board. The byte is divided in four pairs of bits, one for each of the 4 channels present on the analog-mixed board. As can be seen in Fig. 6 there are only 3 possible attenuations selectable. The remaining code of each pair of bits is dedicated to the disconnection of the respective output, when selected.

The generation of a pulse is as follows. The remote system sets the first 3 bytes of the analog-mixed board. The fourth byte needs to be set only once, at the start of the data tacking. If bit 7 of the third byte is 1, the analog-mixed board set the Clock request FO line. When the Trigger line is also set by the boards goes in the idle state. When a pulse generation is in progress all the write operations are disabled to avoid errors.

For all of these operations the CPLD present on the analog-mixed board uses two clock sources, a 500 KHz clock from an on board R-C oscillator, NE555 based, and the 100 µsec clock described above, from the external Clock FO line.

The 500 KHz clock is used for the serial bus communication and for the board setting. It is normally idle and is waken up when either SCL or SDA lines change from their idle state. The 100 µsec clock is the precise reference for the definition of the analog pulse width. It is generated and received on the Clock FO line only when the Clock request and Trigger lines are set from the analog-mixed board itself and the remote system, respectively.

In Fig. 10 the schematic diagram of a bi-directional FO single line used for the synchronous serial bus is shown. It is implemented with two FOs. An Infineon SFH551 converts the signal received from light to TTL, open collector. A Schmidt trigger stabilizes the speed of response. A MOS allows sending back the data on the line. A second FO reads back the data converted from TTL level to light by a buffered Infineon SFH756. In case the line is mono-directional the sender FO and the MOS are not present. Resistors Rf are for line termination and Rp is the pull-up resistor. In Fig. 10 the part of the circuit inside the box is the light to TTL transceiver of Fig. 2.

The implementation of the above-described synchronous FO serial bus uses 4 FOs to operate.

![Fig. 10: An input/output fiber optic line schematic. The rectangular box surrounds the light to/from TTL transducer of Fig. 2.](image)

### IV. MEASUREMENT RESULTS

The accurate characterization of a precise instrument is a very difficult task. The energy given by the pulse generator is proportional to both its width and the square of its amplitude. The pulse error can be expressed in first approximation as:

$$\frac{\Delta E_G}{E_G} = 2 \frac{\Delta V_G}{V_G} + \frac{\Delta t_W}{t_W} + \frac{\Delta R_H}{R_H};$$

(7)

with $E_G$, $V_G$ and $t_W$ defined in eq.(1). We concentrate on the evaluation of the first two terms of the above eq.

The accuracy of the stationary amplitude of the output signal, after thermal compensation, has been obtained under the condition that the switch Signal of Fig. 6 remains always closed during the measurement. During all the tests the 'Clock generator card', the 'Light to/from TTL card' and the 'Analog-mixed board' of Fig. 2 were put inside an environmental chamber the VT7004 by Vötsch. Measurements have been done with a 6 ½ digit multimeter, Keithley 2700.

Results have been very good. As a typical example we show in Fig. 11 the drift at the output at the Atten. 3 pin of Fig. 6. In the Fig. it is shown, left axis, the output of Atten. 3 after its settled average value of 12 mV has been subtracted.

The two horizontal lines superimposed on the curve are where the drift has been extrapolated. On the right axis the corresponding output of the Pos.Tem. of the thermometer of Fig. 7 is shown for reference. The temperature at the output stabilized at 5 °C from counts 20 to counts 40, then was changed to 40 °C from count 40. Each count correspond to
The drift observed in the measurements is about \(-0.6\) ppm/°C. A similar figure of merit has been obtained for all the other outputs.

The pulse width may change with temperature. We have made measurements with the purpose to estimate its effects. The measurements have been taken for the oscillator and the pulse width at the Atten. 1 output of Fig. 6. Measurements have been made in the following way. The signal was triggered at its start, at half of its amplitude, on the rising edge. Then the time scale of the scope, TDS5052 by Tektronix, was delayed an interval equal to the pulse width. The difference between the start time and the stop time, measured at half amplitude of the signal, were considered equal to the width of the pulse.

Since the pulse generator can give arbitrary pulse width in the range 100 \(\mu\)sec to 25 msec, this procedure was repeated at different pulse widths, to study the behaviour. The measurements have been taken at 5 °C and 40 °C. The set-up described allows us to have a precision of the measurements that we estimate about \(\pm 0.5\) ppm/°C. In Fig. 12 a photograph is shown of the falling edge, at the end of the pulse, for one of the measurements taken at the Atten. 1 output at 40 °C.

The final drift of the oscillator resulted limited by our sensitivity, \(\leq 0.5\) ppm/°C.

The signal width at the output Atten. 1 showed a drift of about 1 ppm/°C in the more stringent condition of 100 \(\mu\)sec of pulse width, 0.1 msec/\(\tau_w\)(msec) ppm/°C. It has to be considered that the change of the width of the pulse is independent from the width itself. The two results prove that the oscillator does not contribute to the drift of the pulse width. We have anyway verified the thermal drift of the oscillator adopted. We measured its frequency with a HP53132A (225Mhz Universal Counter) at 5, 10, 20, 30 and 40 °C. The maximum value measured was 0.12 ppm/°C.

Fig. 11: Drift at the output Atten. 3 of Fig. 6, after the temperature change from 5 °C to 40 °C, left axis. The horizontal lines are where the drift has been measured. On the right axis the thermometer output Pos.Tem. of Fig. 7 is shown for reference purpose. It changes about 12 mv/°C. The measurements have been taken every 100 sec.

Fig. 12: Falling edge of the pulse after the scope has been triggered on the rising edge, half amplitude at T 40 °C. The histogram shows the statistics operated over many pulses. The vertical scale is 10mV/div and the horizontal one is 400ns/div. The measured pulse duration has a mean value of 1.000218ms.

So far we have described results obtained when the amplitude of output voltage is measured at DC and the pulse width is measured at a determined threshold. One other source of possible error may arise if the rise or fall time of the signals change, for instance due to the settling time of the OA A3 of Fig. 5 when forced to change the driving current promptly. This phenomenon is correlated with the pulse width drift. As a worst condition we have considered the two effects anyway as independent. We have measured the rise and fall time changes with temperature and verified that the fall time remained practically constant within the temperature range between 5°C and 40°C. Its variation was only a few nsec above 880 nsec. This features was expected since the signal fall time is governed only by the discharging of the filtering capacitance \(C_f\) of Fig. 6 with the resistors connected to it. The rise time changed about 25 nsec in the temperature range considered. This is mainly due to the settling time of the OA A3 of Fig. 5. It is very easy to quantify the error that comes from the rise time change. The rise and fall times of the signal pulses of the circuit implemented are free from any overshoot or undershoot and governed by a simple exponential time constant for both edges. A pulse of unitary amplitude can therefore be modeled as:

\[
V(t) = \begin{cases} 
1 - \exp\left(-\frac{t}{\tau_r}\right) & \text{if } t < t_f \\
1 - \exp\left(-\frac{t-t_f}{\tau_f}\right) & \text{if } t \geq t_f
\end{cases}
\]

where \(\tau_r\) and \(\tau_f\) are the time constants for the rise and fall time, respectively. The energy given to the heater is proportional to the square of eq.(8). If we suppose that only the rise time drifts we easily obtain (\(F\) is for final, \(I\) for initial):
\[ \Delta E = \int_{0}^{+\infty} \left[ V(t)^2 - V(t + \tau)^2 \right] dt = \frac{3}{2} [\tau F - \tau R] = 0.68 \left[ \tau F - \tau R \right] \]

where in the last eq. it has been considered that the rise time \( t_r \) equals 2.2 times the time constant \( \tau_r \). The rise time drift has been measured over a range of 35 °C. From eq. (9) we therefore get about 0.485 msec/t W(msec) ppm/oC of drift in the energy as only the rise time fluctuates with temperature. The drift considered is independent of the pulse width, therefore it increases its effect at the smaller pulse width.

We have measured also the noise due to the jitter of the width of the output pulses. In Fig. 13 there is a photograph where the histogram of the jitter of the falling edge is measured, after the signal has been triggered on the rising edge. Due the limited memory available on the scope and for the required high sample rate, to get enough time resolution we delayed the sampling window shown by 99.9 \( \mu \)s. The trigger level was set at about 20 % and the jitter was evaluated at about 80 % of signal amplitude.

The jitter resulted about 3.5 ppm\(_{RMS} \) at 1 msec of pulse width.

Another issue is the long term stability. The circuits components we have used have specified, on the average, a few tens of ppm/month in their first period of life. To try to limit this performance to a few ppm/month we aged the realized circuits by worming them at about 50 °C. From eq. (9) we therefore get about 0.485 msec/tW(msec) ppm/oC of drift in the energy as only the rise time fluctuates with temperature. The drift considered is independent of the pulse width, therefore it increases its effect at the smaller pulse width.

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Another issue is the long term stability. The circuits components we have used have specified, on the average, a few tens of ppm/month in their first period of life. To try to limit this performance to a few ppm/month we aged the realized circuits by worming them at about 50 °C for days. This together to the periodical (monthly) use of a particle source, should allow to maintain the overall system stability within the limits showed above.

V. CONCLUSIONS

A very precise and stable pulse generator for an array of bolometric detectors has been realized. It is able to generate square pulses having maximum programmable amplitude that, after resistive divider, is 40 mV, with 12 bits of resolution. The width of the pulse can be set between 100 \( \mu \)sec and 25 msec. All the features of the realized instrument can be programmed remotely with a fiber optic synchronous serial bus.

The drift of the amplitude of the pulse was less than 1 ppm/oC. The drift of the pulse width, \( t_W \), was about 1 msec/tW(msec) ppm/oC. Concerning variation of the rise/fall time duration, it was verified a drift of 0.5 msec/tW(msec) ppm/oC. The drifts have been measured in the temperature range 5°C to 40°C.

The noise due to the jitter was about 3.5 ppm\(_{RMS} \) at 1 msec of pulse width.

By supposing a possible change of the room temperature of about \( \pm 5 \) °C, we expect, as a worst condition, 35 ppm (or 87.5 eV at 2.5 MeV) of absolute precision of the calibrating signal at 1 msec pulse width. This figure is much better than the expected detector resolution, which is about 850 ppm\(_{RMS} \) (5 KeV\(_{FWHM} \) at 2.5 MeV particle energy as a best condition).

VI. ACKNOWLEDGEMENTS

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VII. REFERENCES

[6] The resistances used are the A02 from NR New Resistance, Via Garibaldi 21 20092 Cinisello Balsamo IT. The A02 are based on the Bulk Metal\(_{\text{foil}} \) technology.