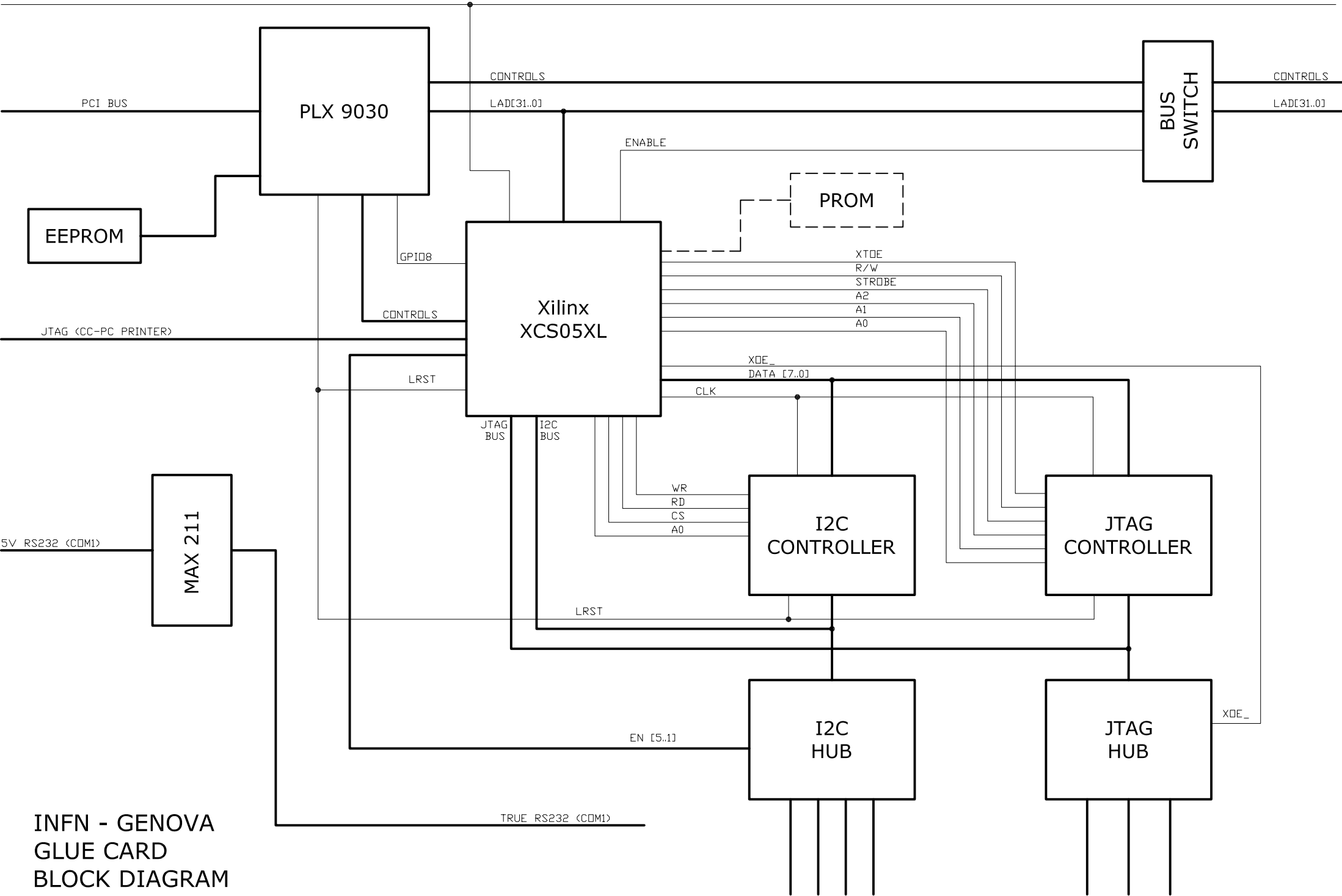


Glue Logic Interface for Smart PC and Test Board

*Flavio Fontanelli, Giuseppe Mini, Mario Sannino
INFN - Sezione di Genova*

CC-PC RESET (CORE)



INFN - GENOVA
GLUE CARD
BLOCK DIAGRAM

Glue Logic Board

Glue Card Features

Busses: 4 I2C (100/400Kb/s), 3 JTAG ($\approx 1\text{Mb/s}$), 1 PLX 9030 Local Bus (10Mhz – to be tested @40Mhz)

FPGA Program: The Xilinx FPGA is connected to the CC-PC parallel port in order to be able to use the commercial programs but also a PROM can be used.

Access during use: All the devices on the glue card are connected to the 9030 local bus and can be reached from the PCI bus.

Logical Devices: The three logical devices of the glue card are the I2C controller (2 addresses), the JTAG controller (8 addresses) and the Enable register (1 address).

Addresses: All the addresses will be located under the PLX9030 address space 0. The Chip select 0 (CS0) is used by the glue card so DON'T USE IT.

Glue Logic Board

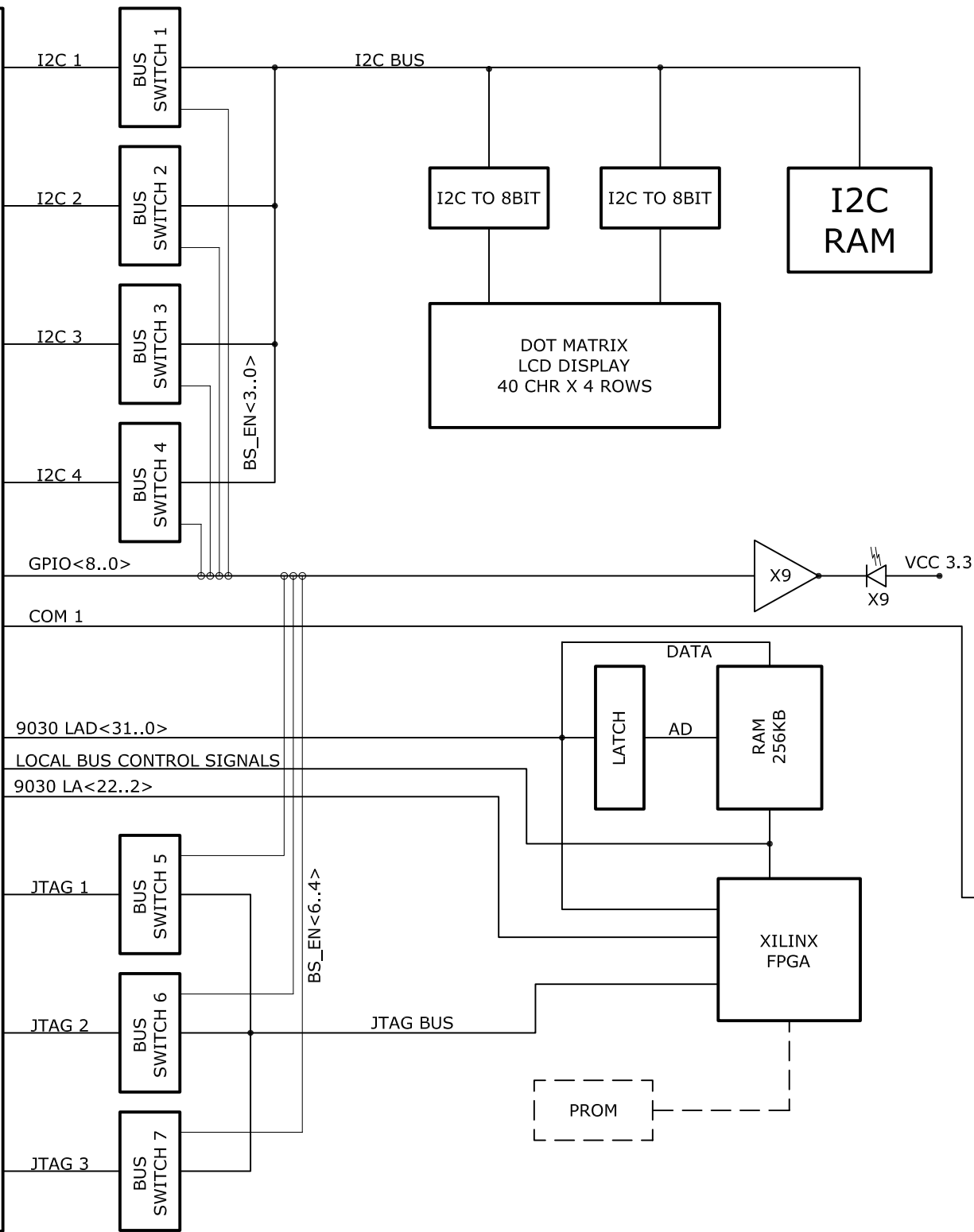
Reset Logic

1. Each bus can be tri-stated individually setting or resetting the right bit on the enable register (9030 local bus - 1 bit, I2C hub - 4 bit, JTAG hub - 1 bit).
2. At power on all the busses are tri-stated and the computer program must enable the various busses before using them.
3. The FPGA program automatically tri-states all the busses if an hardware reset is sent to the CC-PC.
4. Before a soft re-boot of the CC-PC the user can easily tri-state all the busses by accessing the enable register.
5. It's possible to send a reset to the glue logic through the 9030 LRESET signal (software controlled)

FROM CC-PC J2

GLUE CARD

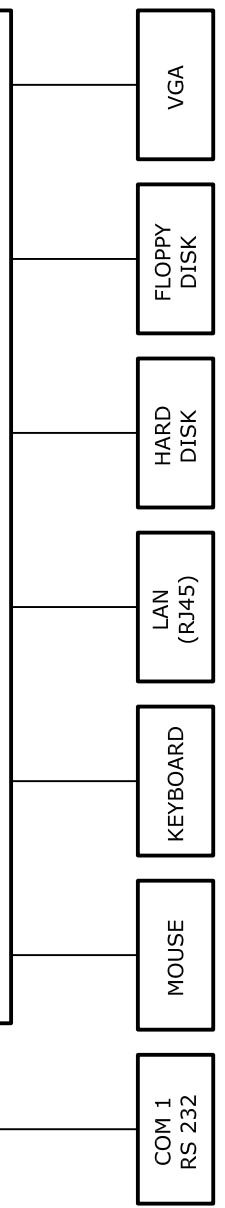
LHCB CONNECTOR



J1

CREDIT CARD PC

J2



INFN - GENOVA
GLUE CARD
TEST BOARD
BLOCK DIAGRAM

Glue Logic Board

Test board features

1. The PCB will be in compliance with the ATX form factor and it can be assembled inside a standard ATX chassis for PC.
2. Also the connectors are the same of a standard PC so we will be able to connect to it standard PC peripherals and power supply.
3. Anyway also a dot matrix LCD display (40x4) will be assembled in order to allow the user to test a glue card running the diagnostic programs and using only a floppy disk and a DC power supply. (LINUX/DOS programs).
4. The I2C bus is tested by writing / reading data on the I2C RAM and Display.
5. The GPIO are tested by means LED and used to enable the various busses.
6. The Local bus is tested by writing / reading the RAM and the FPGA.
7. The JTAG bus is tested by programming the XILINX and re-reading its content.