

TOTEM

TOTEM Experiment

COINCIDENCE CHIP SPECIFICATION

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TOTEM COINCIDENCE CHIP SPECIFICATION

Abstract

This document provides the full specification of the TOTEM coincidence chip, the CC chip. This chip will act on fast trigger signals generated by the detectors' front ends to establish coincidence between different detector planes to establish that a certain number of tracks traversed the detector. In addition the chip will impose some multiplicity constraints to verify whether the event for which particle tracks were detected is sufficiently interesting to generate a level 1 trigger for its readout. This chip is the basis for the generation of the trigger signals provided by TOTEM to the CMS global trigger.

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1 Introduction

The detector front ends in TOTEM generate fast signals which are used to generate the trigger signals provided by TOTEM to the CMS global trigger box. We have opted for the development of a full custom chip rather than using a Field Programmable Gate Array for two main reasons:

1. The latency constraints on the generation of the trigger bits especially from the Roman Pots are very severe: after subtraction of cable delays only about 8-10 bunch crossings are left for the generation of the trigger signals to be provided to CMS from the signals generated by the Roman Pot detector front end. A full custom chip with dedicated logic can implement the required coincidence in one clock cycle, while an FPGA will typically need more time because it was conceived to be much more versatile.
2. Special design techniques can make a full custom chip much more robust against radiation both with regard to total dose and single event effects. This allows to place this chip in aggressive radiation environments very near the detectors. This has the non-negligible advantage that the number of signals is very severely reduced prior to carrying these signals away from the detector, which presents considerable space and cost savings. (Note that the CC chip will be submitted together with the VFAT chip for a very limited marginal cost).

Some programmability of the CC chip is required to deal with different detector geometries and evaluate trigger efficiencies. This programmability is achieved through the use of an I2C interface which makes the CC chip compatible with the standard CMS tracker and ecal control system. This system will also control the VFAT and APV used within the TOTEM experiment and therefore this was the most cost-effective way to obtain programmable trigger generation hardware.

2 Architecture

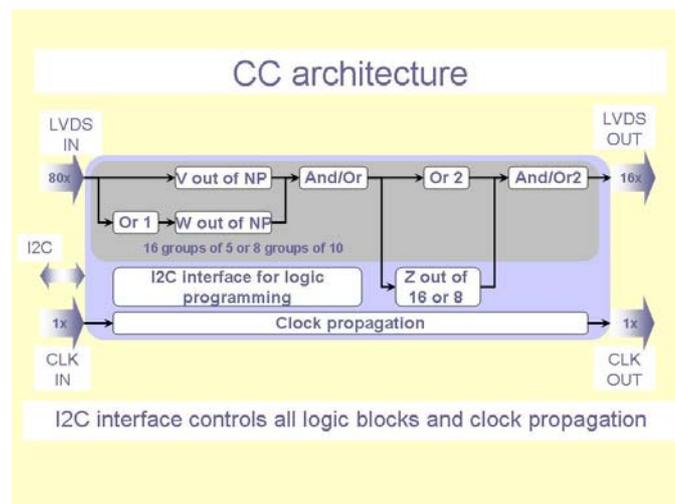


Fig. 1. General CC architecture.

Fig. 1 shows the general CC architecture. The VFAT sends LVDS signals to avoid coupling of digital signals into the analog front end. The CC chip receives 80 digital inputs which normally will be converted from LVDS into single-ended CMOS signals by a number of LVDS to CMOS converter chips. This limits the number of pads on the CC chip and limits its chip area. These 80 digital signals normally correspond to a certain number of coordinates or sectors on a certain number of detector planes. To establish that a real particle track passed through the detector, coincidence will be required between detector planes in corresponding coordinates.

For flexibility the number of detector planes between which coincidence will be required is programmable. To implement this, the inputs are grouped as illustrated in fig. 2. The maximum number of planes is fixed at 10. If the number of planes is 5 or less, the inputs will be grouped in groups of 5 each of which will correspond to a certain coordinate on the different detector planes between which coincidence will be required. If the number of planes is 5 all inputs in a group will be used, if the number is less, the last input or inputs in each group will not be used, and will be disabled internally to avoid errors due to floating inputs. In addition high-value resistors are used to avoid arbitrary floating of non-used inputs.

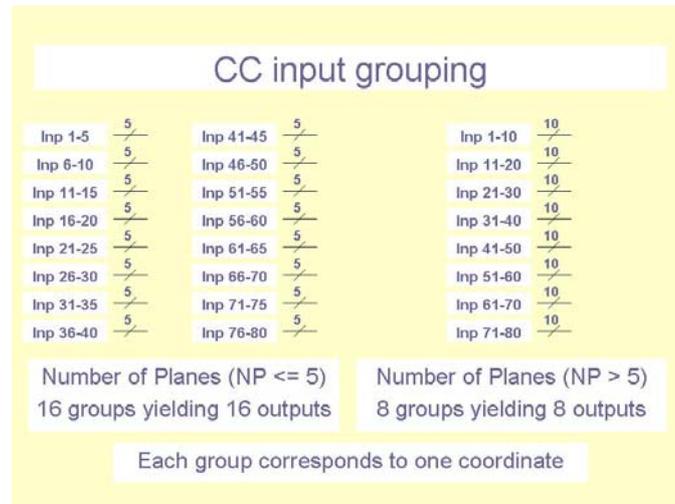


Fig. 2. General organization of the inputs of the CC chip.

If the number of planes to be put into coincidence is greater than 5, the inputs will be grouped in groups of 10, possibly with the last ones unused for a number of planes less than 10. This choice of creating groups of inputs has been made as a compromise between on-chip interconnect complexity and efficient use of inputs: allowing grouping of inputs in a fully arbitrary way would result in very complex interconnect; having two modes of grouping makes the use of the chip more efficient for a small number of detector planes.

The number of planes is specified in the I2C register NP.

Now the different programmable logic blocks in the CC will be detailed:

A first coincidence is carried out in the **V out of NP** block. For every group of inputs a coincidence signal will be generated requiring at least V out of the number of planes (NP) to be “on” in the corresponding coordinate. V should be specified less or equal to NP. If larger the coincidence result will always be zero. V is specified in the I2C register V.

To account for non-perfect alignment between detector planes and particles which traverse the detector at some angle another coincidence is carried out by the **W out of NP** block. The signals presented to this block are the result of an OR (**OR 1**) of the corresponding coordinate in a detector plane with a certain number of its nearest neighbors specified by OV. For instance if OV equals one, each coordinate will be “or-ed” with the input corresponding to the same plane of the previous group of inputs and with the input corresponding to the same plane of the next group of inputs. So, for instance, for NP equal to 5, the or signal corresponding to input 6 will be the or of input 1, input 6, and input 11. At the edges the or will be carried out only on the available neighbour signals (so for input 1 only input 1 and input 6 will be “or-ed”). OV can be maximum 8 and is specified in the I2C register OV.

The result of this OR 1 is presented to the coincidence block **W out of NP**. Allowing some overlap gives margin for tracks at a small angle, some misalignment between planes, etc... Similar to the V out of NP block, W should be specified less or equal to NP. If larger the coincidence result will always be zero. W is specified in the I2C register W.

The result of these two coincidence blocks V out of NP and W out of NP will then be combined in the **And/Or** block. They can be ored, anded, or only one of the two can be considered. Which of these is carried out is determined by the I2C register AO.

AO 1	AO 0	Resulting function for And/Or
0	0	(V out of NP) and (W out of NP) (default)
0	1	(V out of NP) and (W out of NP)
1	0	V out of NP
1	1	W out of NP

Table 1. Definition of the function controlled by the AO register.

The **OR 2** block will combine the 16 or 8 outputs into a lesser number, if so desired: once coincidence has been established it is not always needed to have very detailed coordinate or sector information. Therefore it is possible to or sectors in groups of 2, 4 or 8. In that case only the output corresponding to the first output of the group will be active. The other outputs will be powered down to save power in the LVDS buffers. (specify whether they need to be bonded or can be left unconnected !!!). The operation of the OR 2 block is controlled by the I2C register O2.

O2 1	O2 0	Resulting function for Or 2
0	0	Output all outputs (default)
0	1	Group outputs in groups of 2
1	0	Group outputs in groups of 4
1	1	Group outputs in groups of 8

Table 2. Definition of the function controlled by the O2 register.

The **Z out of 8 or 16** coincidence block provides a multiplicity criterion: if more than Z groups out of 8 or 16 depending on the mode of the circuit are active, the trigger outputs can be masked, or it can be used as another condition. The I2C register LO controls which function is implemented in the **And/Or 2 block**. The block can also be configured to invert the outputs.

LO 1	LO 0	Resulting function for And/Or 2
0	0	Output and not(Z out of 8 or 16) (default)
0	1	Output and (Z out of 8 or 16)
1	0	Not(Output and not(Z out of 8 or 16))
1	1	Not(Output and (Z out of 8 or 16))

Table 3. Definition of the function controlled by the LO register.

Similarly the I2C register LI controls whether the inputs are inverted or not.

LI	Resulting function for the inputs
0	Inputs not inverted (default)
1	Inputs inverted

Table 4. Definition of the function controlled by the LI register.

3 Propagation path for the Clock

The CC chip will be used close to the detector but also at a few meters away. This creates a synchronization issue and requires the cable delay to be taken into account by the clock applied to the CC chip. A straight forward way to take this delay into account is to have the clock propagate in an identical way as the signals. Therefore a propagation path for the clock is foreseen on the CC chip. The I2C register CL determines whether the input signals are sampled and evaluated during the rising or falling edge of the clock. The data will become available at the outputs a few gate delays after the clock edge used for evaluation.

CL	Definition of the evaluation moment
0	Evaluation on rising edge of CLK (default)
1	Evaluation on falling edge of CLK

Table 5. Definition of the evaluation moment controlled by the CL register.

4 Organization of the I2C registers

The previous section defined how the I2C registers influence the logic function of the chip. Here we organize these registers in groups of 8, which is the standard format for I2C. Four eight bit I2C registers fully control the logic function implemented by the CC chip. The following figure gives an overview:



Fig. 3. Organization of the I2C registers.

5 List and organization of the pads

The following table contains a detailed list of pads under the assumption that the chip itself is preceded by LVDS to CMOS converter chips. The idea behind this is to limit the area of the pad limited CC chip by limiting the number of pads of the CC chip itself. The LVDS to CMOS converter chip will contain 17 channels, 16 data channels and one clock channel for clock propagation. The exact organization of the pads is not fully finalized yet, because the packaging of the chip is still under study, probably some more power and ground pads will be added.

Pad	Function	Pad	Function								
1	GND	22	GND	42	GND	62	GND	82	GND	102	GND
2	GND	23	GND	43	GND	63	GND	83	GND	103	GND
3	In1	24	In17	44	In33	64	In49	84	In65	104-105	Out1
4	In2	25	In18	45	In34	65	In50	85	In66	106-107	Out2
5	In3	26	In19	46	In35	66	In51	86	In67	108-109	Out3
6	In4	27	In20	47	In36	67	In52	87	In68	110-111	Out4
7	In5	28	In21	48	In37	68	In53	88	In69	112-113	Out5
8	In6	29	In22	49	In38	69	In54	89	In70	114-115	Out6
9	In7	30	In23	50	In39	70	In55	90	In71	116-117	Out7
10	In8	31	In24	51	In40	71	In56	91	In72	118-119	Out8

11	In9	32	In25	52	In41	72	In57	92	In73	120-121	Out9
12	In10	33	In26	53	In42	73	In58	93	In74	122-123	Out10
13	In11	34	In27	54	In43	74	In59	94	In75	124-125	Out11
14	In12	35	In28	55	In44	75	In60	95	In76	126-127	Out12
15	In13	36	In29	56	In45	76	In61	96	In77	128-129	Out13
16	In14	37	In30	57	In46	77	In62	97	In78	130-131	Out14
17	In15	38	In31	58	In47	78	In63	98	In79	132-133	Out15
18	In16	39	In32	59	In48	79	In64	99	In80	134-135	Out16
19	CLK									136-137	CLKOUT
20	VDD	40	VDD	60	VDD	80	VDD	100	VDD	138	VDD
21	VDD	41	VDD	61	VDD	81	VDD	101	VDD	139	VDD
140	GND	141	SCL	142	SDA	143	VDD				

Table 6. Definition of the pads of the CC.

Need foot print for the chip and packaging details.

6 Conclusions: benefits for the experiment

The CC chip is a chip which carries out a programmable coincidence in straight-forward way. It offers the following advantages:

1. It is radiation tolerant and can be mounted on or very near the detector, where it severely reduces the number of coincidence signals before these are sent to the counting room. For instance in the GEM it will reduce the number of bits from about 4000 to only a few (here the CC chip will be cascaded in two or three layers). For the Roman Pots two chips will be needed per pot, one for each coordinate, which reduce the number of trigger bits from $16 \cdot 10$ planes/pot * 6 pots = 960 to $32/\text{pot} \cdot 6$ pots = 192. A few more CC chips are needed on the Roman Pot station card to reduce the number of bits further to less than 20 per Roman Pot station.
2. It is controlled by means of I2C and as such is fully integrated with the TOTEM standard control system.
3. It offers very minimal latency (less than a clock cycle) and is therefore ideally suited to match the severe trigger latency requirements for the Roman Pot system to be compatible with the CMS global trigger timing.