

GOH Power Up Implementation Recommendations

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1. Background

The GOL Opto-hybrid (GOH) has been developed for the CMS ECAL Optical Data Link system [1]. It employs the Gigabit Optical Link (GOL) serializer and laser driver chip [2].

It was discovered starting in late 2002 and subsequently verified by many users that there is a start up issue with respect to the GOL [3]: “The GOL does not start properly if the clock input signal is present before power on. What is critical about this condition is that a reset pulse is not able to restore normal operation.”

2. Resolution of start up and lockup issues

To resolve the start up issue with respect to the GOH, and to allow a power reset in case of GOL lockup, a number of design changes were made to the GOH:

1. The single-ended clock input (CLKLHC) to the GOL was connected to ground.
2. The “Flag0” input to the GOH was added, which is connected to the selectDiff input to the GOL.
3. The CRT4T power-switching transistor [4] was implemented and the “Flag1” input to the GOH was added, which is connected to the gate of the CRT4T.

The goal of these changes was to allow the user to power up the GOH in the absence of the input clock and to power cycle the GOH if necessary.

3. State-machine description of the GOH

The GOH may be thought of as a state machine with four possible states: Power Up, Operation, GOL Reset and Power Cycle.

At GOH power up, pull-down's on the GOH define the Power Up state. Transitions to the other states, and then between other states, are possible by setting Flag0, Flag1 and/or Reset_B inputs to the GOH. This is described in Figure 1. The inputs are described in Table 1. Notes on the four states:

Power Up: Flag0 is connected to selectDiff input to the GOL. Pull-up of selectDiff in the GOL selects the differential clock input to the GOL, which might already be active. This could lead to the undesirable lockup condition. There is neither pull-up nor pull-down of selectDiff on the GOH. This is in order to be backwards compatible with earlier mother cards. On some (the GOH eval. card for example) the power arrives to the GOH before the clock and the GOL starts without problems. This is not guaranteed for all mother cards! Therefore it is recommended to implement a pull-down of Flag0 on the mother card.
Flag1 is connected to the gate of the CRT4T. It is pulled down on the GOH (GOH powered on). This is in order to be backwards compatible with earlier mother cards.

- Operation: Reset_B must be set to 1 if it is not already. There is neither pull-up nor pull-down of Reset_B on the GOH. Therefore it is recommended to implement a pull-up of Reset_B on the mother card.
Flag0 must be set to 1 (select differential clock).
- GOL Reset: Flag0 must be set to 0 (select grounded single-ended clock).
Reset_B must be set to 0 (GOL master reset).
- Power Cycle: Flag0 must be set to 0 (select grounded single-ended clock).
Flag1 must be set to 1 (GOH powered off). The power-down time of the GOH is
on the order of 10 ns. It is recommended to leave the GOH powered off for at least ~100 ns or (ideally) $\geq 1 \mu\text{s}$.
Flag1 must be set back to 0 (GOH powered on).

4. CRT4T issues

The CRT4T power-switching transistor chip [4] is a CMOS (2.5V) device which exhibits gradual switch-on for gate voltages from 0V or 2.5V. At some intermediate voltages it has been observed to dissipate enough heat to auto-desolder from the PCB. Clearly this is undesirable.

The Flag1 GOH input (connected to the CRT4T gate) is implemented with a 10 kOhm pull-down resistor. This implies that the mother card should not implement a large series resistance on its Flag1 signal; otherwise the voltage divider could result in a gate voltage too far from 2.5V on a Flag1=1 (GOH intended to be powered off) signal.

The power characteristics of the CRT4T are illustrated in Figure 2 through Figure 4. Tests were performed using a GOH evaluation card driving a GOH with a GOL laser driver bias current setting of about 14 mA.

Figure 2 shows the current drawn by the evaluation card vs. gate voltage. At $V_{\text{gate}} = 2.5\text{V}$, the GOH is fully off, and the evaluation card itself is drawing 0.4A. At $V_{\text{gate}} = 0\text{V}$, the GOH is fully on and the evaluation card plus GOH are together drawing 0.5A. At intermediate values of V_{gate} the current spikes and would rise above 1 A if the current supply were not current-limited.

Figure 3 and Figure 4 show detail of the low and high V_{gate} regions. Clearly the mother card should avoid excursions in the region $0.4\text{V} < V_{\text{gate}} < 2.2\text{V}$ for any significant period of time. This implies any series resistance on the mother card's Flag1 signal should be 1 kOhm or less, ideally 500 Ohm or less.

Measurements are ongoing to determine the intrinsic minimum switching time of the CRT4T and the amount of energy dissipated in the CRT4T as a function of ramping speed from $V_{\text{gate}} = 0\text{V}$ to $V_{\text{gate}} = 2.5\text{V}$ and back. Preliminary results are that the former is on the order of 10 ns or faster, and that for ramping speeds of up to $1 \mu\text{s}$ the amount of energy dissipated is negligible.

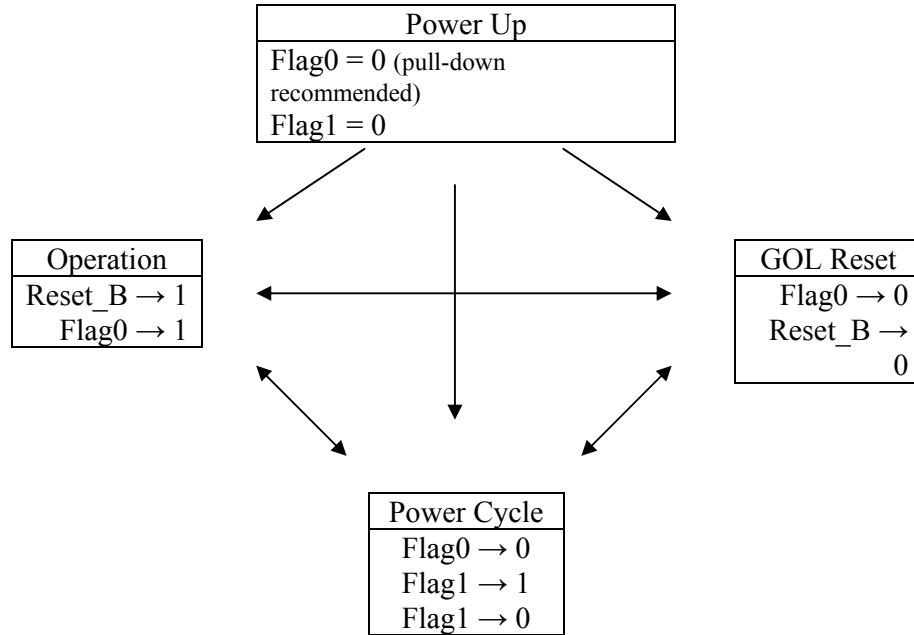


Figure 1. State-machine description of the GOH. Inputs to the GOH which must be changed to arrive at the indicated state are shown. Valid transitions are indicated with arrows.

GOH input	Description	Note	Implementation Recommendation
Flag0	Connected to selectDiff input to GOL (selects between differential and single-ended clock inputs). Pull-up on GOL. 0: single-ended input CLKLHC 1: differential inputs CLKLHCP, CLKLHCN	CLKLHC is connected to ground on the GOH.	Implement pull-down on mother card.
Flag1	Connected to gate of CRT4T. Pull-down on GOH. 0: GOH powered on 1: GOH powered off		
Reset_B	Connected to Reset_B input to GOL (master reset). 0: reset		Implement pull-up on mother card.

Table 1. Description of GOH inputs.

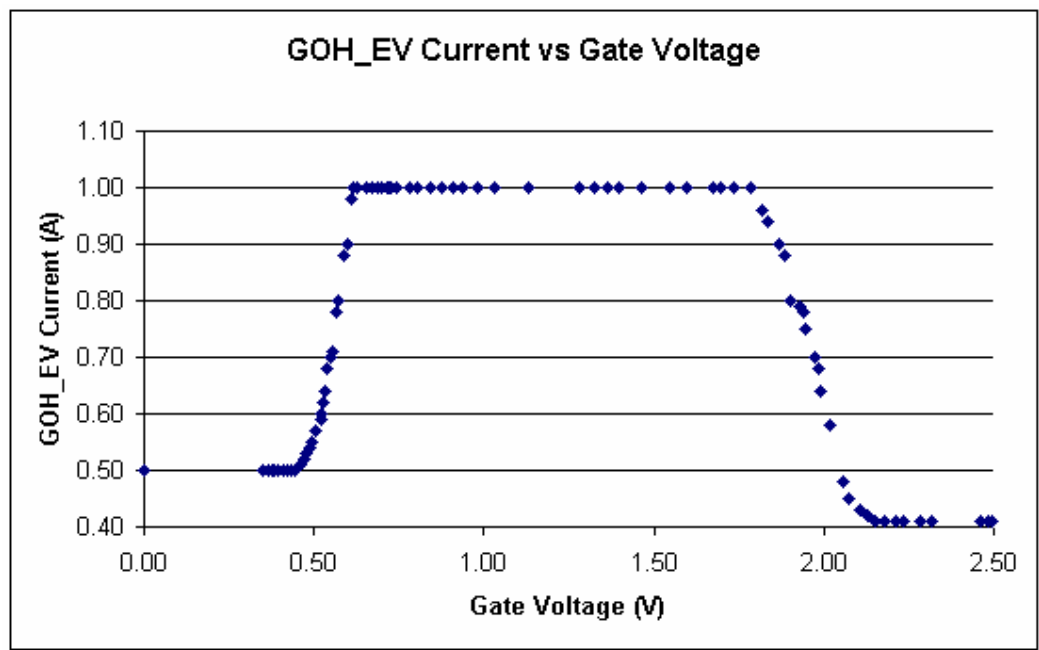


Figure 2. Current drawn by a GOH evaluation card vs. CRT4T gate voltage

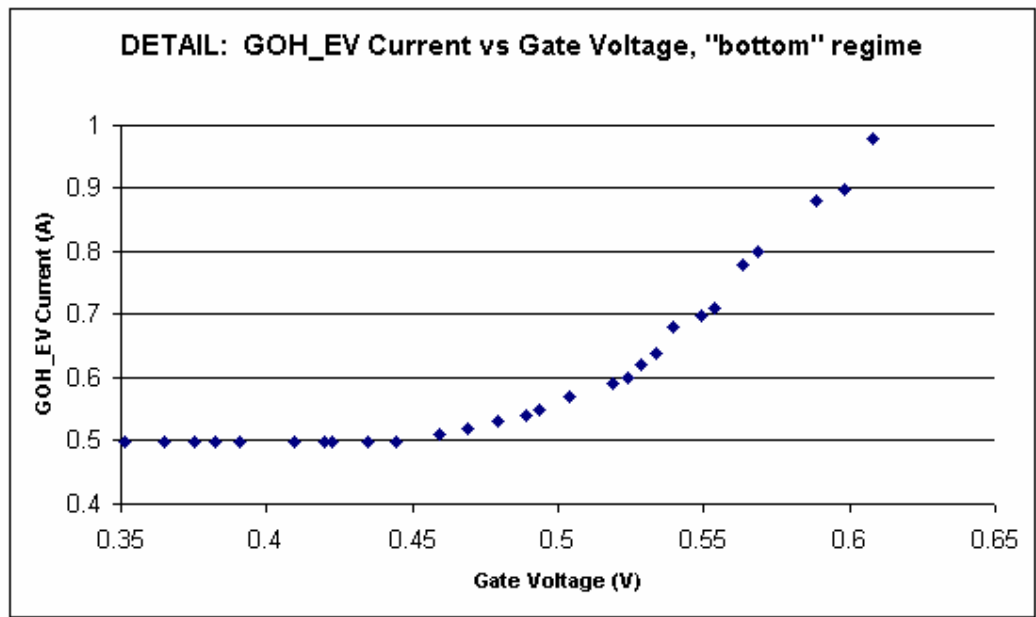


Figure 3. Current drawn by a GOH evaluation card vs. CRT4T gate voltage, low V_{gate} regime.

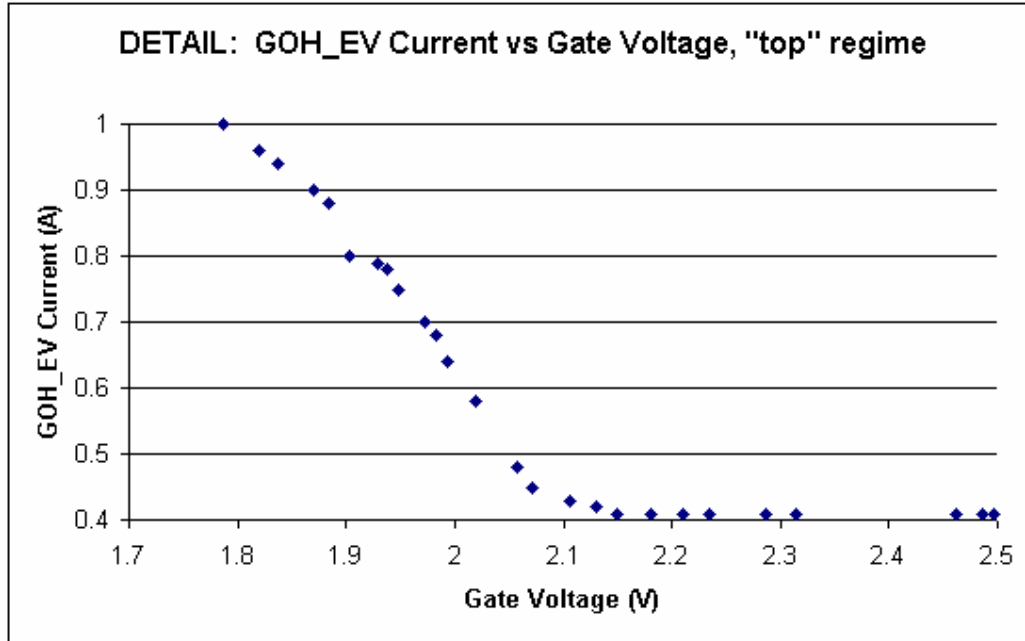


Figure 4. Current drawn by a GOH evaluation card vs. CRT4T gate voltage, high V_{gate} regime

5. References

- [1] J. Grahl, “GOL Opto-Hybrid Manufacturing Specifications”, v. 3.30 (2003). http://cms-ecal-optical-links.web.cern.ch/cms-ecal-optical-links/content/GOH_Specification.doc
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- [3] P. Moreira, “GOL Startup Problem”, CERN EP/MIC private note (2003).
- [4] P. Moreira, “CRT4T”, Rev. 1.0, CERN EP/MIC private note (2003).