A G H U N I V E R S I T Y O F S C I E N C E A N D T E C H N O L O G Y
C R A C O W , P O L A N D

FACULTY OF ELECTRICAL ENGINEERING, AUTOMATICS, COMPUTER SCIENCE AND ELECTRONICS

Fast Bipolar and CMOS Rad-Hard Front End Electronics for Silicon Strip Detectors

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Doctoral Thesis

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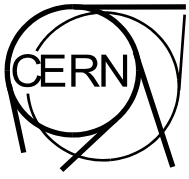

Streszczenie

Prezentowana praca doktorska opisuje projekt szybkiej, odpornej na promieniowanie elektroniki front-end do odczytu paskowych detektorów krzemowych używanych w eksperymentach fizyki wysokich energii budowanych wokół nowo powstającego akceleratora LHC (*ang.: Large Hadron Collider*).

Wielki zderzacz hadronowy (LHC) jest nowym akceleratorem budowanym w Europejskim Centrum Fizyki Wysokich Energii (CERN) pod Genewą, który będzie umożliwiał zderzenia protonów z energią 14 TeV w układzie środka masy, o rząd wielkości większą w porównaniu do akceleratorów istniejących obecnie ([1.1] oraz [1.2]). Tak duże energie zderzeń są niezbędne do obserwacji rzadkich procesów fizycznych, na przykład produkcji bozonu Higgsa, która jak dotąd przewidziana jest jedynie przez teorię.

Wysoka świetlność i duża częstość oddziaływań (wiązki protonów zderzające się co 25ns), jak również geometria i fizyczne rozmiary detektorów wymagające dużej ilości kanałów odczytowych stawiają nowe wymagania elektronice front-end. Wysoka częstość zderzeń wraz z dużą liczbą kanałów detektora zaowocuje olbrzymią ilością danych osiągającą wartości rzędu terabajtów na sekundę. Wielokanałowe układy odczytowe zawierające wzmacniacze front-end odpowiedzialne za odbiór i kształtowanie sygnałów z detektorów muszą jednocześnie zapewnić tymczasowe przechowanie informacji z detektora na czas podejmowania decyzji o ewentualnym dalszym odczycie oraz wstępną selekcję i kompresję danych.

Konsekwencją wysokiej świetlności i dużych energii zderzeń cząstek będzie intensywne pole promieniowania produktów zderzeń. Detektory położone w bezpośredniej bliskości punktu zderzeń takie jak detektory torów, w których używane są paskowe detektory krzemowe, będą szczególnie narażone na promieniowanie. W ciągu dziesięciu lat trwania eksperymentu dawki całkowite dla obszarów, w których umieszczony będzie detektor torów osiągną rząd 10 Mrad dla promieniowania jonizującego oraz 2×10^{14} n/cm^2 równoważnej fluencji neutronów o energii 1 MeV. Tak krańcowe warunki wymagają zastosowania w projekcie technologii elektronicznych o podwyższonej odporności na promieniowanie.

Projekty dwóch prototypowych układów scalonych VLSI w odpornej na promieniowanie technologii DMILL zostały rozpoczęte w roku 1996 i były kontynuowane w latach następnych. Opisywane układy scalone bazują na dwóch podstawowych architekturach odczytu (analogowej i binarnej) i spełniają wszystkie wymagania dotyczące układów elektroniki front-end dla paskowych detektorów krzemowych zastosowanych w warunkach eksperymentów na LHC. Wyniki z kolejnych, prototypowych wersji układów scalonych reprezentujących obie architektury odczytu; analogową (układy z serii SCTA) oraz binarną (układy z serii SCTB a później ABCD) były publikowane na bieżąco [1.14]-[1.29]. Projekty zostały ukończone w roku 2001 a w rezultacie powstały dwa układy elektroniki front-end: układ analogowy SCTA128VG [1.19] i układ binarny ABCD3T [1.28] wdrożone do produkcji masowej [1.29].

Rozprawa podsumowuje wkład autora w projektowanie, optymalizację i testowanie analogowych bloków elektroniki front-end, w szczególności przedwzmacniaczy, stopni kształtujących, jak również komparatorów wymaganych w binarnej architekturze odczytu.

Zarówno w układzie SCTA128VG jak i ABCD3T zastosowano szybki przedwzmacniacz transimpedancyjny z bipolarnym tranzystorem wejściowym poprzedzający potrójny stopień całkujący, zapewniający wymagany kształt impulsu i optymalizację stosunku sygnału do szumu. Wybór architektury przedwzmacniacza jak również rodzaju tranzystora wejściowego były podyktowane kompromisem pomiędzy parametrami szumowymi i mocą rozpraszaną przez układ, przy równoczesnym zapewnieniu wymaganego pasma przenoszenia przedwzmacniacza i odporności radiacyjnej układu.

Konieczność zapewnienia odpowiedniego pola wzmocnienia przedwzmacniacza jest omówiona skrótowo w rozdziale pierwszym w kontekście minimalizacji impedancji wejściowej przedwzmacniacza. W rozdziale omówiono również dwie podstawowe konfiguracje wzmacniacza ładunkoczułego stosowane przy odczycie detektorów krzemowych, przedwzmacniacz ładunkowy i transimpedancyjny. Wykazano, że przedwzmacniacz pracujący w konfiguracji transimpedancyjnej zapewnia mniejszą impedancję wejściową i niższe sygnały przesłuchu niż przedwzmacniacz ładunkowy o tym samym stopniu wejściowym. Pokazano, że w przypadku elektroniki front-end o czasie kształtowania impulsów rzędu 20ns projektowanej dla krzemowych detektorów paskowych o pojemnościach całkowitych rzędu 20pF, dla utrzymania sygnałów przesłuchu poniżej 10% pole wzmocnienia stopnia wejściowego powinno być rzędu 1GHz.

W rozdziale przedstawiono również uproszczoną analizę szumową wzmacniacza ładunkoczułego obciążonego na wejściu pojemnością detektora i równoważnymi źródłami szumów, równoległego i szeregowego. Omówiono w skrócie filtry CR-$(RC)^n$ zbudowane ze stopnia różniczkującego i n stopni całkujących. Ze względu na prostotę i efektywność są one powszechnie stosowane w wielokanałowej elektronice front-end dla krzemowych detektorów paskowych, gdzie oprócz parametrów szumowych, następnym ważnym czynnikiem jest niski pobór mocy układu. Kontrybucja szumów szeregowych do równoważnego ładunku szumowego (*ang.: ENC – Equivalent Noise Charge*) jest wprost proporcjonalna do pojemności wejściowej wzmacniacza i odwrotnie proporcjonalna do pierwiastka z czasu kształtowania impulsu. Wkład szumów równoległych jest niezależny od pojemności wejściowej wzmacniacza i wprost proporcjonalny do czasu kształtowania impulsu. W przypadku ogólnym możliwa jest optymalizacja czasu kształtowania impulsu i minimalizacja ENC dla danej pojemności detektora. W przypadku elektroniki dla eksperymentów LHC czas kształtowania impulsu z detektora jest ograniczony wymaganiami rozdzielczości czasowej układu odczytowego podyktowanej częstością zderzeń co 25ns. Optymalizacja szumowa układu front-end polega na minimalizacji wkładów szumów szeregowego i równoległego, to jest doborze typu i parametrów (wymiarów geometrycznych i polaryzacji) tranzystora wejściowego.

Rozdział pierwszy zakończono omówieniem dwóch podstawowych architektur odczytowych stosowanych w układach front-end detektorów krzemowych dla eksperymentów LHC, analogowej i binarnej. Przykładem architektury analogowej jest układ SCTA128VG posiadający 128 kanałów wzmacniaczy front-end i układów kształtujących, analogową linię opóźniającą (ADB) i szybki, analogowy multiplekser wyjściowy. Przykładem architektury binarnej jest układ ABCD3T zaprojektowany dla detektora torów w eksperymencie ATLAS. Posiada on 128 kanałów wzmacniaczy front-end z układami kształtującymi i komparatorami podłączonymi do cyfrowej linii opóźniającej, dodatkową pamięć buforującą typu RAM, oraz układ kompresji danych i

wyjściowy rejestr przesuwny. Oba układy zostały zaprojektowane i wykonane w technologii BiCMOS DMILL odpornej na promieniowanie.

W rozdziale drugim przedstawiono podstawowe zagadnienia związane ze zniszczeniami radiacyjnymi w elementach półprzewodnikowych pracujących w polach promieniowania typowych dla eksperymentów na LHC. W obszarze detektora torów, gdzie zastosowane są krzemowe detektory paskowe, na elektronikę front-end będą oddziaływać; cząstki naładowane powstające w wyniku bezpośrednich zderzeń w akceleratorze, promieniowanie wtórne powstające w reakcjach jądrowych z materiałami konstrukcyjnymi detektora oraz neutrony.

W półprzewodnikach wyróżnia się dwa podstawowe mechanizmy zniszczeń radiacyjnych; zniszczenia jonizacyjne i strukturalne. W zniszczeniach jonizacyjnych energia zaabsorbowana przez warstwy izolacyjne, głównie dwutlenek krzemu, powoduje generację ładunków wytwarzających pasożytnicze pola elektryczne zmieniające charakterystykę przyrządu półprzewodnikowego. Główną rolę odgrywa tu pułapkowanie dziur, które ze względu na wielokrotnie niższą ruchliwość niż elektrony, mają znacznie większą szansę być przechwycone w obszarze tlenku krzemu, budując w ten sposób dodatni ładunek przestrzenny.

W przypadku tranzystorów polowych drugim ważnym czynnikiem jest indukcja stanów powierzchniowych na granicy cienki tlenek – kanał pod wpływem promieniowania jonizacyjnego. Aktualny ładunek stanów powierzchniowych zależy od rodzaju stanu (stany mogą być donorowe i akceptorowe) i jego energii względem poziomu Fermiego. Ponieważ dystrybucja stanów akceptorowych i donorowych nie jest jednorodna (stany akceptorowe ulokowane są blisko pasma przewodnictwa a donorowe blisko pasma walencyjnego) wypadkowy ładunek powierzchniowy dla tranzystorów PMOS i NMOS spolaryzowanych nominalnie jest odpowiednio dodatni i ujemny. Zarówno indukcja stanów powierzchniowych, pułapkowanie dziur w obszarze tlenku krzemu jak i proces odwrotny, czyli uwalnianie dziur pod wpływem wygrzewania i efektu tunelowego, zachodzą z różnymi stałymi czasowymi i są zależne od temperatury. Wypadkowa charakterystyka tranzystora zależeć będzie nie tylko od pochłoniętej dawki promieniowania, ale i od szybkości naświetlania, temperatury i warunków polaryzacji.

W układzie scalonym poddanym promieniowaniu jonizującemu, opisane procesy będą zachodzić zarówno w obszarach cienkiego tlenku pod bramką tranzystora zmieniając jego charakterystykę, jak również w obszarze grubego tlenku, powodując upływy pomiędzy źródłem i drenem tranzystora oraz pomiędzy różnymi tranzystorami. W przeszłości zapewnienie odporności radiacyjnej dla danej technologii CMOS polegało na rozwoju specjalnych technik produkcji „czystego” (z małą ilością pułapek) cienkiego tlenku charakteryzującego się małą gęstością stanów powierzchniowych. Skalowanie technologii CMOS i towarzysząca mu redukcja grubości cienkiego tlenku znacząco poprawia odporność radiacyjną pojedynczych tranzystorów (bardzo duże prawdopodobieństwo efektu tunelowego). Pełna odporność radiacyjna całego układu może zostać zapewniona poprzez odpowiednie stosowanie pierścieni ochronnych i zaprojektowanie masek tranzystorów w geometrii „gate around”, co zapobiega upływom poprzez tranzystory pasożytnicze obecne w obszarach grubego tlenku.

W zniszczeniach strukturalnych padająca cząstka promieniowania przekazuje w zderzeniu z atomem krzemu ilość energii wystarczającą do jego wybicia z sieci krystalicznej. Puste miejsce w strukturze krystalicznej krzemu może zostać wypełnione

przez atom domieszki produkując stabilne centrum generacyjno-rekombinacyjne zmieniające rezystywność krzemu i czas życia nośników mniejszościowych.

Zwiększenie koncentracji pułapek i centrów generacyjno-rekombinacyjnych w zaporowo spolaryzowanych złączach p-n powoduje zwiększenie prądu generacji. W detektorach krzemowych spolaryzowanych zaporowo powoduje to zwiększenie prądu upływu detektora, który jest jednym ze źródeł szumu równoległego. W złączach p-n spolaryzowanych w kierunku przewodzenia, zwiększenie koncentracji centrów generacyjno-rekombinacyjnych wpływa na zwiększenie prądu rekombinacji i zmniejszenie czasu życia nośników mniejszościowych. W tranzystorze bipolarnym, w spolaryzowanym w kierunku przewodzenia złączu baza – emiter powoduje to zwiększenie prądu bazy i w konsekwencji zmniejszenie wzmocnienia prądowego tranzystora. Ponieważ prawdopodobieństwo rekombinacji, a więc wielkość prądu bazy, jest zależne od koncentracji defektów w bazie, z punktu widzenia odporności radiacyjnej tranzystory o mniejszych wymiarach będą bardziej optymalne. Zmniejszanie wymiarów geometrycznych tranzystora pociąga za sobą zwiększenie rezystancji rozproszonej bazy, jednego ze źródeł szumów w tranzystorze wejściowym. Kompromis pomiędzy odpornością radiacyjną a parametrami szumowymi jest podstawą do optymalizacji wymiarów geometrycznych bipolarnego tranzystora wejściowego w omawianych wzmacniaczach front-end.

Prawdopodobieństwo rekombinacji zmniejsza się wraz ze zmniejszeniem czasu przelotu nośników przez bazę, a więc zmniejsza się wraz ze wzrostem szybkości tranzystorów. Dla technologii DMILL oferującej tranzystory bipolarne o częstotliwości granicznej 5GHz, dla dawek promieniowania rzędu 3×10^{14} n/cm^2 wartość wzmocnienia prądowego w tranzystorach stosowanych w stopniach wejściowych przedwzmacniacza (rezystancja rozproszona bazy rzędu 180Ω) utrzymuje się powyżej 40, co jest wartością wystarczającą do poprawnego funkcjonowania wzmacniacza front-end.

Rozdział drugi zakończono omówieniem efektów typu „Single Event Effect” (SEE) powodowanych przez wysokoenergetyczne cząstki deponujące w obszarze układu scalonego ładunek wystarczający do zniszczenia przyrządu półprzewodnikowego lub do zmiany stanu logicznego obwodu cyfrowego.

Rozdział trzeci zawiera analizę szumową wzmacniaczy front-end pracujących w konfiguracji transimpedancyjnej z filtrami CR-(RC)^3. Omówiono optymalizację szumową przedwzmacniaczy zbudowanych zarówno na tranzystorach bipolarnych jak i polowych. Przedstawiono podstawowe źródła szumów w tranzystorach bipolarnych i polowych, ich korelacje i przenoszenie się na wyjście wzmacniacza front-end, a także ich wpływ na równoważny ładunek szumowy (ENC).

W tranzystorze bipolarnym podstawowymi źródłami szumów są: szum śrutowy prądu kolektora, szum śrutowy prądu bazy oraz szum termiczny rezystancji rozproszonej bazy. Szumy śrutowe prądu kolektora i bazy są ze sobą skorelowane, a współczynnik korelacji zależy od częstotliwości. Współczynnik korelacji dla źródeł szumowych prądu kolektora i bazy jest wprost proporcjonalny do częstości kołowej i pojemności baza – kolektor, a więc jest większy dla dużych tranzystorów. Szum śrutowy prądu kolektora i szum termiczny rezystancji rozproszonej bazy są typowymi szumami szeregowymi, których kontrybucja do ENC jest wprost proporcjonalna do pojemności detektora i odwrotnie proporcjonalna do pierwiastka z czasu kształtowania impulsu. Kontrybucja prądu śrutowego kolektora jest dodatkowo związana zależnością odwrotnie proporcjonalną z transkonduktancją tranzystora. Szum śrutowy prądu bazy jest szumem równoległym i jego kontrybucja do ENC nie zależy od pojemności wejściowej, a jest wprost

proporcjonalna do pierwiastka z czasu kształtowania impulsu i wartości prądu bazy. Kontrybucja składnika korelacyjnego do równoważnego ładunku szumowego jest wprost proporcjonalna do pierwiastka z iloczynu pojemności wejściowej wzmacniacza i pojemności baza - kolektor podzielonego przez czas kształtowania impulsu. Jak pokazano, dla prezentowanych wzmacniaczy front-end optymalizowanych pod względem odporności radiacyjnej i pracujących z detektorem o pojemności około 20pF, najbardziej znaczącymi kontrybucjami do ENC są szum termiczny rezystancji rozproszonej bazy, szum śrutowy prądu kolektora i w przypadku niskiego wzmocnienia prądowego (po naświetleniu) szum śrutowy prądu bazy.

Dużym problemem w optymalizacji szumowej tranzystora polowego MOS pracującego w słabej i umiarkowanej inwersji jest poprawne modelowanie jego parametrów elektrycznych, takich jak transkonduktancja, pojemność bramki czy też współczynnik szumów γ w funkcji prądu polaryzacji i wymiarów tranzystora. W pracy oparto się na analitycznym modelu EKV [3.4] zapewniającym poprawną charakteryzację parametrów mało- i wielko-sygnałowych tranzystora MOSFET pracującego w słabej, średniej i silnej inwersji.

Klasyczne modele szumowe dla tranzystora MOSFET uwzględniają: szum termiczny kanału, szum indukowany prądu bramki GIC (*ang.: Gate Inducent Current noise*) skorelowany z szumem termicznym kanału, oraz szum 1/f. Ten ostatni związany jest z pułapkowaniem i uwalnianiem ładunków na granicy cienki tlenek - kanał. Jego widmowa gęstość mocy zależy od rodzaju technologii i typu tranzystora i jest odwrotnie proporcjonalna do częstotliwości (stąd nazwa) oraz powierzchni bramki i kwadratu pojemności jednostkowej bramki. Poziom tego szumu może się wahać dla różnych okresów produkcji i zwykle zwiększa się po naświetlaniu, co wynika z indukowania dodatkowych stanów powierzchniowych. Do określenia wpływu szumów 1/f na ENC należy użyć parametrów dla największego obserwowanego poziomu szumów dla danej technologii.

Szum termiczny kanału jest szumem szeregowym a jego kontrybucja do ENC jest odwrotnie proporcjonalna do pierwiastka z transkonduktancji tranzystora i czasu kształtowania impulsu i wprost proporcjonalna do pojemności wejściowej wzmacniacza (włączając w to pojemność detektora i pojemność bramki tranzystora). Pomimo że zastępcze źródło prądowe szumu GIC jest umieszczone w obwodzie bramki tak jak typowe źródło szumu równoległego to, ponieważ jego gęstość widmowa zależy od częstotliwości (prąd jest indukowany przez ruchy termiczne ładunków w kanale poprzez pojemność bramka – kanał), jego końcowy wpływ na ENC ma charakter podobny jak szumu szeregowego. Kontrybucja szumów GIC do równoważnego ładunku szumowego jest odwrotnie proporcjonalna do czasu kształtowania impulsu i transkonduktancji tranzystora i nie zależy od pojemności wejściowej wzmacniacza a tylko od pojemności bramki tranzystora wejściowego. Kontrybucja składnika korelacyjnego szumów termicznych i szumu GIC jest wprost proporcjonalna do pierwiastka z iloczynu pojemności wejściowej wzmacniacza i pojemności bramki tranzystora i odwrotnie proporcjonalna do pierwiastka z transkonduktancji i czasu kształtowania impulsu.

Zarówno w przypadku wzmacniaczy z tranzystorami bipolarnymi jak i polowymi, szumy szeregowe, które są odwrotnie proporcjonalne do transkonduktancji przyrządu, stanowią znaczące kontrybucje do równoważnego ładunku szumowego. W celu minimalizacji ENC konieczne jest więc zwiększanie transkonduktancji przyrządu przez zwiększanie prądu (tranzystor bipolarny) lub poprzez zwiększanie prądu i wymiarów geometrycznych (tranzystor polowy). W przypadku tranzystora bipolarnego

optymalizacja ENC poprzez zwiększanie prądu kolektora jest limitowana wzrostem szumów równoległych od prądu bazy i stałą kontrybucją od szumów szeregowych rezystancji bazy. Dla tranzystora polowego zwiększanie transkonduktancji i optymalizacja ENC poprzez zwiększanie szerokości tranzystora jest ograniczona zwiększaniem się pojemności bramki dodającej się do całkowitej pojemności wejściowej wzmacniacza. W obu przypadkach maksymalny prąd tranzystora wejściowego jest określony przez maksymalną moc rozpraszania układu front-end, będącą obok odporności radiacyjnej i parametrów szumowych podstawowym czynnikiem określającym wybór typu tranzystora wejściowego dla prezentowanych wzmacniaczy. Jak pokazano w rozdziale trzecim, w przypadku technologii DMILL przedwzmacniacz z wejściowym tranzystorem bipolarnym jest w stanie zapewnić przy zadowalającej odporności radiacyjnej zarówno mniejszą moc rozpraszania jak i lepsze parametry szumowe układu niż przedwzmacniacz zbudowany na tranzystorze polowym.

Rozdział czwarty opisuje szczegółowo architekturę i działanie wzmacniaczy front-end zastosowanych w układach scalonych SCTA128VG i ABCD3T, skupiając się na ich parametrach szumowych i porównując wartości zmierzone z modelami wyprowadzonymi w rozdziale trzecim. Obok wzmacniaczy front-end wykonanych w technologii DMILL przedstawiono również projekt układu ABCDS-FE zaprojektowanego i wykonanego w technologii submikronowej CMOS IBM 0.25μm. W układzie tym uzyskano parametry analogowe porównywalne z parametrami układów zbudowanych na tranzystorach bipolarnych.

Zarówno w układzie ABCD3T jak i w SCTA128VG zastosowano ten sam przedwzmacniacz zbudowany w oparciu o wejściowy tranzystor bipolarny o wymiarach 10μm × 1.2μm, charakteryzujący się rezystancją rozproszoną bazy w granicach 180Ω, obciążony źródłem prądowym zbudowanym na tranzystorze PMOS. Wysoka rezystancja wyjściowa tranzystora bipolarnego zapewnia duże wzmocnienie w otwartej pętli bez konieczności stosowania układu kaskodowego. Prosta konfiguracja przedwzmacniacza umożliwia uzyskanie dużego pola wzmocnienia (około 1GHz) niezbędnego w celu zapewnienia niskiej impedancji wejściowej układu. Sygnał z przedwzmacniacza jest wzmacniany i wstępnie kształtowany na dwutranzystorowym wzmacniaczu z silnym sprzężeniem zwrotnym zapewniającym dobrą stabilizację punktu pracy układu i całkowite wzmocnienie impulsowe przedwzmacniacza w granicach 17mV/fC. Wymagane wzmocnienie końcowe układów front-end, w granicach 50mV/fC, uzyskiwane jest w następnych stopniach. W przypadku układu SCTA128VG jest to replika drugiego stopnia przedwzmacniacza. W przypadku układu ABCD3T jest to wzmacniacz różnicowy sprzężony AC z przedwzmacniaczem i będący jednocześnie pierwszym stopniem komparatora.

Porównując parametry szumowe mierzone dla układów SCTA128VG i ABCD3T z modelami wyprowadzonymi w rozdziale trzecim, uwzględniono dodatkowe źródło szumów pochodzących od rezystora w sprzężeniu zwrotnym przedwzmacniacza i odstępstwa charakterystyki częstotliwościowej rzeczywistych układów od zakładanego typu filtru CR-$(RC)^3$. Odstępstwa od idealnej charakterystyki filtru wynikają głównie ze skończonego pasma przenoszenia przedwzmacniacza i użytych sprzężeń typu AC pomiędzy poszczególnymi stopniami obwodów. Poprawki dla szumów szeregowych i równoległych obliczone dla obu układów są niewielkie i wahają się w granicach od 1.5% do 6%, co uzasadnia przybliżenie rodzaju filtru dla potrzeb analizy przedstawionej w rozdziale trzecim.

Parametry analogowe układów SCTA128VG i ABCD3T takie jak liniowość, czas kształtowania impulsu, zakres dynamiczny i poziom szumów spełniają wszystkie założenia projektowe. Czas kształtowania impulsu z detektora dla nominalnej pojemności wejściowej układu (18pF) wynosi około 20ns. Dobra liniowość (błąd nieliniowości całkowej mniejszy od 5%) jest utrzymana w całym zakresie dynamicznym układów (16fC).

Mały wpływ pojemności wejściowej wzmacniacza na czas kształtowania impulsu (około 0.1ns na pF) potwierdza niską impedancję wejściową wzmacniacza. Równoważny ładunek szumowy dla pojemności wejściowej 18pF wynosi około 1500e^-. Zmierzone wartości ENC dla różnych pojemności wejściowych układu nie odbiegają od wartości przewidywanych przez analizę przeprowadzoną w rozdziale trzecim o więcej niż ±50e^-, co potwierdza dobrą zgodność modelu z rzeczywistością. Zarówno układ SCTA128VG jak i ABCD3T były testowane pod względem odporności radiacyjnej. Po dawkach promieniowania ekwiwalentnych do 10Mrad promieniowania jonizacyjnego i fluencji neutronów 1MeV 2×10^{14} n/cm^2 (równoważne 10 latom pracy w eksperymencie ATLAS) parametry analogowe są utrzymywane w wymaganych granicach.

W rozdziale czwartym, obok wzmacniaczy bipolarnych, zaprezentowano przykład wzmacniacza front-end zaprojektowanego i wykonanego w technologii CMOS IBM 0.25μm z polowym tranzystorem wejściowym. Przedwzmacniacz transimpedancyjny zbudowany na buforowanym stopniu kaskody pracuje z aktywną pętlą sprzężenia zwrotnego wykorzystującą tranzystor NMOS pracujący w nasyceniu [4.3]. Wybór tej konfiguracji przedwzmacniacza podyktowany został koniecznością poszerzania pasma układu (technologia IBM oferuje tylko niskoomowe rezystory polikrzemowe o stosunkowo dużych pojemnościach pasożytniczych). Aczkolwiek parametry analogowe tego przedwzmacniacza takie jak pasmo, czas kształtowania impulsu i impedancja wejściowa nie odbiegają od wersji bipolarnej, a poziom szumów wejściowych może być nawet niższy, należy pamiętać, że uzyskuje się to kosztem wyższych prądów polaryzacji układu.

W rozdziale piątym omówiono problemy wynikające z integracji na jednym podłożu układu scalonego analogowych wzmacniaczy front-end o dużej czułości i szybkich bloków cyfrowych CMOS. Opisano metody poprawiające parametr PSRR (*ang.: Power Supply Rejection Ratio*) jak również metody rysowania masek układu i pierścieni ochronnych, poprawiające separację obwodów analogowych i cyfrowych i przeciwdziałające przenoszeniu się zakłóceń poprzez elementy pasożytnicze oraz wspólne podłoże układu scalonego.

Nieróżnicowa architektura stopnia wejściowego podyktowana optymalizacją parametrów szumowych przedwzmacniacza i zmniejszaniem mocy rozpraszanej w układzie nie jest idealna z punktu widzenia PSRR. Używanie wspólnych linii zasilających i polaryzujących dla poszczególnych stopni układu otwiera drogę do przenoszenia się zakłóceń z części cyfrowych układu do czułych analogowych stopni wejściowych. W celu minimalizacji tych efektów należy zapewnić odsprzęganie linii polaryzacyjnych do odpowiednich linii masy lub zasilania układu. Przy rysowaniu masek układu należy pamiętać o ekranowaniu linii polaryzacyjnych, przy czym ekrany należy podłączać odpowiednio do masy lub zasilania układu, ograniczając możliwość tworzenia się dzielników pojemnościowych pogarszających parametr PSRR. Używanie różnicowej architektury w dalszych stopniach układu (komparator w układach ABCD3T i ABCDS-FE), gdzie możliwa jest praca z małymi prądami polaryzacji, polepsza odporność układu na zakłócenia rozchodzące się po liniach zasilających. Stosowanie zarówno odsprzęgania

linii polaryzacji oraz architektury różnicowej sprzężonej pojemnościowo (stałe czasowe rzędu 200ns – 300ns) ze stopniami poprzednimi zapewnia dobre tłumienie zakłóceń w pełnym zakresie częstotliwości.

W rozdziale tym zwrócono również uwagę na to, że część pojemności wejściowej detektora krzemowego jest zamknięta do wspólnej masy płytki zawierającej zarówno układy front-end jak i detektor. Jakiekolwiek zakłócenie pojawiające się pomiędzy masą detektora a masą przedwzmacniacza połączoną z emiterem tranzystora wejściowego jest wzmacniane tak samo jak sygnał detektorowy. Dlatego też niezbędne jest zapewnienie dobrego połączenia masy detektora z masą analogową przedwzmacniacza, zarówno na poziomie projektu płytki jak i układu front-end (np. emitery tranzystorów w układach SCTA128VG i ABCD3T są połączone oddzielnymi liniami masy mającymi osobne podłączenia do masy płytki).

Omówiono również podstawowe problemy minimalizacji zakłóceń przenoszących się z części cyfrowych do obwodów analogowych w układach zaprojektowanych w technologii DMILL. Technologia DMILL jest technologią typu SOI (*ang.: Silicon On Insulator*). Na podłożu krzemowym pełniącym rolę nośnika mechanicznego naniesiona jest jednomikrometrowa warstwa epitaksjalna krzemu oddzielona warstwą tlenku krzemu i stanowiąca podłoże dla tworzonych elementów. Elementy tworzone na warstwie epitaksjalnej są izolowane od siebie płaszczami ochronnymi z tlenku krzemu. Aczkolwiek budowanie pierścieni ochronnych, wykorzystujących niskoomowe warstwy zagrzebane podłączane do masy lub zasilania układu, zapobiega przenoszeniu się zakłóceń poprzez izolacyjne płaszcze ochronne, to możliwe jest ciągle wstrzykiwanie pasożytniczych sygnałów z części cyfrowych do podłoża układu. Ponieważ w technologii DMILL, tak jak w każdej technologii SOI, nie ma możliwości polaryzacji podłoża, zakłócenia wstrzyknięte z części cyfrowej filtrowane są przez rezystancje i pojemności rozproszone rozchodząc się praktycznie po całym podłożu układu scalonego. Najbardziej czułymi punktami prezentowanych układów front-end są wejściowe pola kontaktowe z pasożytniczymi pojemnościami do podłoża rzędu 250fF. Zmodyfikowana wersja standardowego pola kontaktowego stosująca warstwę ekranującą wykonaną z niskoomowej warstwy zagrzebanej połączonej z masą analogową przedwzmacniacza skutecznie przeciwdziała przenoszeniu się zakłóceń z podłoża do wejścia układu.

Rozdział szósty podsumowuje wyniki pomiarów modułów krzemowych detektorów paskowych zbudowanych w oparciu o analogowe i binarne układy SCTA128VG i ABCD3T, demonstrując efektywność zastosowanych technik projektowych, zarówno na poziomie struktury obwodów jak i na poziomie topografii masek układów scalonych.

W przypadku modułów zbudowanych w oparciu o układy SCTA128VG dodatkowym czynnikiem mogącym pogorszyć efektywne parametry szumowe jest niejednorodność pamięci analogowej zbudowanej w technice przełączanych pojemności. Rozrzut poziomów sygnałów jest spowodowany głównie przez niejednorodność pasożytniczego wstrzykiwania ładunku z linii zapisujących i odczytowych do pojemności pamięci poprzez klucze analogowe zbudowane na tranzystorach polowych. W układach SCTA128VG rozrzut piedestałów w pamięci analogowej utrzymuje się w granicach 1.1mV rms, co dla wzmocnienia układu 45mV/fC jest równoważne około $150e^-$ ENC nieskorelowanych z ENC przedwzmacniacza. Dla nominalnej pojemności detektora 18pF jest to wielkość zaniedbywalna. W rozdziale zademonstrowano działanie kompletnego modułu z dwoma detektorami krzemowymi o całkowitej długości pasków 13cm. Układ SCTA128VG jest używany w eksperymencie NA60, przy testowaniu detektorów diamentowych oraz przy kwalifikacji produkcji detektorów dla eksperymentu ATLAS.

Jak wspomniano, głównym zastosowaniem układów ABCD3T jest detektor torów w eksperymencie ATLAS. W rozdziale pokazano wyniki testów prototypowego dwustronnego modułu detektorowego o długości 13cm (1536 kanałów elektroniki front-end). Średni poziom ENC waha się w granicach 1500e^- spełniając tym samym wymagania projektowe dotyczące parametrów szumowych układu. Zademonstrowano również działanie sektora zbudowanego z 9 modułów detektorowych, umieszczonych na prototypowej wersji cylindra symulującego docelową konfigurację centralnego detektora torów. Różnice w poziomach szumów modułów działających wspólnie na sektorze, w porównaniu do modułów działających osobno, wahają się maksymalnie co najwyżej o ±50e^-, co mieści się w granicach błędu pomiarowego i potwierdza możliwość zastosowania układu w rzeczywistych warunkach eksperymentu.

W dodatkach umieszczono metody obliczeniowe równoważnego ładunku szumowego dla wzmacniacza bipolarnego i zbudowanego na tranzystorze polowym oraz metodę pomiaru rezystancji rozproszonej bazy.

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Introduction

This thesis describes development of fast, radiation-hard Front-End (FE) electronics for readout of silicon strip detectors to be used in the experiments built around the LHC (Large Hadron Collider) machine.

The Large Hadron Collider is a new accelerator being built at CERN near Geneva in order to collide protons with the energy of 14TeV - such high collision energies have never been achieved before ([1.1] and [1.2]). High luminosity together with high rate of interactions (bunches of protons cross each other every 25ns) brings new requirements for the detectors developed for the LHC experiments. The readout electronics built for LHC experiments has to cope with a huge amount of physical data coming from the detectors. Multi-channel readout chips containing FE amplifiers and signal processing circuits also have to provide temporary data storage during the latency of the first-level trigger decision and the preliminary selection of data to be sent out from the detector for further analysis after the first-level trigger. In addition to that, all on-detector components have to stand high radiation levels, up to 10Mrad Total Ionising Dose (TID) and particle fluencies up to 2×10^{14} n/cm^2 1MeV equivalent during 10 years of operation of the experiment.

The development of two demonstrator chips in radiation hard DMILL technology was started in 1996 and continued for several years. These two demonstrators implement two basic readout architectures (analogue and binary) and satisfy all specifications for readout of long strip silicon detectors at LHC experiments. The results from the successive prototypes of the analogue SCTA family of chips, the binary SCTB and later the ABCD line of chips have been published in a number of papers [1.14]-[1.29]. The development was completed during the year 2001 and yielded two final prototypes of the readout chips, namely the analogue SCTA128VG chip [1.19] and the binary ABCD3T chip [1.28] ready for mass production [1.29].

The thesis summarises the results of the author's work on the design, optimisation and evaluation tests of the analogue blocks of the FE chips, namely the preamplifiers, noise filtering stages (shapers) as well as the comparators required in the binary readout architecture.

Both the SCTA128VG and ABCD3T chip designs, employ fast bipolar transimpedance preamplifiers followed by triple integrators providing the noise filtration function. The choice of the final architecture, as well as the type of the device used in the input stage, was dictated by the trade-off between noise performance and the power consumed by the amplifier, while at the same time achieving the required gain-bandwidth product and radiation hardness of the design. The importance of driving up the gain and bandwidth of the preamplifier will be reviewed briefly in the context of minimizing the preamplifier input impedance and susceptibility to the capacitive load. The other two issues driving the final choice of the front-end architecture, namely the radiation hardness and the noise performance of amplifiers built with bipolar and CMOS devices, will be discussed in Chapters 2 and 3.

Chapter 4 describes in detail the architectures and performance of the front-end amplifiers employed in the SCTA128VG and ABCD3T chips, focusing on the noise figures and comparing measurements with the noise models developed in Chapter 3. Besides the DMILL versions of the amplifiers it also presents the design and test results of the successor ABCDS/FE chip, which has been implemented in a modern deep submicron CMOS technology.

Chapter 5 covers problems related to the mixed-mode nature of the front-end electronics and the integration of the sensitive bipolar analogue circuits with the CMOS digital logic on the same chip substrate. Moreover, it deals with the system issues and techniques for preventing the degradation of the performance in the real multi-channel system.

Chapter 6 summarises the test results of the fully populated detector modules built with SCTA128VG and ABCD3T chips and shows the effectiveness of the applied layout techniques and overall design methodology.

1. Silicon strip detectors for tracking applications

The principal requirement for tracking detectors for High Energy Physics (HEP) experiments is the measurement of the position and the time of passage of particles without disturbing their track [1.3]. Relativistic charged particles traversing matter loose energy through atomic collisions and generate electron hole pairs along their track. An electric field applied in the detector volume drifts the generated charge towards the electrodes and induces a current signal that is read out by the front-end electronics.

The main advantage of semiconductor detectors over other types of detectors is the possibility of achieving very good spatial resolution. For silicon strip detectors with intermediate strip and analogue readout a spatial resolution better than 1μm can be obtained [1.30]. Another important advantage is that production of semiconductor detectors can profit from a number of industrial technologies that have been developed by the microelectronics industry.

1.1. The principles of silicon strip detectors

All present-day semiconductor detectors are based on the reverse biased p-n junction. The space charge region of the reverse biased p-n junction (also named the depletion zone) forms the detection volume. The electric field produced by the externally applied bias voltage ensures collection of the created charges on the electrodes and thereby produces a current signal. The thermally generated carriers in the depletion zone result in a leakage current, sometimes called the dark current. This is an important source of noise and lowering it is one of the key issues in the design of detectors. For tracking applications the most widely used material is silicon, which provides reasonable values of dark current even at room temperature.
The width of the depletion zone depends on the concentration of n-type and p-type dopands i.e. on the resistivity of the material. For the non-uniformly doped junction of a p+ region on lightly doped n-type material one finds the following dependence of the width of the depletion zone d as a function of the bias voltage V_B, the resistivity of n type material ρ_n, the electron mobility μ_e and the permittivity of silicon ε

$$d = \sqrt{2 \cdot \varepsilon \cdot \rho_n \cdot \mu_e \cdot V_B} \qquad (1.1)$$

Evaluating equation (1.1) for silicon with resistivity of the order of a few kΩcm shows that it is possible to achieve a 300μm depletion zone for a bias voltage in the range of 50 to 90V.

The signal created by a high-energy particle in a 300μm thick, fully depleted silicon detector has a Landau distribution with the most probable value around 22500e^-. For a 300μm thick fully depleted silicon detector the collection time, i.e. the width of the current pulse to be readout by the electronics, is typically of the order of a few nanoseconds. The charge collection time depends on the electrical properties of the semiconductor material, the detector thickness, as well as on the applied bias voltage. Working with bias voltages higher than the full depletion voltage (over-depleted detectors) can reduce the charge collection time significantly, however increasing the bias voltage might lead to higher dark current and an increase of noise.

In practice the silicon detector thickness can vary between 100 to 500μm depending on the application. These boundaries are determined by the mechanical properties of silicon

(minimum achievable thickness for large detector area) as well as on the maximum affordable charge collection time, which is longer for thicker detectors.

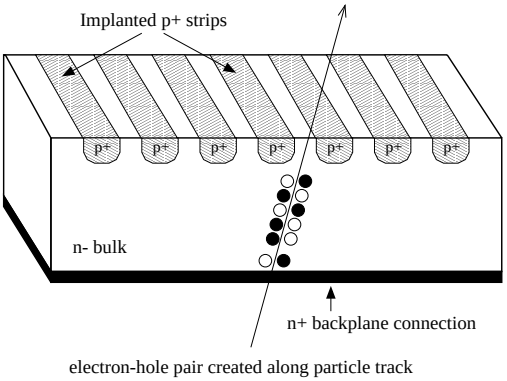


Figure 1.1: Schematic structure of single-sided silicon strip detector. The bias voltage is applied on the detector backplane.

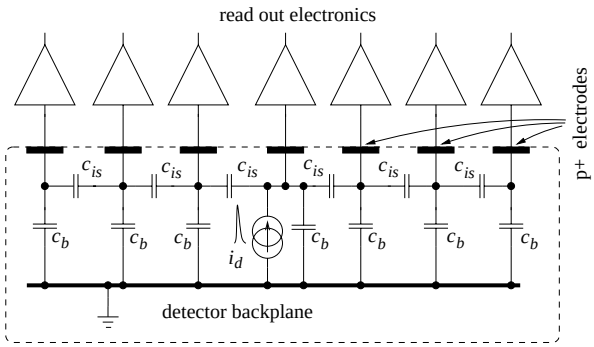


Figure 1.2: Equivalent schematic of the silicon strip detector with the read out electronics connected to each p+ strip. Current source i_d represents signal induced by the charge collected on one detector strip.

As mentioned above, one of the advantages of silicon detectors is the use of manufacturing technologies developed by the microelectronics industry. Standard photolithographic processes allow the segmentation of the detecting area of one silicon crystal into several diodes. These diodes are readout separately in order to obtain the spatial information about the trajectory of the detected particle. Figure 1.1 shows a schematic of the structure of a Silicon Strip Detector (SSD). The p+ diode strips with contacts to the readout electronics are implanted on n type lightly doped silicon material. The bias voltage is applied to the detector backplane. The p+ strips are connected to the readout electronics. Two types of connection are possible. A simple DC connection requires the front-end electronics to be able to supply the detector leakage current from the input of the readout amplifier. A high level of dark current will cause not only a higher level of noise but could result in the total malfunctioning of the readout amplifier connected to the leaking strip. The second type of connection uses AC coupling; this option requires extra processing steps in the manufacturing of the detector in order to provide the DC bias for the readout strips (high value resistors) and the capacitors for coupling the implanted diodes to the read out electronics.

The total capacitance associated with single detector diode depends on the detector geometry, which determines the electric field distribution as well as the detector's thickness. Figure 1.2 shows a simplified equivalent schematic of a silicon strip detector connected to read out electronics. The current source i_d represents the signal generated and collected by one of the detector segments. The capacitive network, consisting of inter-strip capacitances c_{is} and capacitances c_b to the detector backplane, represents the main parasitic components of the silicon strip detector. As one can see, the input of an individual read out amplifier will be loaded with the capacitance to the backplane and two inter-strip capacitances with the neighbouring channels. Assuming low input impedance of the front end electronics, which is in fact required to efficiently collect all created charges[1], the total capacitance loading the individual amplifier input will be the sum of two inter-strip capacitances and the capacitance to the detector backplane.

[1] The problem of signal cross-talk related to the finite input impedance of the read out amplifiers is discussed later.

The front-end electronics presented in this thesis is optimised for silicon strip detectors with total capacitance of around 20pF. Nevertheless, it can also be used for the readout of different types of silicon detectors with capacitances ranging from 0 to roughly 30pF.

Depending on the detector geometry and the number of diodes to be read out, the front-end chips developed for silicon strip detectors typically contain up to 128 electronics channels.

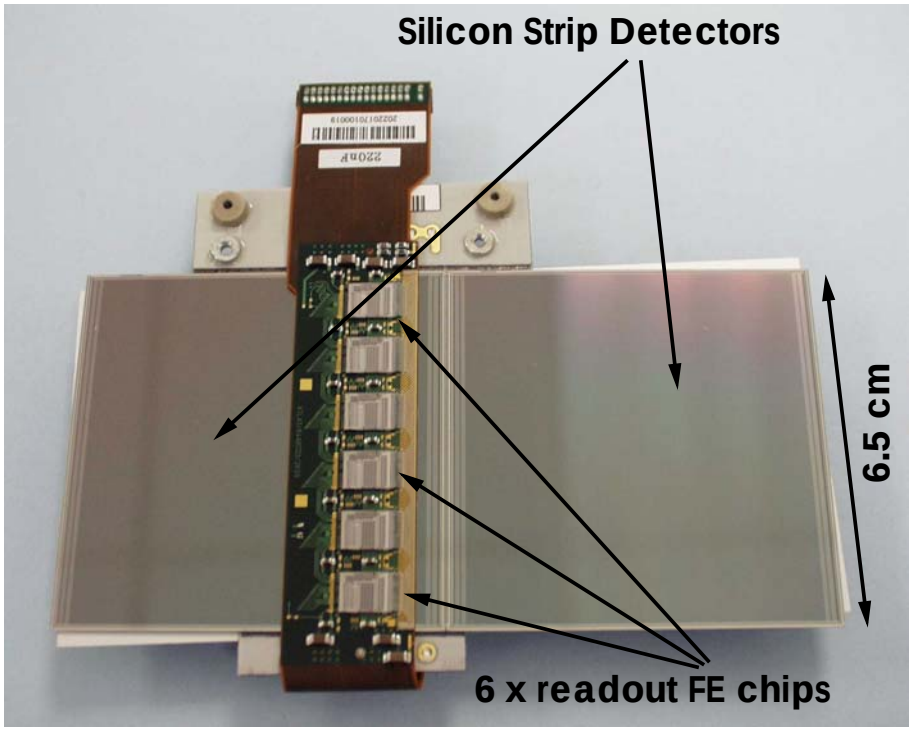


Figure 1.3: Example of a Silicon Strip Detector module built for the ATLAS experiment at LHC. The module consists of four 6.5×6.5cm Silicon Strip Detectors (2 daisy chained per side) read out by twelve 128 channel front-end chips (in total 768 readout channels per side).

Figure 1.3 shows an example of detector module built for the ATLAS experiment at the LHC. It consists of four silicon strip detectors of type p^+-on-n substrate. The dimensions of each silicon crystal are: 6.5cm width, 6.5cm length and 285μm thickness. Two pairs of daisy-chained detectors (total length of the strips 13cm) are placed back-to-back and tilted by an angle of 40mrad in order to obtain two-dimensional information about the particle track. The detector strips are laid out with a pitch of 80μm, which results in a spatial resolution of the order of 20μm rms. Six 128-channel front-end chips are used to read out the 768 strips of each side of the detector module. The capacitance of a strip to the detector backplane is of the order of 0.3pF/cm. The capacitance of a strip to all neighbours before irradiation is about 1.03pF/cm. After ten years of operation of the ATLAS experiment, corresponding to a fluence of 2×10^{14} neutron/cm^2 and a 10 Mrad dose of gamma radiation, it is expected that this latter capacitance will increase to 1.4pF/cm. Thus the total capacitance of a 13cm daisy-chained strip will be of the order of 18pF before irradiation and 22pF after a full radiation dose at the end of the ATLAS experiment. The charge collection time before and after irradiation is less than 10ns. The expected most probable value of the charge signal from the detector is about 21000e^- (3.4fC). As already mentioned, the front-end readout electronics presented in this thesis is optimised for this range of the detector capacitances and signal parameters.

1.2. Reception of signals from silicon detectors

The collection of the charge deposited in the detection volume depends on its location with respect to the electrodes. Hence the pulses from the sensor vary in their shape and in their delays with respect to passage of the particle. For the tracking application the important information is carried by the quantity of the deposited charge, and therefore the readout electronics must integrate that charge with a time constant longer that the possible range of variation in the shape of the detector current pulses. The processing of the detector signals is also important for the optimisation of the noise performance of the front-end amplifier chain. Provided that the time constant of the band-pass filters used for noise filtering and signal shaping is longer than the charge collection time, one can neglect the distribution of the input charge in time and denote the detector signals as Dirac delta pulses. This approach simplifies the mathematical analysis of the front-end amplifier, which is always a first step in the chip design process.

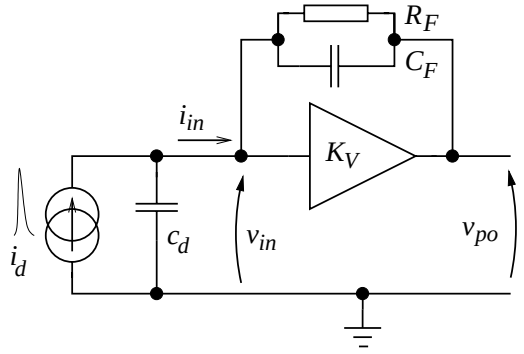


Figure 1.4: Basic configuration of the charge sensitive amplifier.

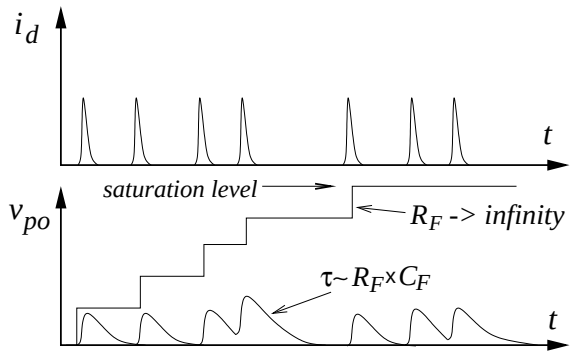


Figure 1.5: Responses of the charge sensitive amplifier to the current pulses for various values of feedback resistor R_F.

The basic configuration of the charge sensitive amplifier is shown in Figure 1.4. It consist of an amplifier working in integrator configuration with the feedback capacitor C_F. The charge accumulated on the feedback capacitor has to be discharged, otherwise the preamplifier stage will be quickly saturated by pulses received from the detector (see Figure 1.5). The decay of the preamplifier output voltage v_{po} is provided by the feedback resistance R_F discharging the C_F with the time constant $\tau_f = C_F \times R_F$. The responses of the charge sensitive amplifier for high and low value of feedback resistor R_F, for the series of signal pulses are shown in Figure 1.5.

Assuming an ideal amplifier of infinite gain and bandwidth, the response of the preamplifier to a Dirac delta pulse is an instantaneous voltage step with an amplitude equal to the quantity of charge divided by the feedback capacitance C_F. In reality, the amplifier has a finite gain K_V and limited bandwidth, which obviously has an impact on the response of the preamplifier. In first approximation the frequency characteristic of the amplifier can be described by a single-pole function as following:

$$K_V(s) = \frac{K_V}{1 + s \cdot \tau_{P0}} \tag{1.2}$$

The time constant τ_{P0} represents the dominant pole of the amplifier and K_V is the gain at low frequencies. Summing the currents at the preamplifier input one obtains following expression for the response to the Dirac delta charge pulse:

$$v_{po}(s)=\frac{Z_F(s)}{1+\frac{1}{K_V(s)}+\frac{s\cdot c_d\cdot Z_F(s)}{K_V(s)}} \cong \frac{Z_F(s)}{1+\frac{s\cdot c_d\cdot Z_F(s)}{K_V(s)}} \tag{1.3}$$

The feedback impedance Z_F is described as following:

$$Z_F(s)=\frac{R_F}{1+s\cdot\tau_f} \qquad \text{where} \quad \tau_f=R_F\cdot C_F \tag{1.4}$$

The general solutions of the Laplace original (1.3) in the time domain can be transformed to three expressions describing the behaviour of the preamplifier with regard to the phase shift of the feedback loop. Depending on the sign of the variable D described in expression (1.8) the response of the preamplifier can be asymptotic (expressions (1.5) & (1.7)) or periodical (1.6) when the preamplifier is on the edge of oscillation.

$$v_{po}(t)=A\cdot\frac{e^{\frac{-t}{B}}\cdot\sinh\left(t\cdot\sqrt{D}\right)}{\sqrt{D}} \qquad \text{for } D>0 \tag{1.5}$$

$$v_{po}(t)=A\cdot\frac{e^{\frac{-t}{B}}\cdot\sin\left(t\cdot\sqrt{-D}\right)}{\sqrt{-D}} \qquad \text{for } D<0 \tag{1.6}$$

$$v_{po}(t)=A\cdot e^{\frac{-t}{B}}\cdot t \qquad \text{for } D=0 \tag{1.7}$$

Where

$$A=\frac{K_V}{c_d\cdot\tau_{P0}} \quad B=\frac{2\cdot\tau_{P0}}{1+\frac{C_F}{c_d}\cdot K_V} \quad D=\frac{\left(\tau_D+\tau_f\cdot K_V\right)^2-4\cdot\tau_D\cdot\tau_{P0}\cdot K_V}{\left(2\cdot\tau_D\cdot\tau_{P0}\right)^2} \quad \tau_D=R_F\cdot c_d \tag{1.8}$$

For the extreme case of the asymptotic response of the preamplifier working with pure capacitive feedback, the circuit responds with the voltage step of amplitude and rise time given by the following equation:

$$v_{po}(t)=\frac{1-e^{\frac{-t\cdot 2}{B}}}{\frac{c_d}{K_V}+C_F} \qquad \text{where} \qquad B=\frac{2\cdot\tau_{P0}}{1+\frac{C_F}{c_d}\cdot K_V} \tag{1.9}$$

From this example one can see the importance of driving up the gain and the bandwidth of the amplifier in order to obtain a fast response of the amplitude independently of the capacitive load c_d of the detector. Figure 1.6 shows the response of the preamplifier working with capacitive feedback to a 1fC input charge for different values of the detector capacitance. The parameters of bandwidth and gain of the amplifier used in the example have been taken from the CMOS cascode amplifier presented later in the thesis. The cascode amplifier implemented in IBM 0.25µm CMOS technology has an open loop gain of around 14000[V/V] (83dB) and the dominant pole is about 800kHz (τ_{P0}=200ns) (roughly 800MHz gain-bandwidth product - GBP). The operation of this amplifier is compared with a hypothetical design having modified bandwidth and open loop gain parameters in order to analyse their impact on the performance of the circuit.

As one can see the rise time of the response depends on the capacitive load and preamplifier gain-bandwidth product. The preamplifiers with the same gain-bandwidth product respond with the same speed, however the higher gain provides a higher amplitude of the response, in accordance with the formulae (1.9).

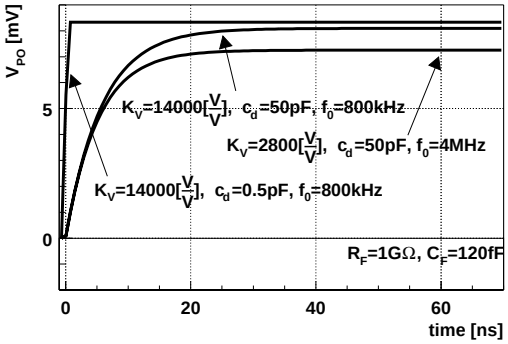


Figure 1.6: Responses of the preamplifier for 1fC signal charge in the case of pure capacitive feedback, various values of gain, amplifier bandwidth and detector capacitance.

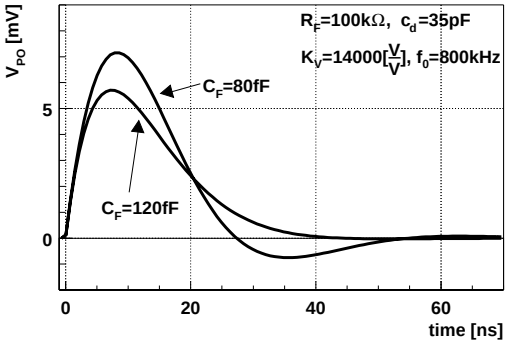


Figure 1.7: Oscillating and asymptotic responses of the preamplifier for various compensation capacitances.

The smaller feedback capacitance C_F offers higher gain of the preamplifier, although in the case of presence of the feedback resistor R_F, increasing the gain may lead to an unstable oscillating response (see Figure 1.7). Therefore for given parameters of the amplifier such as the open loop gain and bandwidth, specified value of R_F and expected detector capacitance, the compensation of the preamplifier is made by increasing the feedback capacitance C_F i.e. by lowering the gain of the preamplifier stage and bringing variable D (equation 1.8) to a positive value.

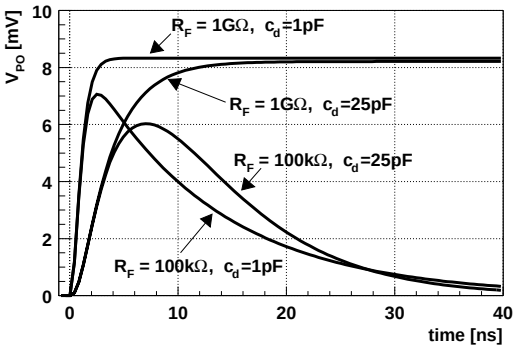


Figure 1.8: Responses of the preamplifier for 1fC signal charge for various values of the feedback resistance and detector capacitances.

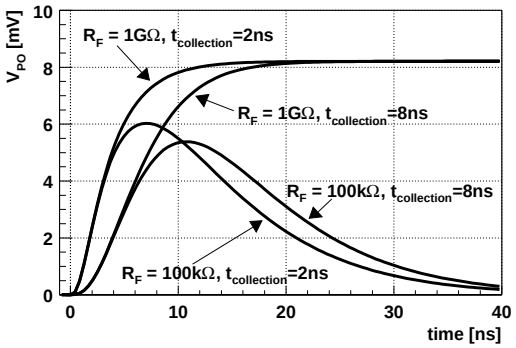


Figure 1.9: Responses of the preamplifier for 1fC signal, loaded with 25pF detector capacitance for various values of charge collection time.

Figure 1.8 shows the response of the preamplifier when it is loaded with various detector capacitances and working either with essentially pure capacitive feedback (C_F=120fF, R_F =1GΩ), or with a 100kΩ feedback resistor in parallel to the 120fF feedback capacitor. The degradation of the response rise time for both preamplifiers loaded with large input capacitances is comparable, however in the case of the resistive feedback there is a loss of gain compared to the capacitive feedback case. Bearing in mind that the final application of these front-end (FE) circuits for the LHC experiments requires high data rates, the

option using a relatively low value of the feedback resistor must be chosen. In this case increasing the speed and open loop gain of the elementary amplifiers is indispensable since it makes the circuit less sensitive to the input capacitance.

The influence of the finite charge collection time on the preamplifier response is shown in Figure 1.9. As can be expected, the slower charge pulse from the detector delays the response of the preamplifier. One can see that for collection times comparable with the feedback time constant τ_f there is further degradation of the pulse amplitude. This effect is known as charge ballistic deficit.

For a 300μm thick fully depleted silicon detector operated under LHC conditions in a magnetic field, it is expected that most of the charge will be collected in less than 8 to 12ns depending on the radiation damages [1.13]. Therefore the optimum shaping for LHC type readout electronics will be somewhere in the range of 20 to 25ns. This will provide reasonable time resolution for consecutive signals from the detector (events occur every 25ns) and will not cause dramatic charge ballistic deficit[2] [1.31].

An important parameter of the preamplifier is the input impedance Z_{in}. It is given by the ratio of the voltage signal at the preamplifier input v_{in} to the preamplifier input current i_{in} (see Figure 1.4). A simple calculation gives the expression for Z_{in} in the operator domain:

$$Z_{in}(s)=\frac{Z_F(s)}{1+K_V(s)}\approx\frac{Z_F(s)}{K_V(s)}=\frac{R_F\cdot(1+s\cdot\tau_{P0})}{K_V\cdot(1+s\cdot\tau_f)} \tag{1.10}$$

Minimization of the preamplifier input impedance is important for two reasons. Together with the detector capacitance c_d the input impedance defines the time constant of the preamplifier response. The influence of the bandwidth and open loop gain on preamplifier response was already discussed using directly expression (1.9).

Another important aspect of lowering the input impedance is related to the cross talk of signals in neighbouring channels. Charge generated in a given strip of the detector will be shared between its readout channel and its two neighbours in the network via the preamplifier input impedance Z_{in} and the two interstrip capacitances c_{is} (see Figure 1.2). Usually the analysis is focused on the characterization of the amplitude of the cross-talk, without paying too much attention to the shape of the parasitic signals. On the other hand, one should keep in mind that the filters applied in order to optimise the noise performance modify the amplitude of the cross-talk signals. To be able to draw general conclusions that can be applied for various implementations of the shaping stages, the whole analysis should be performed in the frequency domain.

Starting from equation (1.10) one can obtain the following expression for the modulus of the input impedance as a function of angular frequency:

$$|Z_{in}|=\frac{R_F}{K_V}\cdot\frac{\sqrt{1+\omega^2\cdot\tau_{P0}^2}}{\sqrt{1+\omega^2\cdot\tau_f^2}} \tag{1.11}$$

Figure 1.11 shows the input impedance as a function of frequency of the amplifier discussed previously and working with two versions of the feedback circuit. It can be seen that important differences exist between those options, especially at low and medium frequencies. The input impedance of the preamplifier working with 100kΩ in the

[2] The ballistic deficit can be lowered by biasing the detector above the depletion voltage, although one has to make a trade off between better charge collection efficiency and increasing the leakage current of the detector.

feedback, at low frequencies depends basically on the open loop gain and resistor value. For medium frequencies one can observe an increase of the input impedance due to limited amplifier bandwidth.
Preamplifiers with this type of input impedance characteristic are described later in the thesis as transimpedance preamplifiers. The preamplifiers working with high values of feedback resistance, where the input impedance for medium frequencies is defined only by the feedback capacitance, are referred to as charge preamplifiers.
One can see that for very high frequencies the input impedance is defined for both types of preamplifiers by the value of the feedback capacitance and the amplifier bandwidth, and is described as follows:

$$\left|Z_{in}^{\omega\to\infty}\right| = \tau_{P0} / \left(K_V \cdot C_F\right) \tag{1.12}$$

In order to evaluate the magnitude of the cross-talk signal in the electronic channel connected to a strip detector, one can assume a basic model of the SSD consisting of three capacitances: capacitance of the strip to the backplane c_b and two interstrip capacitances c_{is} coupling to the closest neighbours (Figure 1.10a).

Figure 1.10b shows the equivalent schematic of two preamplifier stages sharing the charge on the interstrip capacitance c_{is}. It can be seen that the amplitude of the cross-talk normalized to the amplitude of the signal is given by:

$$\left|CrossTalk(j\omega)\right| = \left|\frac{v_{crosstalk}(j\omega)}{v_{signal}(j\omega)}\right| = \left|\frac{Z_{in}(j\omega)}{Z_{in}(j\omega)+Z_{is}(j\omega)}\right| \quad \text{where} \quad Z_{is}(j\omega) = \frac{1}{j\cdot\omega\cdot c_{is}} \tag{1.13}$$

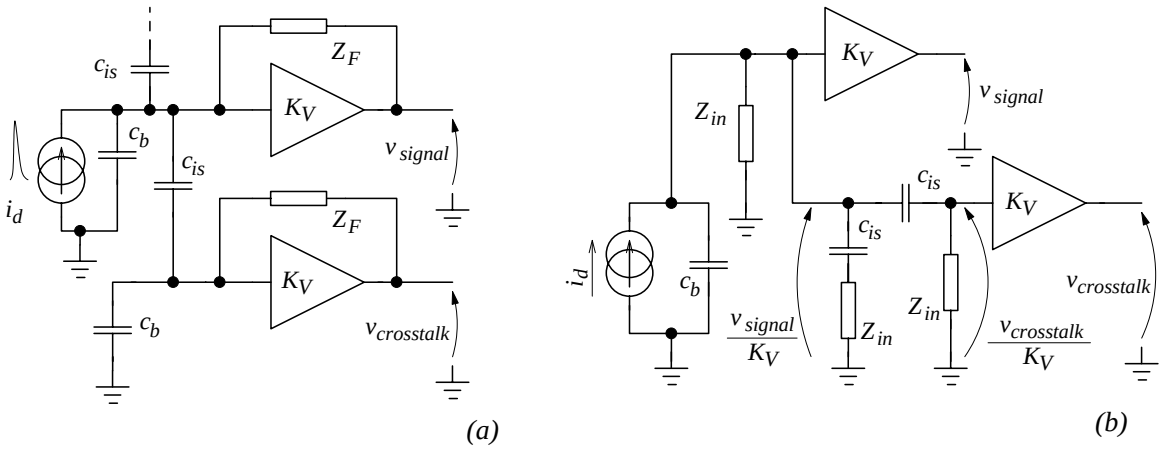


Figure 1.10: Model of charge sharing between preamplifiers connected to the SSD with the signal in one strip of the detector (a) Equivalent schematic of the preamplifier stage coupled to the hit strip with the interstrip capacitance c_{is} (b).

The input impedance $Z_{in}(j\omega)$ can be derived from equation (1.10). Figure 1.12 shows the normalized cross-talk signals as a function of frequency for the charge and transimpedance preamplifiers used in the previous example and for 10pF inter-strip capacitance c_{is}.

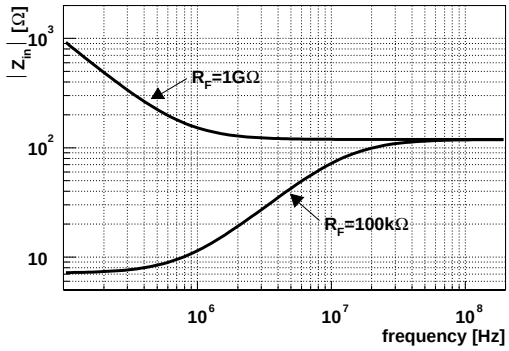


Figure 1.11: Input impedance for charge preamplifier (R_F=1GΩ) and trans-impedance (R_F=100kΩ) preamplifier as a function of frequency. The open loop gain of the elementary amplifier is 83dB with τ_{P0}=200ns, the feedback capacitance C_F=120fF.

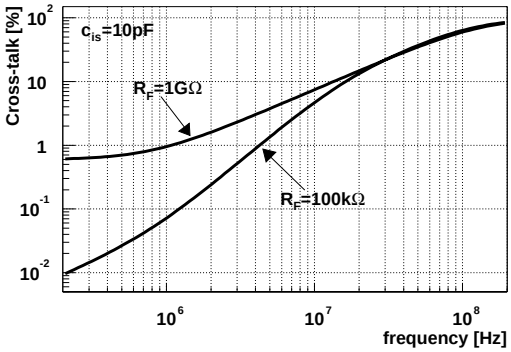
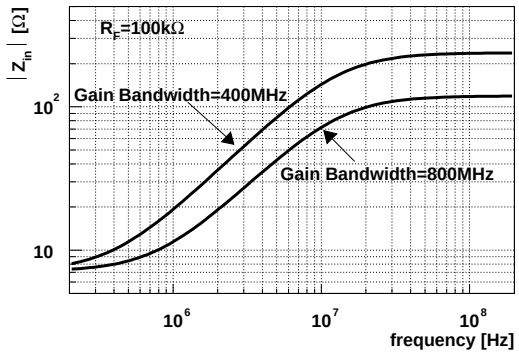
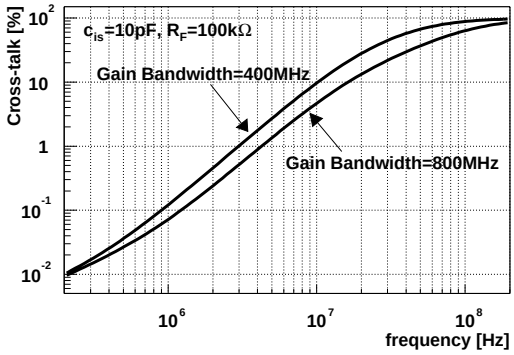


Figure 1.12: Normalized cross-talk signals versus the frequency for charge and transimpedance preamplifiers.

Generally, transimpedance preamplifiers appear more interesting. However, one has to remember that low values of the feedback resistor together with the 120fF feedback capacitance result in time constants in the feedback circuit that cannot be neglected from the point of view of shaping the signal. In practice this type of feedback is used for fast front-end electronics in which band-pass filters following the preamplifier stage are tuned to a rather high frequency. For such applications transimpedance preamplifiers will offer significantly lower input impedance and consequently better attenuation of the cross-talk signals than charge preamplifiers.



(a)



(b)

Figure 1.13: Comparison between the input impedance (a) and cross-talk (b) for transimpedance preamplifiers with two different gain-bandwidth products.

The importance of the high gain-bandwidth product of the elementary amplifier was already mentioned during the timing analysis of the preamplifier's response to the detector signal. Figure 1.13 shows the impact of the gain-bandwidth product on the preamplifier input resistance and the cross-talk signals. One can see that for medium frequencies the relationship between gain-bandwidth product and cross-talk is roughly linear i.e. halving the gain-bandwidth product causes a doubling of the cross-talk.

1.3. Noise filtering in practical implementations of VLSI Front End amplifiers for readout of silicon detectors

As was already mentioned, in order to improve the Signal-to-Noise Ratio (SNR) at the preamplifier output one has to limit the bandwidth of the system. The filters located after the preamplifier in the signal chain affect in the same way both the noise and the signal spectra. Because the signals are usually considered in the time domain, the filter circuits are commonly named as shapers.

In order to estimate the noise filtering efficiency of different type of filters one can assume a simplified model for noise generation in the charge sensitive preamplifier shown in Figure 1.14[3]. To simplify the analysis only white and non-correlated noise sources are considered. The influence of the feedback resistance on the transmittance of the preamplifier is neglected for the moment and its noise contribution is represented as part of the parallel noise source i_{np}.

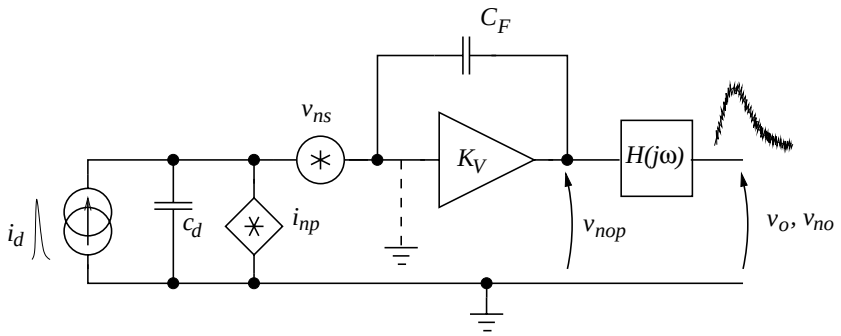


Figure 1.14: Equivalent noise schematic diagram of the charge preamplifier and shaper stage working with the silicon detector. The electronic noise is represented by two noise sources, parallel and serial, transferred to the amplifier input. The frequency characteristic of the shaper stage is represented by the transmittance H(jω).

Assuming that we have an ideal elementary amplifier with infinite gain and bandwidth and using superposition methods and Thevenin's theorem for voltage noise source v_{ns} one can write the following expression for the power spectrum of noise v_{nop} at the preamplifier output:

$$\frac{\overline{v_{nop}^2}}{\Delta f}=\frac{\overline{v_{ns}^2}}{\Delta f}\cdot\frac{c_d^2}{C_F^2}+\frac{\overline{i_{np}^2}}{\Delta f}\cdot\frac{1}{\omega^2\cdot C_F^2} \tag{1.14}$$

The equivalent series noise voltage v_{ns} represents the collector current shot noise of the input BJT or channel thermal noise of the MOS transistor. The equivalent parallel noise current source i_{np} represents the detector leakage current contribution, with the contribution from the feedback resistance, as well as the base current shot noise in the case of a BJT device. Thus, the noise spectrum at the preamplifier output is no longer white.

The classical theory of noise filtering described in [1.4] and [1.5], developed for nuclear spectroscopy systems is focused on the maximisation the Signal-to-Noise-Ratio factor. It

[3] The detailed noise analysis of the transimpedance amplifier working with CR-RC^3 type of filter, taking into account all noise sources and their correlations as well as realistic parameters of the elementary amplifier is presented in Chapter 3 and in Appendix 7.

introduces the idea of the optimum linear filter. Its functionality can be split into a whitening section and a matched filter section [1.6]. Using the Schwarz inequality it can be shown that the transfer function of the matched filter should be the conjugate of the signal spectrum. In the time domain, the pulse response of the matched filter should represent the mirror image of the input signal delivered by the whitening section, delayed by the measurement time. Assuming an ideal response of the preamplifier to a Dirac delta charge delivered by the silicon detector (i.e. a voltage step function), the response of the whitening section will be an exponential signal, decaying with a noise corner time constant, τ_C. The noise corner time constant is equal to the inverse of the angular frequency at which the contributions of parallel and series noise sources v_{ns} and i_{np} to the preamplifier output noise become equal. Notice that a simple CR differentiation stage tuned to the τ_C time constant provides the whitening function. Therefore the response of the optimum noise processor to the ideal voltage step at the preamplifier output will be a cusp function, truncated in order to achieve a realizable design.

For tracking systems developed for LHC experiments, in addition to amplitude measurement, one has to take into account timing aspects of the system. The timing requirements for the tracking systems at LHC experiments can be defined by two goals: correct association of the event with the bunch crossing in which it occurred, and a double pulse resolution that should not exceed 50ns i.e. two bunch crossing periods. The timing requirements determine the upper range of the response time of the signal chain. Classical optimisation using a whitening section of the filter followed by the matched one is not feasible when the noise corner time constant, τ_C, is higher than the required time resolution, which is the case for silicon strip detectors working with front-end electronics under LHC conditions. In order to provide a good performance of the optimum filter with relatively high data rates, practical implementations are based on a time-variant option, with the weighting function of the filter changing with time. Consequently, designing an optimum filter becomes more complex, which is in contradiction with another basic optimisation goal for multi-channel SSD front-end electronics, namely achieving low power consumption and simplicity. The latter is translated directly into smaller silicon area occupied by the filter circuits and better robustness of the chip, which has to work in a radiation environment.

In order to trade off performance against power consumption and simplicity of the design, it is preferable to use more conventional band-pass filters, such as CR-$(RC)^n$ continuous filters, which are easy to implement in multi-channel front-end chips. They consist of one differentiating stage, which filters low frequency noise and n-stages of integrators attenuating the high frequency components. The transmittance of the n-order CR-$(RC)^n$ type filter, with equal differentiation and integration time constant τ, is given by the equation (1.15).

$$H(s)=\frac{s\cdot\tau}{(1+s\cdot\tau)^{n+1}} \tag{1.15}$$

The general expression describing the response of the filter working with the preamplifier stimulated by a Dirac delta signal charge Q_i in the time domain (Figure 1.14) can be calculated as the following:

$$v_o(t)=\frac{Q_i}{C_F}\cdot\frac{1}{n!}\cdot\left(\frac{t}{\tau}\right)^n\cdot e^{-\frac{t}{\tau}} \tag{1.16}$$

The amplitude of the filter response is given by equation (1.17). The signal peaks at the time t_{peak} commonly called the peaking time of the shaper response. For the CR-(RC)^n filter it is equal to n times the filter time constant τ.

$$V_{o\max} = \frac{Q_i}{C_F} \cdot \frac{1}{n!} \cdot \left(\frac{n}{e}\right)^n \quad \text{for} \quad t_{peak} = n \times \tau \tag{1.17}$$

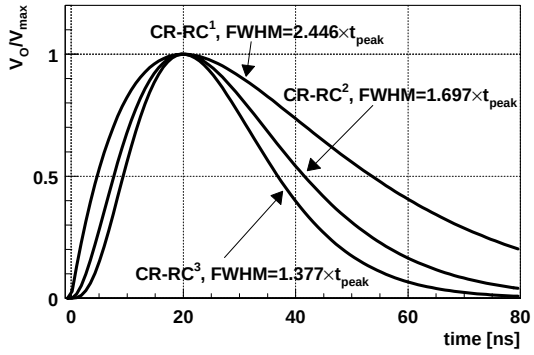


Figure 1.15: Responses of the preamplifier-shaper stage for various order CR-RC^n filters normalised to the same amplitude and peaking time.

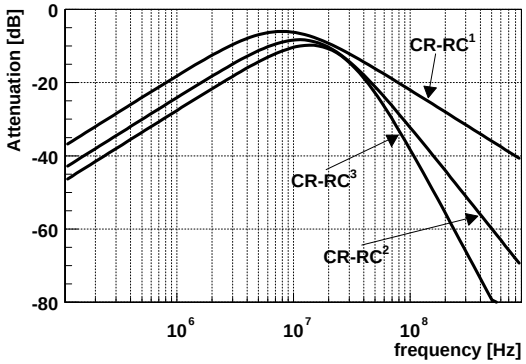


Figure 1.16: Frequency characteristics of various order CR-RC^n filters normalized to the same peaking time (20ns).

In Figure 1.15 the pulse shapes described by the equation (1.16) are plotted for various orders of the filter after normalization to the same peaking time. The figure also shows the timing parameter Full Width at Half Maximum (FWHM). It can be seen that the higher order filters provide lower values of the FWHM parameter and consequently better double pulse resolution of the amplifier, i.e. the ability of the amplifier to distinguish two consecutive signals from the detector. Examples of the frequency characteristics for various CR-(RC)^n filters normalized to the same, 20ns peaking time are shown in Figure 1.16.

The rms noise σ_{nfo} at the output of the CR-(RC)^n shaper can be described by the following definite integral:

$$\sigma_{nfo}^2 = \int_0^\infty \frac{\overline{v_{nop}^2}}{\Delta f} \cdot |H(j\omega)|^2 \, \partial f = \int_0^\infty \left(\frac{\overline{v_{ns}^2}}{\Delta f} \frac{c_d^2}{C_F^2} + \frac{\overline{i_{np}^2}}{\Delta f} \frac{1}{\omega^2 \cdot C_F^2} \right) \cdot \frac{\omega^2 \cdot \tau^2}{\left(1+\omega^2 \cdot \tau^2\right)^{n+1}} \, \partial f \tag{1.18}$$

Solving integral (1.18) one obtains:

$$\sigma_{nfo}^2 = \frac{\overline{v_{ns}^2}}{\Delta f} \cdot \frac{c_d^2}{\tau \cdot C_F^2} \cdot \frac{\Gamma(n-1/2)}{8 \cdot \sqrt{\pi} \cdot \Gamma(n+1)} + \frac{\overline{i_{np}^2}}{\Delta f} \cdot \frac{\tau}{C_F^2} \cdot \frac{\Gamma(n+1/2)}{4 \cdot \sqrt{\pi} \cdot \Gamma(n+1)} \tag{1.19}$$

The front-end amplifier converts the charge delivered by the silicon detectors to a voltage signal, therefore the equivalent input noise of the amplifier is given usually as Equivalent Noise Charge (ENC). The ENC for the preamplifier working with CR-(RC)^n shaper given in coulombs is equal to the output noise divided by the maximum amplitude of the response to the unity input charge pulse (Q_i = 1):

$$ENC[C]=\frac{\sigma_{nfo}}{V_{o\max}} \tag{1.20}$$

In order to show more clearly the dependence of the ENC on the detector capacitance and the peaking time of the applied shaper, the equation (1.20) can be rewritten in a more general form. Using the expressions describing the output noise and response amplitude the equation (1.20) can be transformed to the following:

$$ENC[C]=F_V \cdot \frac{\overline{v_{ns}}}{\sqrt{\Delta f}} \cdot c_d \Big/ \sqrt{t_{peak}} \oplus F_i \cdot \frac{\overline{i_{np}}}{\sqrt{\Delta f}} \cdot \sqrt{t_{peak}} \tag{1.21}$$

The factors F_V and F_i can be evaluated for different filter orders n, from equation (1.19), replacing the filter time constant τ by the peaking time according to (1.17). Table 1.1 gives the weighting factors derived from equation (1.21) for various order CR-RC filters.

Table 1.1 Noise factors for different order of CR-RC filters as defined by equation (1.21)

	CR-RC	***CR-RC²***	***CR-RC³***
$\boldsymbol{F_V}$	$\frac{e}{2\cdot\sqrt{2}}$	$\frac{e^2}{8}$	$\frac{e^3}{12\cdot\sqrt{3}}$
$\boldsymbol{F_i}$	$\frac{e}{2\cdot\sqrt{2}}$	$\frac{e^2\cdot\sqrt{3}}{16}$	$\frac{e^3}{36}\cdot\sqrt{\frac{5}{3}}$

Although the example of noise calculation has been performed for the preamplifier working in a charge configuration, its result can be extended directly to the transimpedance preamplifiers. In order to provide the CR-RC^n transfer function for the transimpedance front-end amplifier, the feedback time constant τ_F has to be equal to the time constant of the low-pass RC^n filter. In that case the feedback circuit of the transimpedance amplifier provides the same function as the differentiating stage of the charge preamplifier. In both cases the maximum amplitude of the response is inversely proportional to the feedback capacitor C_F. Propagation of the series and parallel equivalent noise sources to the output for charge sensitive preamplifiers is shown in the Appendix. The output noise related to the series equivalent input noise (for example collector current shot noise), assuming an ideal elementary amplifier, is equal to $v_{ns} \times Z_F \times Y_d$. For the parallel noise (base current shot noise) it can be shown that the output noise is equal to $i_{np} \times Z_F$. By replacing Y_d by $j\cdot\omega\cdot c_d$, Z_F by $R_F/(1+j\cdot\omega\cdot R_F\cdot C_F)$ and $1/(j\cdot\omega\cdot C_F)$ respectively for the transimpedance and charge amplifiers, and by assuming a CR-(RC)^n filter in the case of the charge sensitive preamplifier and a (RC)^n low-pass filter for the transimpedance amplifier, one derives the same expression for the ENC in the cases of amplifiers working in the charge or the transimpedance configuration. In the case of a transimpedance amplifier one has to take into account the contribution to the ENC from the feedback resistance R_F, which has to be considered as an extra source of parallel noise (see the analysis in Chapter 4).

From Table 1.1 it can be seen that the coefficients determining the contribution of series noise have very similar values independently of the order of the filter (in fact the series

noise contribution starts to increase for higher filter orders[4]). On the other hand, the factors describing the contribution of parallel noise decrease for higher filter orders. In discussing the possible sources of parallel noise one has also to take into account the shot noise of the detector leakage current. At the beginning of the experiment it will be relatively low, however, it will increase continuously with time due to the radiation damage. Consequently the higher order filters will be more favourable for the front-end electronics of the silicon trackers at LHC experiments.

For relatively long silicon detectors, one can expect that the series noise will be the dominant noise source because of its dependence on the input load capacitance, which in the case of the foreseen LHC silicon detector modules is in the range of 20pF. In order to achieve the required noise performance of the front-end electronics with a specified detector type and speed requirement, one has to take care over the levels of the equivalent input noise source itself i.e. the values of v_{ns} and i_{np}. The noise analysis of front-end amplifiers built with different types of devices, with regard to its elementary noise sources, as well as power consumption and radiation hardness is presented in Chapter 3.

In discussing the performance of the CR-RC filters one should mention the idea of triple correlated sampling filters, used in the readout chip of tracker system in the CMS experiment. The idea of reshaping the long pulses delivered by a relatively slow front-end amplifier by using the deconvolution method is described in reference [1.8]. The results from recent prototypes of front-end chips with the Analogue Pulse Shape Processor (APSP) providing this deconvolution function can be found in [1.9]. That idea was very interesting in the past, because of limited gain-bandwidth product in the old CMOS radiation hard technologies. However, even though the theoretical limits of the noise performance of triple correlated sampling filters are close to CR-RC filters [1.8], one should not overlook two limitations that may degrade their performance in the real experiment. The first limitation is related to variations in the charge collection time in the silicon detectors, which will have an impact on the pulse shape provided by the shaper before the data enters the APSP. A deviation of the pulse shape may result in two effects: an incorrect value of the signal amplitude and the appearance of a fraction of the signal in subsequent time slots. A second limitation is related to the sampling of the pulses, which is made at the signal peak as well as on the signal edges. Thus the time jitter of the sampling clock will cause uncertainty in the measured signal amplitudes.

Standard bipolar technologies and the DMILL BiCMOS radiation hard process, the latter available since 1995, were fast enough to allow development of bipolar preamplifiers with performance sufficient to enable the use of simple CR-RC filters for electronics for LHC applications. The recent introduction of deep sub-micron CMOS technologies, which allow radiation-tolerant circuit development when certain layout methods are employed, has now opened up this possibility for designs made in CMOS.

In considering the use of continuous CR-RC filters for the LHC type of front-end electronics, one has to select a configuration of the preamplifier and the order of the band-pass filter applied in the shaping stage. Taking into account minimization of the

[4] One can find in the literature [1.7] that the noise performance of CR-RC filters improves towards higher filter orders n, and it is the best for an ideal Gaussian filter ($n \rightarrow \infty$). This is valid for the case of optimum filtering i.e. for the filter time constant equal to the corner noise time constant τ_C, when the contribution of parallel and series equivalent noise sources are the same. Keeping the filter time constant equal to τ_C and continuously increasing the filter order causes a linear increase of the response peaking time i.e. for an ideal Gaussian filter the peaking time of the optimum filter goes to infinity. For the LHC front-end electronics requiring fast response time (which does not permit optimum filtering), the contributions of series and parallel noise sources have to be taken into account separately.

preamplifier input impedance, improvements in filtering of the parallel noise as well as the specifications needed to handle a high data rate (lower FWHM parameter), the transimpedance amplifier followed with a triple integrator would be a preferred option.

In order to implement a CR-$(RC)^n$ type of filter in a system with transimpedance preamplifier, one has to keep the time constant of the feedback circuit, which provide differentiation of the signal, the same as the time constant of the n-stage integrator following the preamplifier. In practical implementations of the amplifiers intended to work with minimized power consumption, various sections of the amplifier together with their dominant poles will influence the overall transfer characteristic of the integrator. Ensuring that the feedback time constant is exactly equal to the time constant of the integrators could be sometimes difficult. The minimum value of the feedback resistance (which acts as an extra source of parallel noise) is determined by the maximum tolerable ENC. In addition, the primary objective in the optimisation of the feedback capacitor C_F, is providing the frequency compensation of the preamplifier.

In consequence the overall transfer function of the real transimpedance amplifier implementations is close to, but not an ideal CR-$(RC)^n$. Nevertheless, by keeping the same central frequency as well as order of the filter one can achieve the same noise filtering efficiency. Consequently, for the noise analysis one can approximate a transfer function of a given transimpedance amplifier by an ideal CR-$(RC)^n$ filter characteristic. As will be shown later, the transfer function of all front-end transimpedance amplifiers presented in this thesis can be approximated by a 3rd order CR-RC filter.

1.4. Basic readout architectures

As was already pointed out, the readout chips designed for silicon trackers at LHC experiments have to deal with a high volume of data from the detector. They have to provide not only sufficient time resolution in order to correctly assign the data to a given physical event (bunch crossing), as was discussed in the previous sections, but they also have to transmit the data off the detector for further processing. Transmitting the data associated with each bunch crossing from every detector channel is simply not possible due to its huge volume – and it is also unnecessary to do so, because not all the events are interesting from the physics point of view. The decision whether a given event is worth analysis, is produced in separate sub-detectors, usually the calorimeters and the muon spectrometers, which measure the energy and type of particles created during the interactions. This decision is sent to the tracking detectors in the form of a signal called "trigger level one" (L1). It arrives after some delay with respect to the corresponding bunch crossing time, which has to be accommodated by the front-end chip. Therefore the data received from the silicon detectors, after it has been amplified and shaped, has to be kept on-chip until the L1 trigger signal arrives.

The issue determining the architecture of the data buffers is whether the pulse amplitude information from the detector signal is used or not. Historically most collider experiments have used full analogue readout for silicon trackers and vertex detectors. In order to delay an analogue data coming from the detector an Analogue Delay Buffer (ADB), a kind of analogue memory, has to be employed. Retaining the full analogue data, allows the use of algorithms providing improvement of the spatial resolution and significant reduction of the so-called common mode noise, which is the external electromagnetic pickup affecting all electronic channels synchronously in the same manner. The price paid for the safety and overall performance offered by the analogue readout solution is the necessity of using a large number of analogue links to send uncompressed data off the detector.

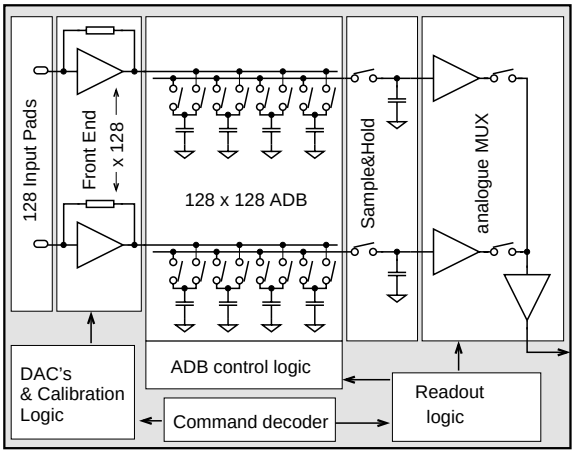


Figure 1.17: Block diagram of the SCTA chip representing full analogue readout architecture.

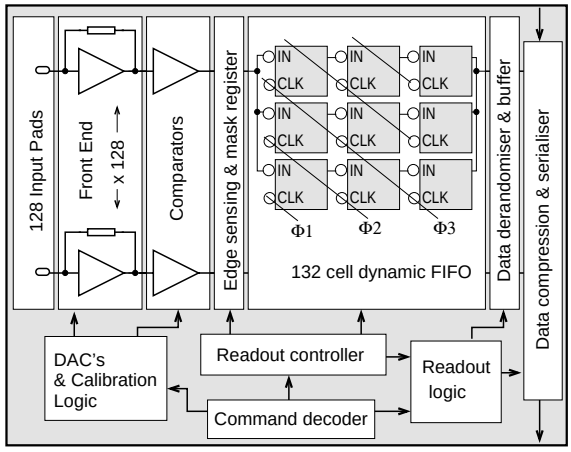


Figure 1.18: Block diagram of the ABCD chip representing binary readout architecture.

Some of the experiments, such as ATLAS, require moderate spatial resolution in the range of 20μm. This resolution can be handled with the binary readout system, which transmits simple yes/no information from silicon strips designed with the proper pitch. The binary data could be stored in a clock-driven digital pipeline or a standard Random Access Memory circuit (RAM) during the L1 trigger latency. In this case a standard digital optical link can be used for the data transmission. This solution requires a front-end chip with very good uniformity of the gain and comparator offsets across the channels, as well as good Power Supply Rejection Ratio (PSRR), which is always difficult to achieve in the case of single-ended input structures[5]. Figures 1.17 and 1.18 show examples of two different, basic architectures in front-end chips developed for readout of silicon detectors at LHC experiments; the SCTA128VG chip implements the analogue readout approach and the ABCD3T chip the binary readout architecture designed for the ATLAS silicon tracker.

1.4.1. SCTA chip – a full analogue readout architecture implemented in radiation hard DMILL technology

Figure 1.17 shows the block diagram of the SCTA128VG chip, a final version of an analogue front-end chip developed for readout of silicon strip detectors at LHC experiments. It comprises six basic blocks: 128 channels of the front-end amplifiers, analogue memory (ADB) with the control logic, analogue output multiplexer with sample-and-hold circuit, command decoder, readout logic with sequencer, block of bias DAC's and calibration circuits providing good testability of the chip.

The front-end circuit is a fast transimpedance amplifier followed by an integrator providing a semi-gaussian pulse of 20ns peaking time. The peak values are sampled with a 40MHz clock which is synchronised with the particle collisions and stored in a 128-cell deep analogue memory (ADB). Upon arrival of the trigger signal L1 the analogue data from the corresponding column of the ADB are tagged and, depending on the availability of the readout unit, are sampled in the buffer and sent out through the analogue

[5] The choice of single-ended architecture of the input stage is driven by the strong requirement of lowering the power consumption, while at the same time achieving the desired noise performance of the front-end chip.

multiplexer. Since the readout time of the 128-channel chip with the multiplexer working at 40MHz is equal to 3.75μs[6], and the L1 trigger is expected to arrive randomly in time with an average rate of up to 100kHz, the probability of another trigger arriving while the chip is still sending out data is not zero.

The skip logic, governing the write and read pointers of the analogue memory, can handle up to eight ADB columns that are marked and protected from overwriting because they contain data waiting to be transmitted off-chip. Organized in this way the derandomizer-buffer subtracts those cells from the overall size of the memory intended for delaying the data for the L1 trigger latency.

The bias currents of the analogue stages of the circuit are controlled by internal DACs**.** This feature allows for noise optimisation and compensation of the drifts of the operating points caused by radiation damage. Internal calibration circuitry improves general testability of the chip by simulating the charge pulses delivered by the detectors. All the communication to the chip, including the sending of triggers and the set-up its configuration, as well as generation of calibration pulses, is done via a 40MHz serial interface. The detailed architecture of the chip and its analogue building blocks, together with its simulated performance and test results are described in the following chapters.
The SCTA chip was developed from the beginning as one of the possible options for readout of the silicon strip detectors in the ATLAS Semi-Conductor-Tracker (SCT). Currently, the SCTA chips have found the following applications:

- Read-out of silicon strip detectors for NA60 experiment.
- Production quality assurance testing of silicon strip detectors for ATLAS SCT.
- Fast read-out chip for diamond strip detectors.
- Read-out of silicon pad detectors for HPD applications.

1.4.2. ABCD3T chip – a final version of binary read-out chip for ATLS SCT in DMILL technology.

Figure 1.18 shows the block diagram of the binary read-out chip for the ATLAS SCT [1.10] – the ABCD3T chip. It comprises in a single chip all blocks of the binary read-out architecture: 128 front-end amplifiers followed by the comparators, binary pipeline, derandomizing buffer, block of DAC's providing biasing currents to the analogue stages as well as threshold control for the comparators, calibration circuit and data compression logic together with readout control logic.
The comparators following the front-end amplifiers provide only 1-bit yes/no information, which is transferred to a 132 cell deep multiplexed FIFO. The signals delivered by the comparators are sampled by the input register (in the so-called level mode of operation), or alternatively the edge of the signal is detected, latched and clocked into the pipeline (the edge mode of operation). The input register also provides channel masking and can be loaded with a test pattern allowing separate testing of the digital part of the chip.
Upon receiving the trigger signal the data from the pipeline output is transferred to the eight-event second level buffer (otherwise it is lost), which serves as a derandomizing buffer. At every trigger three bits corresponding to the triggered bunch crossing and the

[6] Apart from sending the analogue data itself from the 128 regular channels, the chip must also send:

- The contents of two independent 4-bit counters (counting BCO and L1 triggers) for correct synchronization with the off-detector electronics;
- Three fixed analogue levels for calibration of the optical link;
- A few bits of header and trailer information used for correct data stream identification.

time slots immediately before and after it are transferred to the second level buffer. The overall size of the second level buffer is 24 bits, which results in less than 1% of dead time. Before sending out the data it is compressed in the DCL block (Data Compression Logic), which makes mainly zero suppression. It is then serialized in the ROL unit (Read-Out Logic). Given that the expected occupancy of the detector is only 2%, the zero suppression operation is made on-chip and provides a significant reduction of the volume of data to be sent out. This allows a reduction of the number of optical links required per chip, but it required the implementation of a special protocol allowing for data transfer between the chips on the detector modules [1.23].
The main application of the ABCD3T chip is the readout of the silicon strip detector modules in ATLAS SCT. An example of the detector module holding four, 6.5 by 6.5 centimetres, silicon strip detectors, intended to use in the barrel part of the ATLAS SCT is shown in Figure 1.2.

2. Radiation effects in front-end electronics

The subject of radiation effects in electronics is very broad and covers all possible interactions of different types of radiation with the material of the devices under consideration. This chapter presents a short overview of the issues concerning front-end electronics to be used in the LHC radiation environment. In the inner detector, where the tracker front-end electronics will be installed, the radiation field consists of [2.1]:

- Primary particles from the proton-proton collisions,
- Secondary radiation from the interaction of these particles with the beam-pipe and the material of the inner detector,
- Albedo neutrons from the calorimeters.

Semiconductor devices will suffer from two basic radiation damage mechanisms:

- Ionisation damage in which the energy absorbed by the insulating layers, which mostly consist of silicon oxide, releases free charge carriers. These result in the build-up of parasitic electric fields that change the electrical characteristic of the devices.
- Displacement damage in which the incident particle (neutron, proton, electron) or gamma quantum transfers enough energy to the Si atom to displace it from its site in the crystal lattice. This results in the distortion of the lattice structure and changes the electrical properties of the semiconductor.

2.1. Radiation damage units

The ionising radiation effect depends basically on the absorbed energy and it is not related to a particular type of radiation. Therefore the ionisation damage can be quantified in terms of the energy absorbed per unit of mass of the material, which is measured in units of rad or gray (1rad = 100erg/g, 1Gy = J/kg, 1Gy = 100rad). Because the amount of charge released by the given dose depends on the material, the ionising dose must be specified for a given type of the absorber. In the case of silicon devices most of the ionising damage is related to changes in the silicon oxide. Therefore the Total Ionising Dose (TID) numbers discussed in this chapter will be referred to SiO_2.

Displacement damage is related to the non-ionising energy loss of the incident particle and it depends on the type of particle and its energy. In order to compare displacement damage in the real radiation environment with the results of irradiation tests using particular beam sources, all fluencies are normalised to the equivalent mono-energetic beam of 1MeV neutrons (1MeV n/cm^2). The normalization is done using the cross-sections for inelastic collisions of the incident particles with the silicon lattice. The normalization works only for the displacement damage caused by the collision with silicon atoms and does not take into account, sometimes non-negligible, effects due to nuclear reactions. For example boron, which is commonly used as a p-type dopant, will interact with thermal neutrons[1] and will be transformed into a lithium atom, an alpha particle and a gamma quantum, thereby producing both displacement and ionisation damages.

[1] At room temperature the most probable energy for thermal neutrons is in the range of 12meV(mili-electron-Volt). It is roughly three orders of magnitude less than the mean energy of the Si lattice displacement (25eV).

2.2. Ionisation damage

Depending on their energy, gamma or X-Rays can interact with matter in three different ways:

- At low energy, for X-Rays in the range of a few keV the photoelectric effect dominates. The incoming photon is completely absorbed. The excited atom emits an electron from the innermost shell structure. The remaining energy of the photon is transferred to the emitted electron as its kinetic energy. An electron from the valence band de-excites the atom by dropping into the new energy vacancy and emitting a low energy photon.
- For higher energy photons, above 100keV, the Compton effect dominates. The incoming photon collides with the electron, which is free or weakly bound to the atom, transferring only a part of its energy.
- Electron-positron pair creation takes place for high-energy photons (above 1MeV). The annihilated high-energy photon produces an electron and a positron according to the mass energy conservation law $E = m \times c^2$.

For TID testing of electronics two different radiation test environments are commonly employed:

- An X-Ray tube equipped usually with a tungsten target and producing an X-Ray spectrum with a peak around 10keV.
- A radioactive isotope providing a source of gamma rays. A standard isotope commonly in use is ^{60}Co. It emits two characteristic gamma rays of 1.17 and 1.33MeV.

2.2.1. Charge generation, recombination and hole transport in SiO_2 [2.3]

As already mentioned the part of the device that is most sensitive to ionisation damage is the oxide-insulating layer. The energy of ionisation in silicon oxide has been estimated to be roughly 18eV. The radiation-generated electrons have mobility of the order of $20 cm^2/V \cdot s$ at room temperature. The mobility of the holes depends strongly on temperature and electric field and is in the range of $10^{-4} \div 10^{-11}$ $cm^2/V \cdot s$. For this reason the electric field sweeps the electrons out from the oxide quite rapidly, in a time less than a pico-second. The fraction of the charges that recombine during this first short period of time depends on the applied field, the energy and the kind of incident particle. Although without an applied electric field the generated electron/hole pairs have a higher probability of recombining, the fraction of non-recombined charge might nevertheless be up to 30% in the case of cobalt irradiation [2.3].

Non-recombined holes remain initially near their point of creation and cause a negative shift of the flatband voltage and the threshold voltage. With time the holes start to move towards the negative electrode under the effect of the applied electric field, where they are collected or captured in deep trapping sites. This hole transport process, which is also dependent on the value of the electric field, can take between seconds at room temperature to tens of hours at 80K. There are at least two models describing the transport mechanisms of the holes through the silicon oxide. In the multiple-trapping model the holes move in between localized states through the valence band. Because of the wide distribution of the trap energy, one can expect large fluctuations of the thermal release rates from the traps and consequently a high dispersion of the transport timescale. The second model is the hopping transport mechanism, in which the holes move between trap

states by a phonon-assisted tunnelling process. The initially empty localized state captures the hole, which in consequence lower the total energy of the system by distortion of the lattice around the trap site (self trapping). The tunnelling of the hole between two neighbouring states occurs when thermal fluctuation of the system brings the energy level of the occupied trap to the same level as that of empty trap**.** The transition probability for this process is the product of the spatial integral of the wave functions of the two sites and the probability of creating the intermediate activate state of the coincident energy levels. The temperature dependence of the process implies that hopping is perhaps the primary mechanism responsible for hole transport in SiO_2.

2.2.2. Hole trapping and annealing in $Si0_2$

The holes generated in the oxide bulk arrive in the proximity of the negative electrode, i.e. the polysilicon gate or silicon channel, where they encounter the distribution of hole traps that starts at the Si/SiO_2 interface and extends a few nanometres into the oxide. The fraction of holes captured will depend on the density of the traps and the hole capture cross-section. The remaining holes will continue towards the silicon and finally recombine. It has been found that the holes are trapped mostly in a thin, 5 to 20nm region at the SiO_2/Si interface. This region is under mechanical stress as well as being oxygen deficient. Most of the hole traps are probably local oxygen vacancy defects.

Trapped holes disappear from the oxide with time scales ranging from milliseconds to years. There are two annealing mechanisms observed at normal and elevated temperatures. The tunnel annealing mechanism, observed at room temperatures, assumes that electrons from the silicon tunnel into the oxide, where they recombine with the trapped holes. As a consequence of the exponential dependence of the tunnelling probability on the depth in the oxide, annealing of the trapped holes takes place with a logarithmic time dependency. At temperatures above about 150°C annealing occurs as a result of the thermal release of the holes from the traps.

In the past radiation-hardening efforts were focussed on decreasing the quantity of the trapped oxide charge through the development of clean, low-growth-temperature oxides that are characterised by low trap densities. The scaling down of CMOS technologies and the accompanying reduction of the oxide thickness significantly improved the radiation hardness of the devices. The hole trapping efficiency diminishes with the square of the oxide thickness and furthermore, for oxide thicknesses below 10nm, the trapped holes are rapidly removed by the tunnelling effect (see Figure 2.1).

2.2.3. Radiation-induced interface traps [2.4]

As already mentioned the interface between the amorphous oxide and the crystalline silicon is generally deficient in oxygen, giving rise to dangling silicon bonds. These dangling bonds act as interface traps with energy levels within the forbidden bandgap at the SiO_2/Si interface. Since they are located within one or two atomic bond distances (~0.5nm) from the silicon lattice, the electron or holes in the conduction or valence bands can readily make quantum mechanical transitions into and out of these traps. High quality MOS devices have pre-irradiation interface-trap densities in the range of 10^9-10^{10} traps/cm^2. This value is very dependent on the process parameters and typically increases after ionising radiation.

Depending on the energy of the traps within the bandgap, the inverse of the transition rate can be in the range between microseconds to tens of milliseconds at room temperature, and between 10^6 to 10^{18} seconds at 100°K. The transition rate is the basis of most

measuring techniques for the characterisation of the density and location of interface traps.

Another fundamental property of the traps is that the net residing charge can be positive, negative or neutral. From this standpoint the interface traps are classified as:

- Donor traps. If the energy level of the trap is below the Fermi level then the net charge is neutral, otherwise the net charge is positive (the trap is donating the electron).
- Acceptor traps. The net charge is neutral for traps above the Fermi level and it becomes negative for traps below the Fermi level (the trap is accepting the electron).

Under all conditions the interface trap is in a more positive charge state if its energy is above the Fermi level. The current models postulate that the radiation-induced interface traps are acceptors in the upper part of the bandgap and donors in the lower part of the bandgap. This hypothesis fully explains the behaviour of the NMOS and PMOS transistor characteristics after ionising radiation.

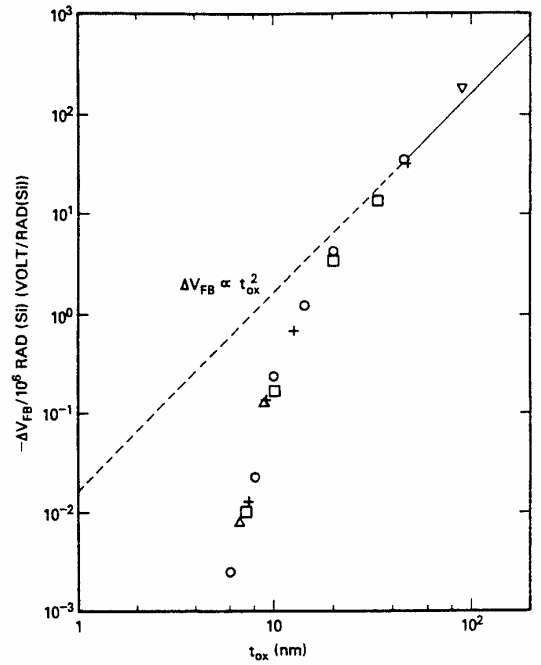


Figure 2.1: Increase of the flat-band voltage[2] per Mrad dose for MOS capacitors as a function of oxide thickness. Figure after [2.5].

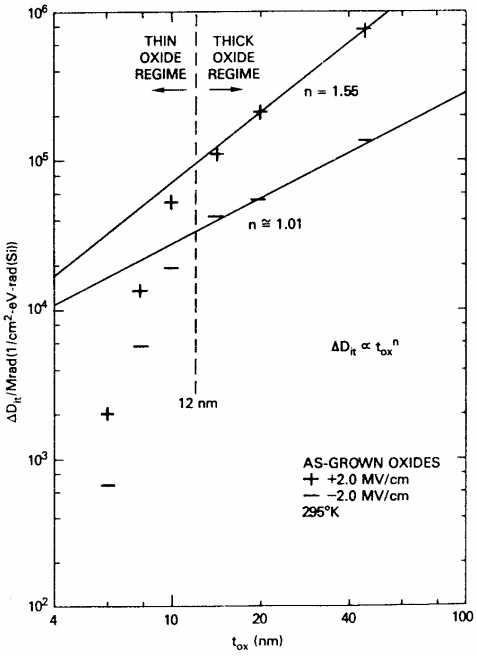


Figure 2.2: Increase of radiation-induced interface traps for as-grown oxides in case of positive and negative electric field. Figure after [2.6].

There are several models that describe the increase of interface traps with ionising radiation. The "hydrogen" model suggests that hydrogen atoms bonded with trivalent Si atoms during the processing are released into the bulk of the oxide in response to the ionising radiation. Later on, they drift or diffuse to the interface where they react with interfacial Si-H bonds, breaking them and producing molecular hydrogen H_2 and dangling Si bonds, which then act as interface traps. This model together with the low mobility of the hydrogen ion explains the slow build-up of the interface traps, which continues even while annealing is taking place. The second model, referred to as the "injection" model,

[2] In case of MOS transistor the change of the flat-band voltage reflects directly the change of the threshold voltage.

suggests that holes trapped near the interface are converted to the interface traps by electron injection from the channel. This injection model could explain the "prompt" component of the build-up of interface traps that appears on a short time scale. The third model is called Bond-Strain Gradient (BSG). It postulates that electron/hole pair generation near the interface in the strain region leads to rupture of the Si-O bond causing migration of oxygen defects and a consequent increase of interface traps. The observation that mechanical stresses during the processing influence the radiation hardness of MOS devices confirms that strain in the interfacial region plays a role in the generation of interface traps.

The build-up of radiation-induced traps depends on the applied electric field during irradiation. Generally, a very strong effect is observed for positive fields and significantly smaller build-up for negative fields (see Figure 2.2). Therefore for NMOS transistors, which are biased typically with positive voltages, the effect of the interface traps is much more pronounced than in the case of PMOS devices. As in the case of the charges trapped in the silicon oxide the build-up of radiation-induced interface traps is strongly dependent on the oxide thickness.

As shown in Figure 2.1 and Figure 2.2, for submicron technologies with the oxide thickness below 8nm, the increase of the radiation-induced interface traps as well as build-up of the net charge in the silicon oxide are almost negligible[3]. In view of the low sensitivity of the threshold voltage to ionising radiation one can consider that standard technologies with oxide thicknesses below 8nm produce MOS transistors that have an intrinsic radiation tolerance. Nevertheless, in order to provide complete radiation hardness of designs developed in such technologies, a special layout technique, described in the next section, has to be employed.

2.2.4. Radiation effects in MOS devices

Figure 2.3 shows schematically the basic effects induced by ionising radiation in silicon-oxide for the example of an NMOS transistor biased in the inversion region of operation. The electron/hole pair generated by the photon is separated and both components move under the effect of the applied electric field. The electron is quickly removed from the oxide, while the hole, which is transported by the hopping mechanism, is captured by the deep trap near the Si/SiO_2 interface.

As mentioned previously, trapped holes can be released during the thermal or tunnel annealing process. Due to the external voltage providing the biasing of the NMOS transistor in the inversion region, a fraction of the acceptor interface traps moves with energy below the Fermi level and become negatively charged. The net positive charge trapped in the oxide together with the negatively charged acceptor interface traps produces an electric field which adds to the electric field produced by the external voltage applied to the gate.

As already mention, the two processes of trapping the holes in the oxide and building up the interface traps, have different time dependences. Consequently the transfer characteristic of the transistor and the actual value of the threshold voltage depend on the ionising dose as well as time, i.e. the dose rate and possible annealing. Since trapping of the charges in the silicon oxide is a relatively fast process, the NMOS transistor will initially show a negative threshold voltage shift and later on, during the radiation or

[3] The radiation hard BiCMOS DMILL 0.8µm technology offers MOS devices with the gate-oxide thickness of 20nm. The standard CMOS IBM 0.25µm offers MOS devices with gate-oxide thickness of 5nm.

annealing, a positive shift due to the build-up of the interface traps. The final positive shift of the NMOS threshold voltage is commonly known as the "rebound" effect.

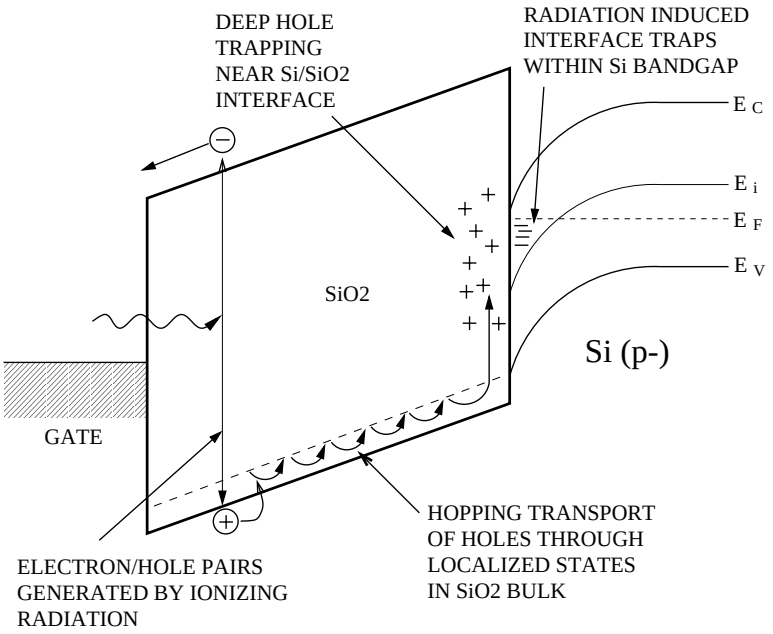


Figure 2.3: Schematic of the ionising effects in the NMOS device biased in the inversion region.

In case of PMOS devices, which are biased nominally with the opposite voltage polarity, the positively charged donor states are more pronounced. Nevertheless one should keep in mind that in the case of PMOS devices the density of radiation-induced interface states is significantly smaller than for NMOS transistors and the biggest influence on the final shift of the threshold voltage is due to positive charges trapped in the oxide. Figure 2.4 shows the typical evolution of the threshold voltage for PMOS and NMOS transistors manufactured in DMILL radiation-hard technology and biased with low and high gate voltage. The threshold voltage shift of the NMOS transistors shows the typical "rebound" effect, which is visible also during the annealing period.

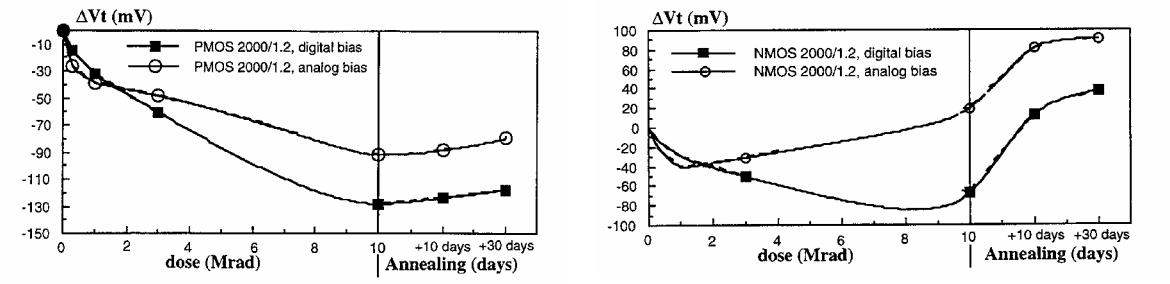


Figure 2.4: Typical threshold voltage shift of the PMOS and NMOS transistors in DMILL technology vs. the total ionising dose and the annealing time in case of digital bias (V_{gate}=5V) and analogue bias (V_{gate}=1.5V). RD29 [2.7] results.

It can be seen that this evolution of the threshold voltage depends strongly on the gate bias applied during the irradiation. Even if the absolute value of the threshold shift is well inside the process corners guaranteed by the DMILL foundry (maximum shift < 300mV), the performance of circuits that rely on device matching might be significantly degraded. This especially concerns the design of Digital-to-Analogue Converter (DAC), Analogue-

to-Digital Converter (ADC) or MOS comparator circuits. For example, the typical architecture of DACs employing gate-switched MOS current mirrors cannot be used for applications in a radiation environment.
Although the absolute scale of the threshold voltage shift depends on the particular process (standard or radiation-hardened process, oxide thickness), Figure 2.4 demonstrates a characteristic time-dependence of the threshold voltage and its dependence on the bias voltage which is valid for any CMOS technology. Therefore in order to ensure good analogue performance of circuits that are sensitive to transistor threshold matching the designer has to employ special precautions, even if the design is implemented in radiation hard or modern submicron technology.

In addition to the changes of the threshold voltage, ionising radiation affects other transistor parameters. Thus, it has been shown that the build-up of interface traps degrades the mobility of the carriers in the transistor channels i.e. it lowers the transconductance of the device [2.13]. Another consequence is the increase of flicker noise due to the trapping and releasing of the carriers at the interface of the channel and the gate oxide [2.14] and [2.15]. Since the build-up of the interface traps is significantly higher for the NMOS devices, one can expect that the noise increase will concern mostly that type of transistor. Although in the case of the fast front-end electronics presented in this thesis the increase of the flicker noise has rather limited influence, in the general case its effect should be taken into account during the noise optimisation of the preamplifier stage (see the analysis in Chapter 3).

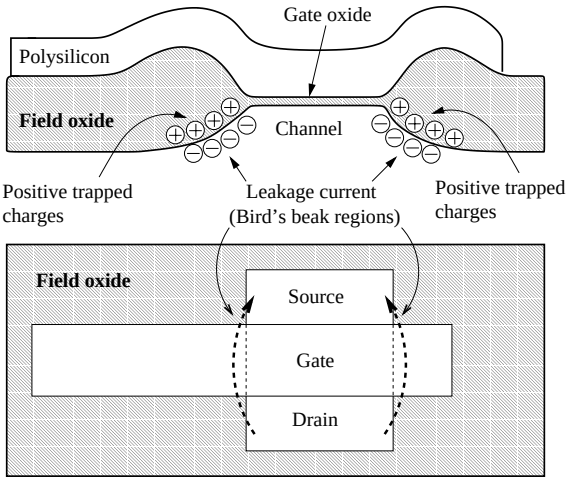


Figure 2.5: MOS transistor cross-section indicating the leakage paths due to the parasitic edge transistors.

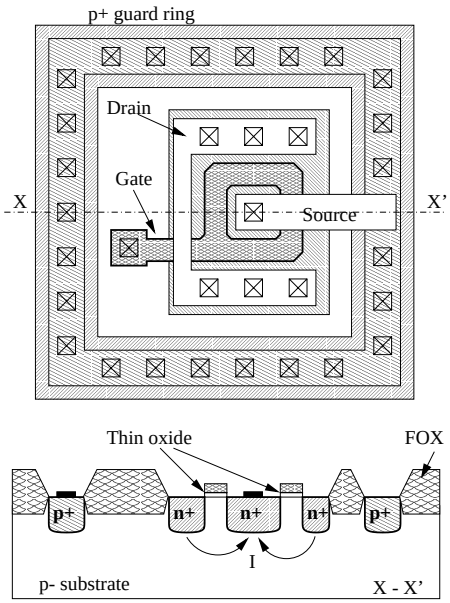


Figure 2.6: Enclosed-geometry layout and cross-section of the minimum size NMOS transistor in standard N-well IBM 0.25µm technology (not to scale).

Present-day CMOS processes are typically self aligned i.e. the polysilicon gate material is deposited over a thin oxide region while the source and drain implants are made in the region not covered by the Field Oxide (FOX) and poly. The transition region between the FOX and the thin oxide of the gate is very susceptible to the ionising effects. The silicon dioxide in this transition region, known also as the bird's beak, is under mechanical stress due to the dynamics of the oxide growth process and the transition between the thin and thick oxide. It also suffers from ion implant damage incurred during the implantation of

the source and drain. For these reasons the number of trapped holes in the FOX is much greater than in the thin oxide. In the case of NMOS devices built on p-type bulk, the threshold voltage of the parasitic edge transistor may be reduced significantly. If sufficient holes are trapped in the bird's beak it can decrease below zero and will then open a leakage path between source and drain, as shown in Figure 2.5, leading to an increase of the power consumption and/or malfunctioning of the circuit.

The cure for the post-radiation leakage problem in N-channel transistors depends on the technology under consideration. In a standard, commercial submicron process, a most effective solution is to use enclosed geometry layouts for all NMOS transistors in the circuit [2.8]. Figure 2.6 shows the layout and the cross-section of the minimum size NMOS transistor designed with enclosed geometry in IBM's 0.25μm commercial grade technology. The gate oxide thickness for this technology is in the range of 5nm and the threshold voltage shift due to ionising radiation is negligible. For the case of circuits using enclosed-geometry NMOS transistors radiation tolerance of up to a 30Mrad TID has been reported [2.9]. Although very safe from the radiation hardness point of view, the use of enclosed geometry transistors, also called edgeless transistors, has several disadvantages:

- Less dense layout
- Increase of the gate-to-source and gate-to-drain capacitances
- Difficulties in modelling the W/L ratio
- Asymmetry
- Limiting choice of the W/L ratio disallowing the use of long and narrow transistors

Nevertheless, for the front-end electronics implemented in commercial, submicron technologies and intended for installation in the LHC radiation environment, the use of this hardening technique is unavoidable [2.10].

Parasitic leakage paths can also be opened up between the source and drain of two adjacent NMOS transistors. The use of guard rings surrounding each transistor is a standard solution that is adopted for breaking this type of leakage path [2.10].

Figure 2.7 shows the layout and the cross-section of an NMOS transistor implemented in the radiation hard DMILL process. DMILL is a 0.8μm BiCMOS technology fabricated using a Silicon-On-Insulator (SOI) substrate and providing MOS devices with 20nm gate-oxide thickness. The process is qualified by the foundry for radiation doses up to 10Mrad and 10^{14} n/cm^2 1MeV equivalent. The use of the SOI substrate combined with lateral isolation by trenches, completely eliminates latch-up problems and also reduces the probability of other types of Single Event Effects (SEE) (these phenomena are described later).

In order to avoid the post-radiation leakage problems, the layout of the NMOS transistors in DMILL employs a special mask that defines the source and drain implants inside the thin oxide region (see X-X' cross-section). The edge leakage is eliminated because only thin oxide is present at the source and drain edges. In order to prevent leakage occurring along the poly edges, extra doping is used below the poly gate. The p+ implant region prevents the creation of the inversion layer and shifts the threshold voltage of the parasitic transistor towards safe values (see Y-Y' cross-section).

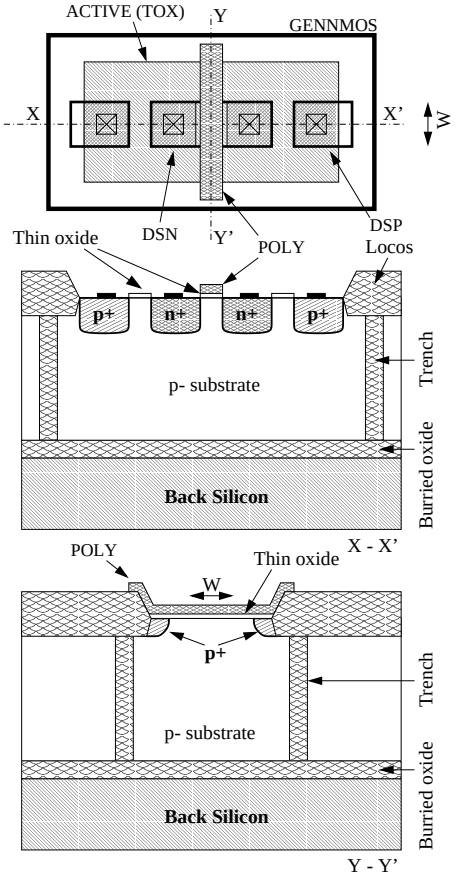


Figure 2.7: Layout and cross-sections of a minimum size NMOS transistor in radiation-hard DMILL technology (not to scale).

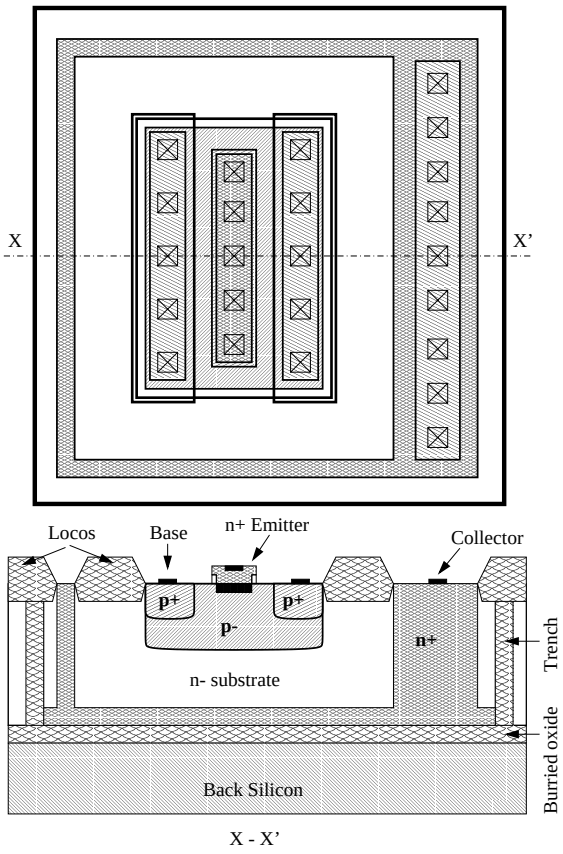


Figure 2.8: Layout and cross-section of a bipolar transistor in DMILL technology. The emitter dimensions are 10×1.2µm (not to scale).

2.2.5. Ionisation damages in BJT transistor [2.12]

Figure 2.8 shows the layout and cross-section of a bipolar transistor implemented in DMILL technology with an emitter size 10µm×1.2µm. This bipolar transistor is used as the input device in the SCTA and ABCD preamplifiers. In junction devices such as BJT transistors, charges trapped in the oxides near the device's surface produce an inversion layer causing an increase of the surface state generation-recombination current. This results in decreased minority carrier lifetime and current gain β in the BJT. The degradation of β is more visible at low collector currents (see Figure 2.10).

One can expect that the susceptibility of the bipolar transistor to ionisation damage will be dependent on the oxide quality. For the DMILL transistor the oxide covering the base is of the same quality as the gate oxide of the MOS transistor, i.e. it is produced using the radiation hard process. Thus the charge trapping in the oxide is kept at reasonable levels and consequently the BJT does not show a high sensitivity to ionisation damage when compare to a standard, commercial bipolar process.

2.3. Displacement damages [2.12]

An incident particle or photon capable of transferring at least 20eV energy to a silicon atom can dislodge it from its lattice site, causing it to take up an interstitial position within the crystal. This results in distortion of the local lattice structure. The displaced atom is called an "interstitial", and the vacated site of the displaced atom is called a

"vacancy". The interstitial-vacancy pair is known as a "Frenkel-defect". If the energy of the incident particle is sufficiently large, it can transfer enough energy to create further interstitials by a cascade process. Finally all displaced atoms will reach thermal equilibrium. Some of them will slip into the vacancies, thereby reconstituting the lattice structure, while the remainder will combine with the impurities or dopants creating stable defects. Because they are electrically inactive they do not act as recombination or trap centres. However, mobile vacancies that combine with impurities or dopant atoms can produce temperature-stable defects called "defect complexes". The defect complexes are effective recombination centres, and they produce changes in the material resistivity and in the minority carrier lifetime. The increase of traps and recombination centres in the depletion regions of a junction leads to an increase the generation current (the current in a reverse biased pn-diode). For forward biased junctions the recombination process causes charge loss (for example lowering the current gain of the BJT).

2.3.1. Recombination and trapping processes

In addition to carrier diffusion, a second mechanism that reduces non-equilibrium carrier concentrations in semiconductors is the recombination process. In equilibrium carrier generation is balanced by the recombination process. Direct band-to-band recombination in silicon is a low probability process. Given that the probability of recombination is an exponential function of the energy difference, the introduction of intermediate energy levels in the forbidden gap due to impurities or crystal defects will enhance the recombination process.

Whether generation or recombination dominates depends on the relative concentrations of carriers and empty defect states. In the depletion region the conduction band is under-populated and the principal process is generation. In a forward biased junction one can expect the recombination process to dominate.

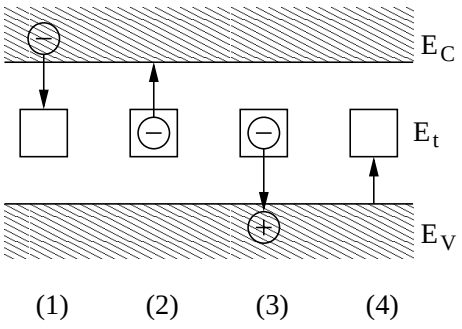


Figure 2.9: Recombination processes.
(1) - Electron capture
(2) - Electron emission
(3) – Hole capture
(4) – Hole emission

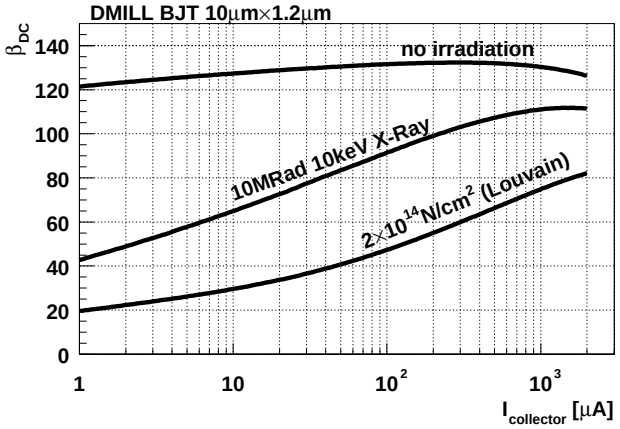


Figure 2.10: DC current gain vs. collector current of a DMILL bipolar transistor with emitter size 10×1.2μm.

Figure 2.9 shows four basic recombination processes occurring in silicon. If the energy level of the mid-gap states has a probability of reemitting the carrier before it recombines it is usually called a "trap". Processes (1) and (2) in Figure 2.9 describe the trapping process of the electron. If the probability of recombination compared to reemission is higher, it is refereed to as a "recombination centre". Processes (1) and (3) depict such recombination. Estimating the probability of these processes, one finds that the traps are

usually located near the bandgap edges, whereas the recombination centres are distributed close to the mid-gap.

2.3.2. Displacement damage in the BJT transistor

Figure 2.8 shows the layout and cross-section of the bipolar transistor used as the input device in the SCTA and ABCD preamplifiers implemented in the DMILL technology. The most important displacement damage consequence in the BJT is the degradation of the current gain β factor. The damage mechanism is a simple formation of mid-gap states in the base of the transistor and the lowering of the minority carrier lifetime due to the recombination processes. The fraction of recombined and lost carriers in the base region depends on the number of defects and the number of injected carriers, and consequently on the collector current density. Therefore for a transistor of a given geometry, the degradation of β will depend on the value of the collector current (see Figure 2.10). Consequently for a given collector current one can expect less degradation in case of smaller transistors. Unfortunately the decrease of the emitter area causes an increase of the base spread resistance, which acts as a significant noise source (see analysis in Chapter 3). The final geometry of the input transistor selected for the front-end amplifiers presented in this thesis is a compromise between the affordable noise contribution from the base spread resistance and the radiation hardness of this device.

The probability of recombination depends on the transit time through the junction region and consequently on the base width. Base width is directly related to the transistor speed and the unity gain frequency f_T. Basically all technologies are optimized for the improvement of the BJT speed, which results in an indirect improvement of the radiation hardness of the bipolar transistors to displacement damage.

Figure 2.10 shows the measured current gain of the DMILL BJT implemented in the input stage of the SCTA and ABCD chips and irradiated with X-Rays up to a TID of 10Mrad and with a fast neutron beam up to a fluence 2×10^{14} n/cm^2 1MeV equivalent. At the nominal bias condition of the transistor working as an input device, which is between 100 and 300μA, the β value remains above 40 after the full neutron fluence. Although quite low, the post-radiation value of beta still ensures the correct functioning of the front-end amplifier, as will be show later in the thesis.

2.4. Single Event Effects (SEE)

Single Event Effects (SEE) are those phenomena caused by high-energy particles passing through the circuit and generating immediate malfunctions, which can either be destructive (Single Event Gate Rupture, Single Event Burn Out) or non-destructive. The latter can be divided in to: Single Event Upset (reversible modification of the logic state) or Single Event Latch-up, which can be non-destructive or destructive.

The continued scaling of CMOS technologies, which is driven primarily by the goal of increased speed of CMOS logic, has a direct impact on the sensitivity of the circuit to soft errors, mainly caused by Single Event Upsets (SEU). The SEU is triggered by the very high-energy deposition in a small volume of the chip, usually in the region of reverse biased p-n junctions. The charge generated along the ionising path is collected and integrated on the parasitic capacitance of the affected node, thereby forming a voltage pulse. Depending on the sensitivity of the node, the transient pulse may change its logic state and create an error. SEU is an important issue for those applications in which some vital control function may be lost due to memory or register upsets.

Decreasing the feature size for modern technologies results in lowering of the parasitic capacitances associated with a single logic gate, and consequently increases the intrinsic susceptibility of the circuits to SEU. In this context we note that there is an extra benefit from the use of enclosed geometry layout for the NMOS transistors, which increases the size of the layout of the logic gate and therefore of its parasitic capacitance, thereby reducing its susceptibility to SEU. The DMILL technology uses as a substrate 1μm epitaxial, oxide-isolated layer, which limits the silicon volume for possible charge deposition and therefore reduces the SEU effects.

The primary methods used for the characterisation of ASICs from the standpoint of their susceptibility to SEU were developed for space applications. The development of a particular method to estimate SEU rates for the electronics at LHC experiments was driven by the specific radiation environment present in the accelerator [2.11]. The test results of the SEU rate for the final version of the ABCD3T chip for ATLAS SCT implemented in DMILL technology can be found in [1.28].

2.5. Radiation effects on integrated circuits

Keeping in mind the expected radiation doses for the LHC front-end electronics one can not ignore radiation effects, even in case of radiation-hard qualified technologies. The shifts of the threshold voltages of MOS transistors, the degradation of the current gain β of the BJTs, and changes in other technological parameters have to be taken into account, even if they can be partially compensated by adjustable bias generators.

In principle the response of the whole integrated circuit to radiation may be predicted with the SPICE program by using the post-radiation parameters of single devices. In practice the post-radiation models are derived for the worst case biasing condition of the single devices i.e. they do not take into account the actual operating points of the simulated devices. This approach gives good results in many cases, such as the simulation of the speed degradation of digital circuits, or the change in the operating point of analogue amplifiers. On the other hand, for analogue circuits relying on matching it may give incorrect results. An example of two different architectures of a Digital-to-Analogue Converter (DAC) is shown in Figure 2.11.

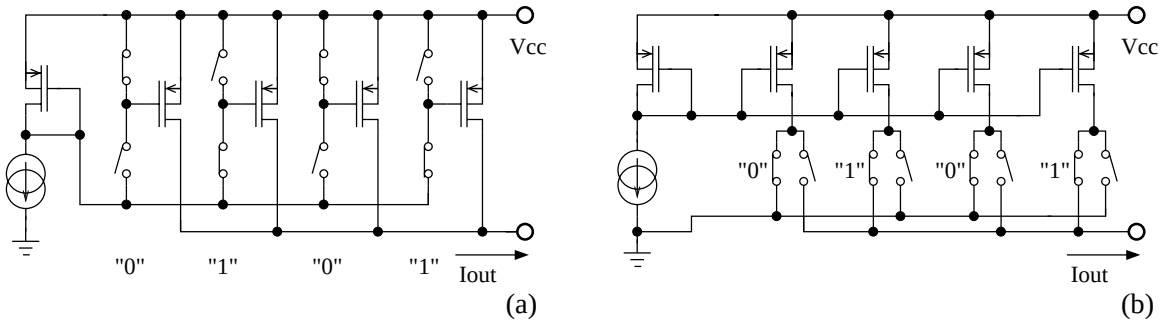


Figure 2.11: Example of two different current DAC architectures: (a) sensitive to the MOS threshold shift and (b) radiation hard.

In simulation both circuits will show equally good performance after irradiation. In reality the threshold voltage of the transistors in circuit (a) will shift depending on the DAC setting, degrading matching and leading to malfunctioning of the circuit. Circuit (b) based on current switching, and providing identical bias conditions for the matched transistors, will show no degradation after irradiation.

In conclusion, the architecture of circuits that are sensitive to the spread of the parameters, especially the threshold of the MOS transistors, must be revised and possible optimised in order to provide equal bias conditions for the matched devices during operation in a radiation environment.

In case of severe degradation of the matching of the diffusion resistors (independent of the bias condition) a possible solution could be the introduction of a special trimming DAC to correct the offset in each electronic channel. The design of the ABCD3T chip has adopted this approach.

2.6. Test considerations

The different time dependences of the ionisation processes that occur in silicon oxide set special requirements on the qualification methods of the electronics for work in the radiation environment. Although the final value of the TID predicted for the LHC tracker electronics is of the order of 10Mrad, one has to remember that this dose will be accumulated over ten years of operation in the experiment. Therefore the expected dose rate will be relatively low, on the order of 2rad/min.

Limited availability of radiation sources, as well as the necessity of collecting the experimental data in a relatively short period of time, imposes the use of much higher dose rates during the characterisation of the constructed electronics. In order that a fast dose rate test procedure can closely emulate the expected TID effect on silicon oxide irradiated in the real radiation environment of the experiment, an accelerated aging step (called annealing) is applied at elevated temperature after the irradiation. The set of procedures developed for qualification of electronics for space missions and for nuclear and military applications are described in documents ESA/SCC-22900 [2.16] and MIL-STD-883 [2.17] respectively.

3. Noise performance of Front-End transimpedance amplifiers built with BJT and MOS devices

As already mentioned, the Front-End amplifiers designed for LHC applications need to operate at sufficiently high speed to achieve the time resolution required to properly tag events with the corresponding beam crossing in which they occurred. Therefore noise performance cannot be improved by applying longer shaping of the signals, which limits the amplifier bandwidth and deteriorates the time resolution.

The analysis presented in this chapter assumes that the shaping stages of the front end amplifiers can be represented by third order CR-RC^3 filter providing a 20ns peaking time of response to the detector signal.

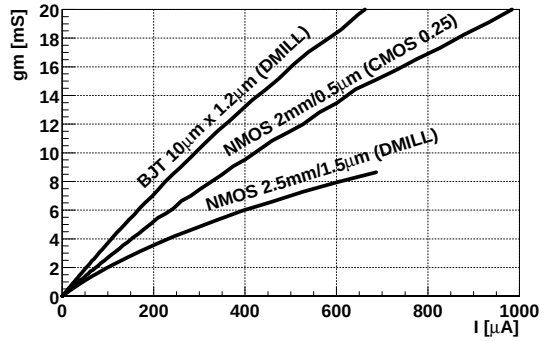


Figure 3.1: Transconductance of BJT and MOS transistors as a function of device current.

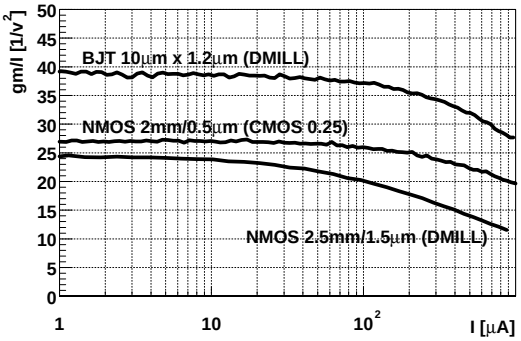


Figure 3.2: Normalized transconductance of various types of transistors as a function of device current.

One method of noise reduction in amplifiers working with capacitive input loads, when serial noise dominates, is to increase the transconductance of the input transistor. In the case of the BJT this can be done by increasing the current supplied to the device; in the case of NMOS devices it can be done by optimization of the transistor size and the increase of the transistor current (Figure 3.1).

Raising the collector current in the BJT transistor causes an increase of the base current (another source of noise), which is proportional to the value of the current amplification factor β.

Increasing the gate width-to-length ratio for the MOS transistor brings the operating point of the transistor closer to the weak inversion region. Consequently we can obtain higher transconductance for the same current provided to the transistor, but with the penalty of higher input capacitance due to the increase of gate area. The weak inversion region of operation of the MOS transistor is characterised by a linear dependence of the transconductance versus the bias current. Figure 3.2 shows normalised transconductance of the BJT and MOS transistors as a function of bias current. The weak inversion region of operation of the MOS device is represented by the flat part of the curve**.**

The analysis presented below searches for the optimal bias conditions and geometries for the various types of transistors and compares the noise performance of front-end amplifiers implemented with those devices in the input stage. Therefore for the purpose of evaluation of the various types of transistors, only the noise related to the input device is considered.

The current that needs to be delivered to the transistor in order to achieve the required noise performance has a direct consequence on the power consumption of the whole chip. As previously pointed out, the available power budget for the front-end readout chips designed for the LHC experiments is limited, and together with the requirements on noise performance and radiation hardness, it is a driving issue for the final choice of the chip architecture and the technology for the implementation.
Although the main application of the front-end circuits presented is the readout of silicon strip detectors with a total capacitance of about 20pF, the analysis is made for an extended range of the input load capacitance. Therefore the capability of the amplifiers to readout a broad variety of particle detectors designed with various geometries is demonstrated.

The comparison of the noise performance of FE amplifiers built with different input devices is made using two technologies as examples. The radiation-hard DMILL technology, available from 1995 offers BJT devices as well as CMOS transistors, the latter with parameters typical of sub-micron technologies with a gate oxide thickness around 20nm. In comparing the noise performance of amplifiers using Bipolar Junction Transistors and DMILL NMOS devices for their input stage, one should remember that the result of that analysis formed the basis of a choice in 1995 for further development of one of the two options. The final chips, including not only the front-end amplifiers but also complicated readout blocks, are today already produced and are starting to be integrated in the experiments. In addition, an analysis of an amplifier implemented in the IBM 0.25μm CMOS technology, which has now become accessible to the HEP community, shows the potential of that technology to build a front-end amplifier with the analogue performance required by the tracker systems at the LHC experiments. All the results presented from the IBM 0.25μm version of the Front-End electronics are derived from prototypes submitted in the year 2001.

When it is not specified, the analysis of the bipolar Front-End is made using the example of the DMILL BJT transistor with an emitter size 1.2μm×10μm. Compared to the minimum geometry BJT, with an emitter size 1.2μm×1.2μm, it shows a significantly lower value of base spread resistance, good stability of the β parameter with respect to the collector current and a reasonable radiation hardness.

The choice of the gate length of the NMOS transistors in the DMILL and IBM 0.25μm technologies was determined by minimization of the excess noise factor Γ, which becomes worse in short-channel devices. The gate lengths: 1.2μm for the DMILL NMOS transistor and 0.5μm for the IBM 0.25μm version are optimal from this point of view for both technologies. Additional increases of the gate length do not affect the Γ factors and lead to enlargement of the total gate area, which consequently degrades the noise performance. The significant difference between the optimum values of the gate lengths for DMILL and IBM 0.25μm transistors shows a substantial improvement of the analogue performance in modern CMOS technologies.

For the purpose of the analysis that follows, Table 3.1 defines the constants and symbols used in the formulae.

Table 3.1: Definition of physical constants used in calculations.

Symbol	Constant description	Value	Units
k	Boltzmann's constant	1.3806×10^{-23}	Joules/°K
q	Electron charge	1.6021×10^{-19}	C
ε_{ox}	Permitivity of SiO_2	3.45×10^{-11}	F/m
T	Temperature		°K
f	Frequency		[Hz]
ω	*Angular frequency*	$2\pi f$	[rad/sec]

3.1. Noise sources in Bipolar Junction Transistor

In order to analyze the noise performance of a FE amplifier stage built with bipolar devices I follow the ideas summarised by A. Van Der Ziel [3.1]. A short compilation of the ideas related to devices working in common emitter configuration follows.

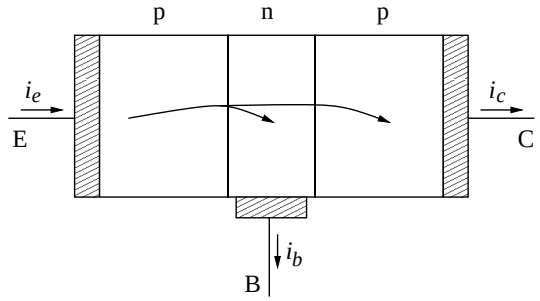


Figure 3.3: Current flow in the p-n-p Bipolar Junction Transistor (the entire current is carried by the holes).

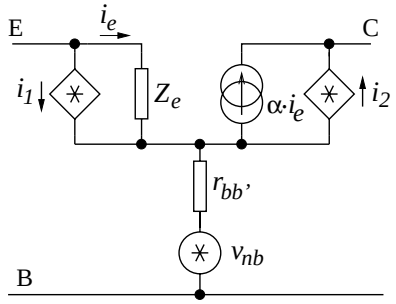


Figure 3.4: Equivalent circuit of the transistor showing current flow and corresponding noise sources.

The current flow in the BJT is shown in Figure 3.3, for the case of a p-n-p transistor where the entire current is carried by the holes. We consider only holes injected into the base and partly collected by the collector. They give contributions to the emitter current I_E and the collector current I_C. Each of these current components contributes a full shot noise which is represented in Figure 3.4 by noise sources i_1 and i_2. The current amplification factor α is the ratio of the collector current to the emitter current.

$$\overline{i_1^2} = 2 \cdot q \cdot I_E \Delta f \tag{3.1}$$

$$\overline{i_2^2} = 2 \cdot q \cdot I_C \Delta f \tag{3.2}$$

At low frequencies the transfer of the holes through the base to the collector can be considered as an instantaneous process. Since the currents I_E and I_C have a current αI_E in common we can evaluate the correlation term for noise sources i_1 and i_2:

$$\overline{i_1^* i_2} = 2 \cdot k \cdot T \cdot g_m \Delta f \tag{3.3}$$

In the above equation we have used the fact that the transconductance g_m of the transistor defined as $\frac{\partial I_C}{\partial V_{BE}}$ can be calculated as the following:

$$g_m = \frac{q \cdot I_C}{k \cdot T} \tag{3.4}$$

At high frequencies, holes injected simultaneously by the emitter, will arrive at the collector with different delays, because their diffusion is a random process. Because the noise is affected in the same way as the signal one can expect that at high frequency the correlation term is proportional to the high frequency transconductance Y_m:

$$\overline{i_1^* i_2} = 2 \cdot k \cdot T \cdot Y_m \Delta f \tag{3.5}$$

In addition to the current noise sources i_1 and i_2, one should also take into account the thermal noise from the parasitic contacts and the bulk resistances. One of the most important parasitic parameters is the base spread resistance represented in Figure 3.4 by the resistor $r_{bb'}$ with its voltage noise source v_{nb} :

$$\overline{v_{nb}^2} = 4 \cdot k \cdot T \cdot r_{bb'} \, \Delta f \tag{3.6}$$

The equivalent circuit of the transistor working in common emitter configuration including the noise sources is shown in Figure 3.5. It consists of a current generator $i_b = i_1 - i_2$ connected in parallel with base-emitter admittance and current generator i_2 placed between collector and emitter.

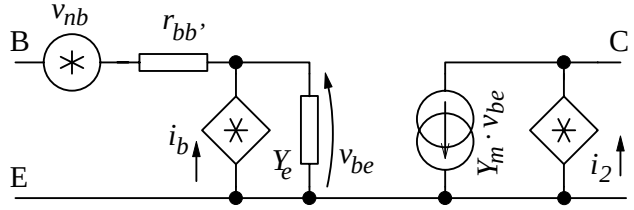


Figure 3.5: Equivalent circuit of the transistor in common emitter configuration including the noise sources.

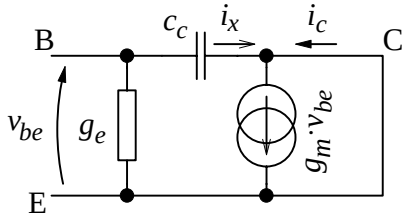


Figure 3.6: Current flows in the equivalent circuit working with shorted output considering base-collector capacitance for calculation of Y_m.

The current gain β in the common emitter configuration is defined as the ratio between collector and base currents. The noise spectra density of current generator i_b may be calculated as following:

$$\overline{i_b^2} = \overline{(i_1 - i_2) \cdot (i_1^* - i_2^*)} = \overline{i_1^2} + \overline{i_2^2} - 2 \cdot \mathrm{Re}(\overline{i_1^* i_2}) = 2 \cdot q \cdot (I_E + I_C) \Delta f - 4 \cdot k \cdot T \cdot \mathrm{Re}(Y_m) \Delta f \tag{3.7}$$

where "Re" stands for real part, and $I_E - I_C = \dfrac{I_C}{\beta}$ is a base current. Consequently the equation can be transforms to:

$$\overline{i_b^2} = 2 \cdot q \cdot \frac{I_C}{\beta} \Delta f + 4 \cdot k \cdot T \cdot (g_m - \mathrm{Re}(Y_m)) \Delta f \tag{3.8}$$

For $\overline{i_b^* i_2}$ one can write:

$$\overline{i_b^* i_2} = \overline{(i_1^* - i_2^*) \cdot i_2} = \overline{i_1^* \cdot i_2} - \overline{i_2^2} = 2 \cdot k \cdot T \cdot Y_m \Delta f - 2 \cdot q \cdot I_C \Delta f = 2 \cdot k \cdot T \cdot (Y_m - g_m) \Delta f \tag{3.9}$$

The high frequency transconductance Y_m can be determined, as for any two-port network, by measurement of the current at the short circuited output. Figure 3.6 shows the part of the equivalent circuit of the transistor in common emitter configuration with shorted output. The equivalent circuit presented includes the base-collector Miller capacitance c_c, which is responsible for the high frequency fraction of the transconductance Y_m. Summing the currents at the output of the circuit we have:

$$i_X + i_C - g_m \cdot v_{be} = 0 \tag{3.10}$$

Since $i_X = j \cdot \omega \cdot c_c \cdot v_{be}$ (3.11)

and Y_m is defined as $\partial I_C / \partial v_{be}$, one can calculate Y_m to be:

$$Y_m = g_m - j \cdot \omega \cdot c_c \tag{3.12}$$

Therefore one can simplify the equations (3.8) and (3.9) to:

$$\overline{i_b^2} = 2 \cdot q \cdot \frac{I_C}{\beta} \Delta f \tag{3.13}$$

$$\overline{i_b^* i_2} = 2 \cdot k \cdot T \cdot (-j \cdot \omega \cdot c_c) \Delta f \tag{3.14}$$

3.2. Calculation of the output noise for the bipolar preamplifier stage

In order to calculate the Equivalent Noise Charge in a transresistance amplifier with a CR-(RC)^3 filter one has to start from the analysis of the transresistance preamplifier stage. The equivalent schematic of the stage, including the noise sources discussed in the previous section, is shown in Figure 3.7.
The detailed analysis of the propagation of the noise sources related to the input transistor, to the preamplifier output, has been made in Appendix 7.1.

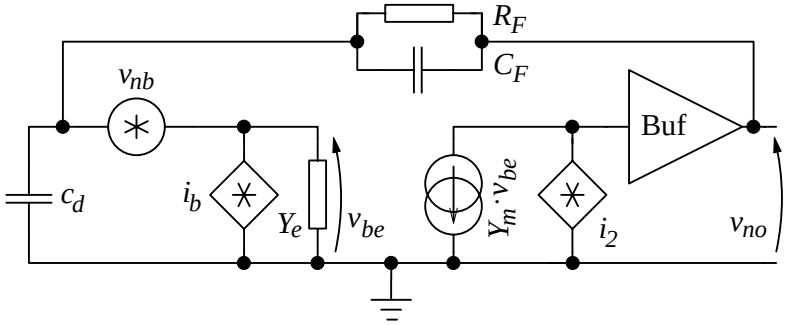


Figure 3.7: Equivalent schematic of the transresistance preamplifier with BJT input transistor including the noise sources.

Initially describing all noise components in the time domain, one can distinguish the following noise sources with their final contribution to the output noise of the bipolar preamplifier.
The noise generated by base spread resistance $r_{bb'}$ seen at the amplifier output v_{no_rbb}, will be equal to (equation 7.7):

$$v_{no\_rbb}(t) = v_{nb}(t) \cdot Z_F \cdot (Y_d + Y_F) \quad \text{where} \quad Y_d = j \cdot \omega \cdot c_d \quad \text{and} \quad Y_F = \frac{1}{R_F} + j \cdot \omega \cdot C_F \tag{3.15}$$

The contribution to the output noise from the i_2 shot noise generator v_{no_i2}, neglecting the imaginary part of Y_m will be as follows (equation 7.14):

$$v_{no\_i2}(t) = \frac{i_2(t)}{g_m} \cdot Z_F \cdot (Y_F + Y_e + Y_d) \tag{3.16}$$

Neglecting the imaginary part of Y_m will create an error in evaluation of the transconductance of the device at high frequency. For transistor transconductances above 5mS and capacitances c_c below 200fF the maximum error at 100MHz is less than 2%. Taking into account simplification of the future calculation and the fact that the central frequency of our filter is around 10MHz, the error from the above approximation is fully acceptable.
The contribution to the output noise from the i_b noise generator is as follows (equation 7.19):

$$v_{no\_ib}(t) = i_b(t) \cdot Z_F \tag{3.17}$$

The noise v_{no}, seen at the amplifier output will be the sum of the contributions from the $r_{bb'}$, i_2 and i_b noise generators.

$$v_{no}(t)=v_{no\_rbb}(t)+v_{no\_i2}(t)+v_{no\_ib}(t) \tag{3.18}$$

In order to calculate the noise spectrum at the preamplifier output related to all the mentioned noise sources, one has to go to the frequency domain i.e. find the Fourier representations of all terms of equation (3.18). Since the collector and base current shot noise are correlated, and the correlation factor depends on frequency, the correlation term has to be depicted separately. This can be done using the Wiener-Khintchine theorem for more variables described well in [3.1]. The full analysis made in Appendix 7.2 results in following expression for the output noise spectral density for a preamplifier built with a BJT.

$$\frac{\overline{v_{no}^2}}{\Delta f}=\frac{\overline{v_{no\_rbb}^2}}{\Delta f}+\frac{\overline{v_{no\_i2}^2}}{\Delta f}+\frac{\overline{v_{no\_ib}^2}}{\Delta f}+\frac{\overline{v_{no\_corr}^2}}{\Delta f} \tag{3.19}$$

The noise spectra densities related to the thermal noise of the $r_{bb'}$, shot noise of the collector and base currents, as well as to the correlation term are described by the following equations (Appendix 7.2, equations 7.35, 7.37, 7.38 and 7.39):

$$\frac{\overline{v_{no\_rbb}^2}}{\Delta f}=4\cdot k\cdot T\cdot r_{bb}^{'}\cdot\left(\omega^2\cdot\left(c_d+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.20}$$

$$\frac{\overline{v_{no\_i2}^2}}{\Delta f}=\frac{2\cdot k\cdot T}{g_m}\cdot\left(\omega^2\cdot\left(c_d+c_e+C_F\right)^2+\left(\frac{g_m}{\beta}+\frac{1}{R_F}\right)^2\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.21}$$

$$\frac{\overline{v_{no\_ib}^2}}{\Delta f}=2\cdot q\cdot\frac{I_C}{\beta}\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.22}$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f}=\frac{4\cdot k\cdot T}{g_m}\cdot\omega^2\cdot\left(c_d+c_e+C_F\right)\cdot c_c\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.23}$$

The base spread resistance and collector current shot noise, with its equivalent noise resistance $1/(2\cdot g_m)$, represent series noise sources. Comparing the expressions (3.20) and (3.21) it can be seen that the noise spectral densities of $r_{bb'}$ and the collector current shot noise contribute to the output noise with different weights. This is due to the fact that the voltage noise source related to the $r_{bb'}$ resistance is shared between the input impedance of the transistor ($Z_e=1/Y_e$) and detector and the feedback impedances. The simplified[1] scaling factor (equation 3.24) considering only the capacitive part of the feedback and the BJT input impedance for $r_{bb'}$ and collector current shot noise contributions is identical to the factor**,** which can be found in the literature [3.11] calculated for the bipolar charge preamplifier ($R_F \rightarrow \infty$):

[1] This simplification does not work very well for low detector capacitances and certain region of biases where one can see not negligible contribution from real part of the input impedance of the transistor (see Figure 3.9a).

$$\frac{\overline{v_{no\_rbb}^2}}{\overline{v_{no\_i2}^2}} \sim \frac{(c_d + C_F)^2}{(c_d + c_e + C_F)^2} \tag{3.24}$$

3.3. Calculation of the equivalent input noise for the bipolar transresistance amplifier working with triple integrator (CR-(RC)^3 filter)

The equivalent schematic of the Front-End amplifier including the shaper stage denoted by the transfer function $H(j\omega)$ is shown in Figure 3.10.

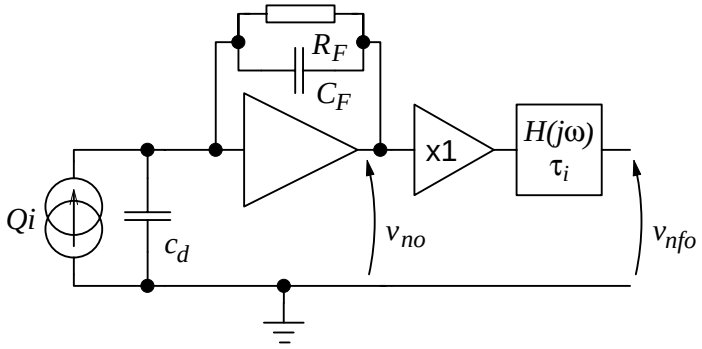


Figure 3.8: Equivalent schematic of the Front-End amplifier including the shaper stage with transfer function H (jω).

The current source *Qi* represents signal charge from the detector. The noise spectral density at the preamplifier output, v_{no}, is described by equation (3.19). Assuming that the shaper stage is a triple integrator with the integration time constant τ_i equal to the time constant of the preamplifier feedback τ_f, one can write the spectrum density of the noise at the shaper output v_{nfo} as:

$$\frac{\overline{v_{nfo}^2}}{\Delta f} = \frac{\overline{v_{no}^2}}{\Delta f} \cdot |H(j\omega)|^2 = \frac{\overline{v_{no}^2}}{\Delta f} \cdot \frac{1}{\left(1 + \tau_f^2 \cdot \omega^2\right)^3} \tag{3.25}$$

where $\frac{\overline{v_{no}^2}}{\Delta f}$ is described by equation 3.19.

Integrating the noise spectrum density $\overline{v_{nfo}^2}$ over the full frequency range starting from zero to infinity, one obtains the following expression for the rms noise σ_{nfo} at the shaper output:

$$\sigma_{nfo} = \left(\int_0^\infty \left(\frac{\overline{v_{no\_rbb}^2}}{\Delta f} + \frac{\overline{v_{no\_i2}^2}}{\Delta f} + \frac{\overline{v_{no\_ib}^2}}{\Delta f} + \frac{\overline{v_{no\_corr}^2}}{\Delta f} \right) \cdot \frac{1}{\left(1 + \tau_f^2 \cdot \omega^2\right)^3} \partial f \right)^{\frac{1}{2}} \tag{3.26}$$

The Front-End amplifier processes the charge signals delivered by the silicon detector and outputs voltage signals. Therefore the equivalent input noise for the front-end amplifier can be described in terms of a quantity of charge, which is commonly referred to as an Equivalent Noise Charge (ENC). In chapter 1 the analysis of a front-end amplifier with

the CR-RC^3 shaper type gave the following expression for the pulse amplitude of the response to the input signal charge *Qi*:

$$A_{CR-RC3}=\frac{9}{2\cdot e^3}\frac{Qi}{C_F}=G_{CR-RC3}\cdot Qi \tag{3.27}$$

The factor $G_{CR\text{-}RC3}$ represents the charge gain of the Front-End amplifier. Consequently one can present the following expression for ENC given in Coulombs for a transresistance amplifier working with triple integrator:

$$ENC\,[C]=\frac{\sigma_{nfo}}{G_{CR-RC3}} \tag{3.28}$$

Often the ENC is specified in terms of a number of electrons. Therefore the *ENC* [*e*-] will be equal to *ENC*[*C*]/*q* where q is the charge of an electron.
In order to simplify the analysis and for better transparency, each term of equation (3.26) can be integrated separately to find the partial contributions to the ENC from the corresponding noise sources. The final number for the ENC is obtained by a quadratic addition of the partial contributions.

3.3.1. ENC contribution from the collector current shot noise

The ENC contribution from the collector current shot noise can be calculated similarly to the previous section and using expression (3.21) as follows:

$$ENC_{Ic}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{2\cdot k\cdot T}{g_m}\cdot\left(\omega^2\cdot\left(c_d+c_e+C_F\right)^2+g_{if}^2\right)\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.29}$$

For better transparency the term $\frac{g_m}{\beta}+\frac{1}{R_F}$ was replaced by the equivalent transconductance g_{if}, which representing the input and feedback circuit.

Solving the definite integral one can obtain the following expression for an equivalent noise charge originating from the collector current shot noise:

$$ENC_{Ic}[e^-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{\frac{2\cdot k\cdot T}{g_m}}\cdot\sqrt{\left(c_d+c_e+C_F\right)^2+5\cdot\tau_f^2\cdot g_{if}^2}\cdot\frac{1}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.30}$$

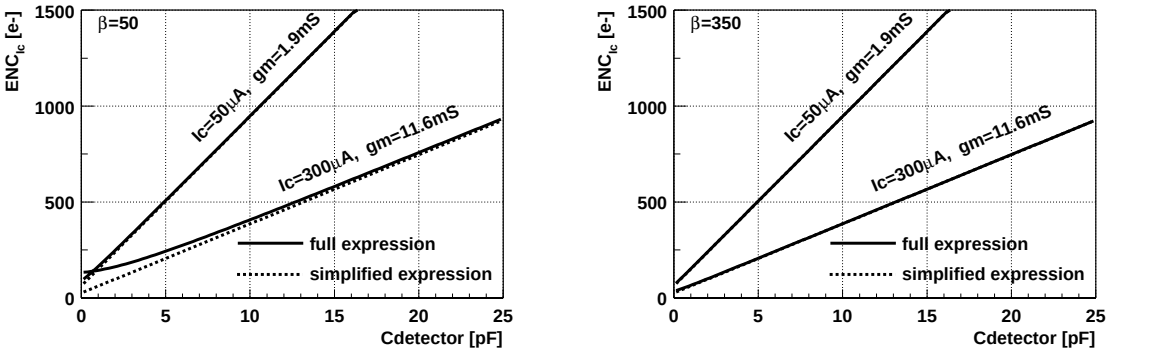
where $t_{peak}=3\cdot\tau_f$

For typical values of c_e of the bipolar transistor in the range of 0.5 to 1pF, the feedback time constant in the range of a few nanoseconds, and the input resistance $r_e=\beta/g_m$ above 5 kΩ, equation (3.30) for a detector capacitance above 5pF can be simplified to:

$$ENC_{Ic}[e^-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{\frac{2\cdot k\cdot T}{g_m}}\cdot\frac{c_d+c_e+C_F}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.31}$$

As can be seen in Figure 3.9a the discrepancy between the simplified and the exact equation can be observed only at low input capacitances and for low values of the input resistance r_e i.e. low beta and high collector current. Even so, under these conditions, the error in the estimated total value for ENC will be completely negligible, because the collector current shot noise will be masked by the shot noise of the base current, which dominates at low detector capacitances (see Figure 3.10).

In the final expressions for the ENC we use the peaking time of the amplifier response t_{peak} instead of the time constant of the filter τ_f. Making that conversion has significant advantages. It allows direct comparison between ENC figures of FE amplifiers with filters of different orders although having the same central frequency. In addition, the peaking time can be measured directly from the amplifier response. According to the calculation made in Chapter 1, for CR-RC^3 type shapers t_{peak} is equal to $3\,\tau_f$.



(a) *(b)*

Figure 3.9: ENC originating from collector current shot noise versus input capacitance for different bias currents and BJT beta values equal to 50 (Figure a) and 350 (Figure b).The difference between simplified and exact formulae for ENC_{Ic} is visible only for low beta and higher (300μA) collector current (low Z_e).

One can see that the contribution from the collector current shot noise is proportional to the detector capacitance and inversely proportional to the square root of the peaking time and the transconductance of the input transistor. The ENC figures calculated according to equation (3.30) for different values of g_m, assuming 20ns peaking time, as a function of input capacitance are shown in Figure 3.9a and 3.9b for β equal to 50 and 350 respectively. One can observe a difference between the exact and simplified expressions for ENC_{Ic} occurring for low input impedance of the BJT, i.e. for the combination of low beta and high collector current (Figure 3.9a, lower traces).

3.3.2. ENC contribution from the base current noise generator

Using the same method and definition for the output noise spectral density caused by base current from equation (3.22) one can calculate the ENC contribution from the base current noise generator:

$$ENC_{Ib}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{2\cdot q\cdot I_C}{\beta}\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.32}$$

Solving integral (3.32) we obtain the final expression for the ENC:

$$ENC_{Ib}[e^-]=\frac{e^3}{36}\cdot\sqrt{\frac{5}{3}}\cdot\sqrt{t_{peak}}\cdot\sqrt{\frac{2\cdot q\cdot I_C}{\beta}}\cdot\frac{1}{q} \tag{3.33}$$

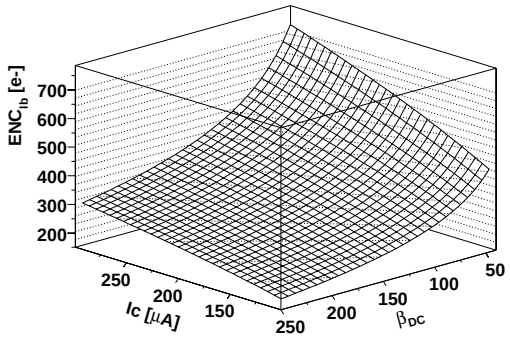


Figure 3.10: ENC contributed by base current shot noise as a function of bias currents and beta of the BJT.

It can be seen that the contribution from the base current shot noise is proportional to the square root of the peaking time and the base current of the input transistor. As for any parallel noise source it is independent of the input capacitance. The ENC figure originating from the base current shot noise for different values of bias and 20ns peaking time is shown in Figure 3.10. For the bipolar transistor working with collector current below 300μA it may vary from 200 to 700 e-, depending on the value of the transistor current gain β.

3.3.3. Contribution of the base spread resistance $r_{bb'}$ to the Equivalent Noise Charge

Solving the following definite integral leads to the expression for the ENC contribution from base spread resistance.

$$ENC_{rbb}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}4\cdot k\cdot T\cdot r_{bb'}\cdot\left(\omega^2\cdot\left(c_d+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.34}$$

$$ENC_{rbb}[e^-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{4\cdot k\cdot T\cdot r_{bb'}}\cdot\sqrt{\left(c_d+C_F\right)^2+5\cdot C_F^2}\cdot\frac{1}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.35}$$

Usually the feedback capacitance C_F is in the range of tens of fF, i.e. is much smaller than the detector capacitance or parasitic capacitance connected at the preamplifier input (but outside the feedback loop). Therefore one can neglect the term containing its square and simplify equation (3.35) to:

$$ENC_{rbb}[e^-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{4\cdot k\cdot T\cdot r_{bb'}}\cdot\frac{\left(c_d+C_F\right)}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.36}$$

The final value of the ENC is proportional to the detector input capacitance c_d summed with the feedback capacitance C_F. Figure 3.11 shows the ENC contribution from $r_{bb'}$ as a function of input capacitance and biasing conditions for a preamplifier connected to a shaper with 20ns peaking time. The calculation of the ENC is made for two examples of DMILL bipolar transistors with emitter sizes 2×10μm×1.2μm and 10μm×1.2μm. The base spread resistances are equal to 90 and 180Ω respectively (see the measurement of the base spread resistance of DMILL transistors given in Appendix 7.5).

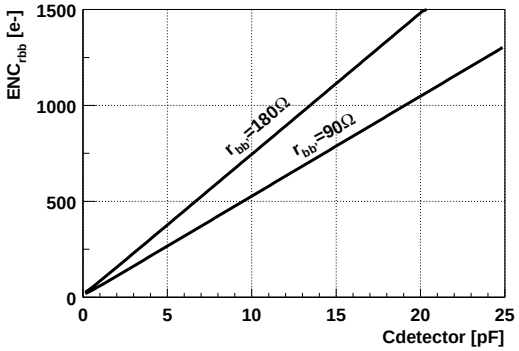


Figure 3.11: ENC figures related to the base spread resistance as a function of input capacitance for various values of the $r_{bb'}$.

From the point of view of noise performance, the bigger transistor could provide at least 30% lower contribution of noise to the total ENC. Unfortunately the radiation hardness of the BJT is worse for the bigger devices. This concerns particularly the degradation of β, which is proportional to the emitter area and the current density in the transistor. For the ATLAS semiconductor tracker, when the final radiation doses are in the range of 10Mrads and $2\times10^{14}$of 1MeV equivalent neutrons per square centimetre, the β of the bipolar transistors with the emitter area 10μm×1.2μm measured for the nominal (200-300μA) collector current can be degraded down to 40 (see Figure 2.10). Therefore the choice of the optimal transistor geometry for the final version of the Front End amplifier is dictated by the improvement of the radiation hardness of the device and general robustness of the design, sacrificing a little bit the noise performance. Nevertheless the analysis presented yields a general model, which could be used for the optimization of noise performance of front end amplifiers designed for similar applications, but not limited by the radiation hardness constraints.

3.3.4. Contribution from the correlation term to the Equivalent Noise Charge

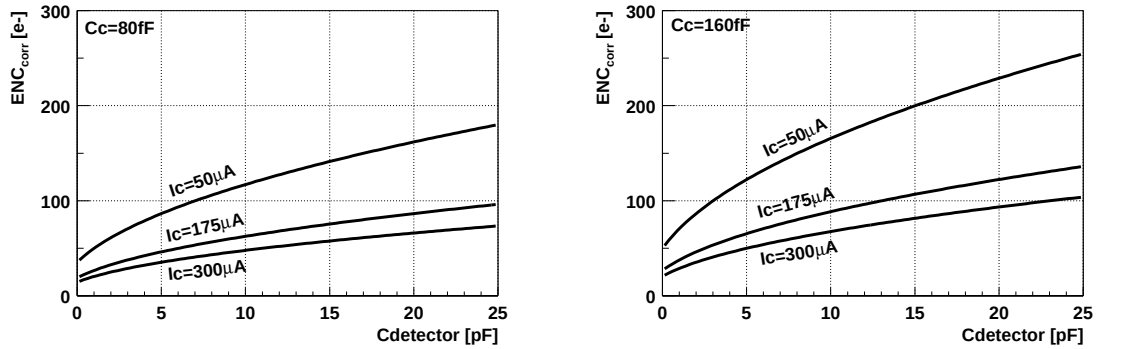
The calculation of the partial contribution from the correlation term is made as for the other noise sources. Solving the following definite integral gives the ENC contribution from the correlation term:

$$ENC_{corr}=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{4\cdot k\cdot T}{g_m}\cdot\omega^2\cdot\left(c_d+c_e+C_F\right)\cdot c_C\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.37}$$

Consequently we obtain:

$$ENC_{corr}[e^-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{\frac{4\cdot k\cdot T}{g_m}}\cdot\frac{\sqrt{\left(c_d+c_e+C_F\right)\cdot c_C}}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.38}$$

The correlation term contribution is proportional to the square root of the input capacitance and inversely proportional to the square root of the peaking time. Figures 3.12a and 3.12b plot the ENC originating from the correlation term as a function of input capacitance for two different examples of the DMILL transistors, with emitter sizes of 10μm×1.2μm and 2×10μm×1.2μm, and under different bias conditions. The capacitances c_c for these two transistors are equal to 80 and 160fF respectively.



(a) *(b)*

Figure 3.12: The Equivalent Noise Charge originating from the correlation term for the BJT transresistance amplifier with 20ns peaking time versus different bias condition and beta gain for low (a) and high (b) c_c capacitances.

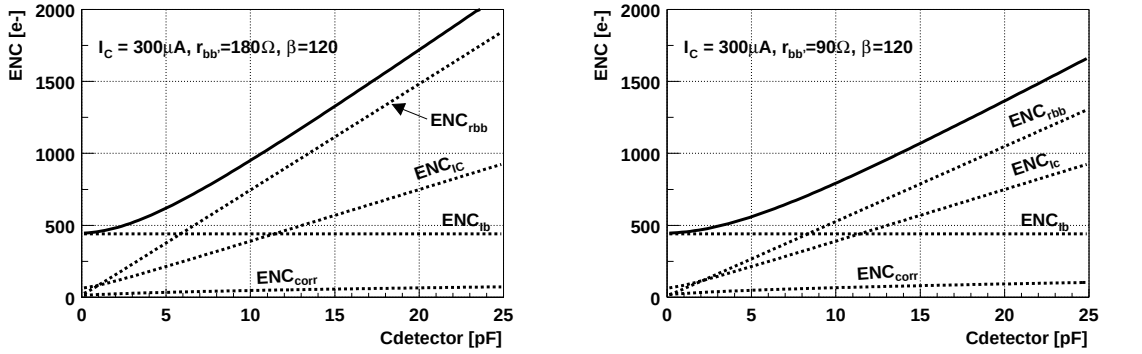
Comparing the values of the ENC related to the correlation term with the other sources of noise one can easily notice that the correlation term does not make a large contribution to the total ENC figure. This is because of the fact that the central frequency of the analyzed filter is in the range of 10MHz. At that frequency the correlations are still small, especially for the transistor sizes considered for our applications. Limiting the transistor sizes, basically in order to improve radiation hardness of the transistor reduces the base-to-collector capacitance c_c, which is responsible in the noise model for the correlations.

3.3.5. Final ENC figure for the BJT amplifier

The final ENC figure considering all the previously mentioned noise sources can be obtained by quadratic summation of the partial contributions:

$$ENC = ENC_{Ic} \oplus ENC_{Ib} \oplus ENC_{rbb} \oplus ENC_{corr} \tag{3.39}$$

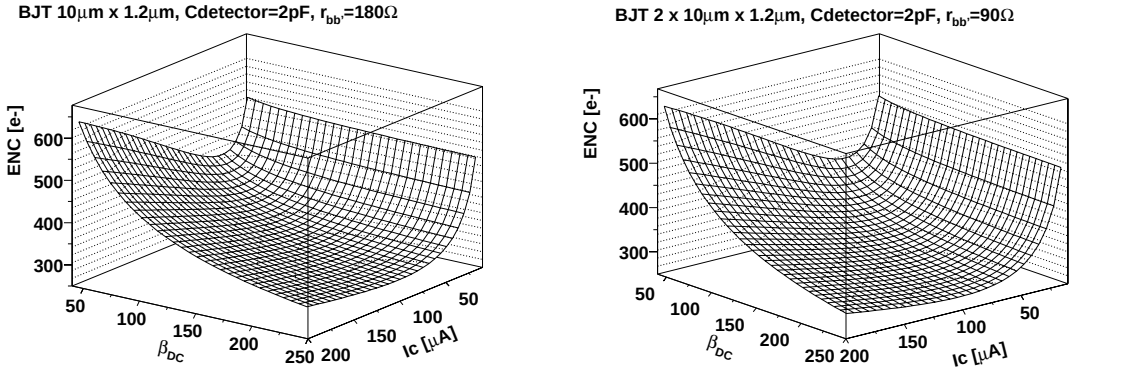
Figures 3.13 (a) and (b) show the example of the ENC figure calculated as a function of the input capacitance for one particular bias condition (high collector current and nominal beta). The comparison between two examples of the BJT transistors shows that in both cases the dominant contributor of noise under those bias conditions is the base spread resistance. It sets a basic limitation to the improvement of the noise performance by increasing the device transconductance. Of course, for applications which do not require radiation hard electronics, the radiation hardness constraints can be ignored and one can use input transistors with larger emitter area and consequently lower $r_{bb'}$. Therefore, in order to optimize the size of the input transistor, one has to compare the contributions from the base spread resistance and the correlation term, which will be rising with the transistor size and c_c. Obviously, looking at the low frequency application, the correlation will not be important anymore, and therefore the increase of the transistor size will be limited by another constraint, like the required bandwidth of the amplifier, which decreases for bigger transistors.



(a) *(b)*

Figure 3.13: The Equivalent Noise Charge showing the partial contributions for bipolar transresistance amplifier with 20ns peaking time versus detector capacitance for BJT 2×10×1.2μm (a) and BJT 10×1.2μm (b) input transistors.

The final plots showing the ENC versus bias condition and beta gain for two different values of the detector capacitances and for two examples of the BJT transistors of different size are presented in the figures 3.14a to 3.15b. The calculations have been made assuming 20ns peaking time of the shaper and relevant values of c_c and $r_{bb'}$ for the used transistors.



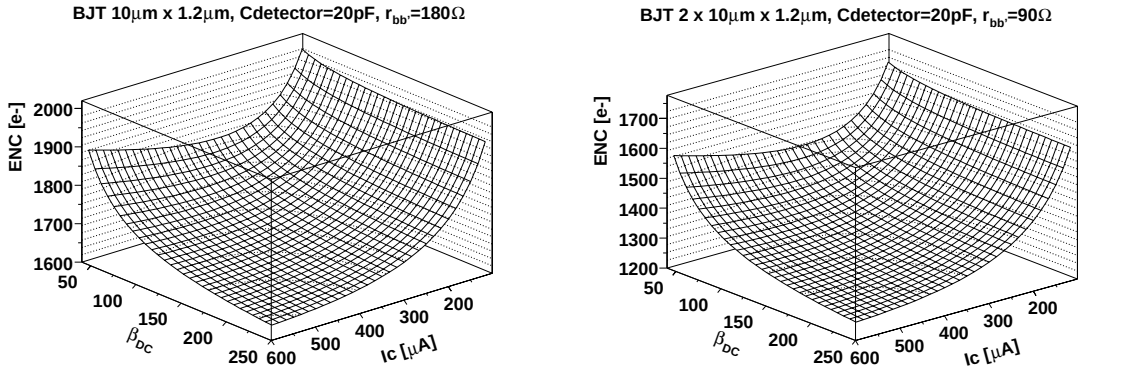
(a) *(b)*

Figure 3.14: The Equivalent Noise Charge for the BJT transresistance amplifier with 20ns peaking time versus different bias condition and beta gain for low 2pF detector capacitance. Comparison of noise performance between the BJT 10×1.2μm (a) and BJT 2×10×1.2μm (b) input transistor.

One can see that for the detector capacitances in the range of 2pF the differences in noise performance of the two presented BJT devices are negligible (Figure 3.14 (a) and (b)). This is due to the fact that the contribution from the $r_{bb'}$ is proportional to the detector plus feedback admittance, while the collector current shot noise contributes proportionally to the total admittance of feedback, detector and the input admittance of the transistor, which is complex in the general case (see equations (3.30) and (3.36)). This effect can be observed in Figure 3.13, where for low input capacitances the base spread resistance contribution is lower than the collector current shot noise. As a result, one can observe linearization of the final ENC figure as a function of the detector capacitance.

Figure 3.15 shows the comparison between noise performance of two analyzed BJT transistors for 20pF detector capacitance. A transistor with 10×1.2μm emitter area working in the range of 300μA collector bias, and having a beta gain above 100, yields in

the range of 1600 to 1700e$^-$ ENC. This result is worse by about 200e$^-$ ENC compared to the bigger transistor. As already mentioned, the choice of final geometry for the LHC application will be driven also by the radiation hardness of the device, which is still satisfactory for the smaller device (see Chapter 2) but not acceptable for the bigger transistor, where the beta parameter drops below 30 after the full radiation dose.



(a) *(b)*

Figure 3.15: The Equivalent Noise Charge for the BJT transresistance amplifier with 20ns peaking time for different bias conditions and beta gains, for a high 20pF detector capacitance. Comparison of the noise performance between the BJT 10×1.2μm (a) and BJT 2×10×1.2μm (b) input transistors.

The optimum bias current providing the lowest ENC for a transistor of nominal beta around 120 is between 300 and 400μA and towards the higher values of beta[2] it increases above 600μA. One has to remember that the operating point of the input transistor is determined not only by the optimisation of the noise performance but also by the power consumption budget. The nominal bias current of the input transistor for non-irradiated SCTA128VG and ABCD3T chips is limited to 300μA because of the maximum affordable power consumption of the FE electronics. During operation in the radiation environment, the optimum bias current will decrease due to the beta degradation caused by the radiation damage. In the case of bipolar transistors with post-radiation values of beta in the range of 40, the optimum value of the collector current is between 150 and 200μA.

3.4. Modelling of MOS devices using the EKV model

In order to describe accurately the noise performance of the MOS transistor one has to precisely calculate the electrical parameters for a given value of the bias current. Because of the power constraints, the analyzed Front-End amplifiers will use MOS devices operated in weak and moderate inversion. Therefore one has to use a model accurately describing behavior of the MOS transistor in those regimes. A fully analytical MOS transistor model suitable for low-current applications and proposed by C.Enz, F.Krummenacher and E.Vittoz (EKV) is described in reference [3.4]. It provides continuity between weak, moderate and strong inversion regions for all large- and small-signal variables, such as transconductance and intrinsic capacitances. Since our analysis is focused on the noise performance of MOS devices, one can simplify the general model to

[2] For non-irradiated DMILL bipolar transistors beta can vary between 90 and 350 for different production lots.

the case of the transistor working in saturation, between weak and moderate inversion regions.

Table 3.2: Definition of model parameters for DMILL and IBM 0.25μm NMOS transistors.

Symbol	Parameter description	Value	Technology
n	Slope factor	1.5	DMILL
		1.45	IBM-0.25
t_{OX}	Effective gate oxide thickness	18×10^{-9} [m]	DMILL
		6×10^{-9} [m]	IBM-0.25
K_P	Transconductance parameter - $\mu_0 \cdot C_{OXU}$	82 [μA/V^2]	DMILL/NMOS
		300 [μA/V^2]	IBM-0.25/NMOS
		70 [μA/V^2]	IBM-0.25/PMOS
W	Transistor width [μm]		
L	Channel length [μm]		

The assumption that the transistor will not operate in the strong inversion region allows use of constant values for the slope factor n and the electron surface mobility μ_0, which are usually bias dependent. These assumptions substantially limit the number of variables and equations without any degradation of the accuracy for the analyzed case. The definitions of model parameters and variables used for the DMILL and IBM 0.25μm technologies are given in table 3.2. The slope factor n has been extracted from measurements of the transconductance of transistors working in weak inversion. The other parameter values are given by the foundries.

3.4.1. Modelling the transconductance

The EKV model uses a semi-empirical approach in which different regions of operation, namely weak and strong inversion, are described by different physical functions. The parameters of the transistor for moderate inversion are obtained from the empirically found interpolation function, which has continuous first and second derivatives.

In the EKV model the current has to be normalized in order to obtain a relation between the current and the voltages that is independent of the technology parameters and the transistor dimensions. The specific current *Is*, used for the normalization is described by the equation [3.4]:

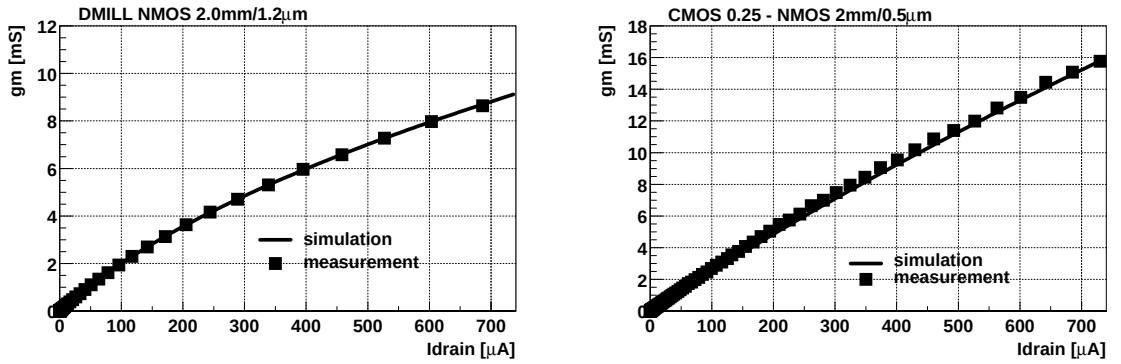
$$I_S = 2 \cdot n \cdot \beta \cdot U_T^2 \quad \text{where } \beta = K_P \cdot \frac{W}{L},\ U_T = \frac{k \cdot T}{q} \text{ and } n \text{ is the slope factor} \tag{3.40}$$

The transconductance of the MOS transistor is normalized to the maximum value, which can be reached in the weak inversion. The function (empirical) used for interpolation of the transconductance between strong and weak inversion for a given drain current I_D is described by the equation [3.4]:

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2} \cdot \sqrt{I_f} + 1}} \qquad \text{where} \quad I_f = \frac{I_D}{I_S} \tag{3.41}$$

Finally the transconductance of the CMOS transistor operated in weak and moderate inversion is given below:

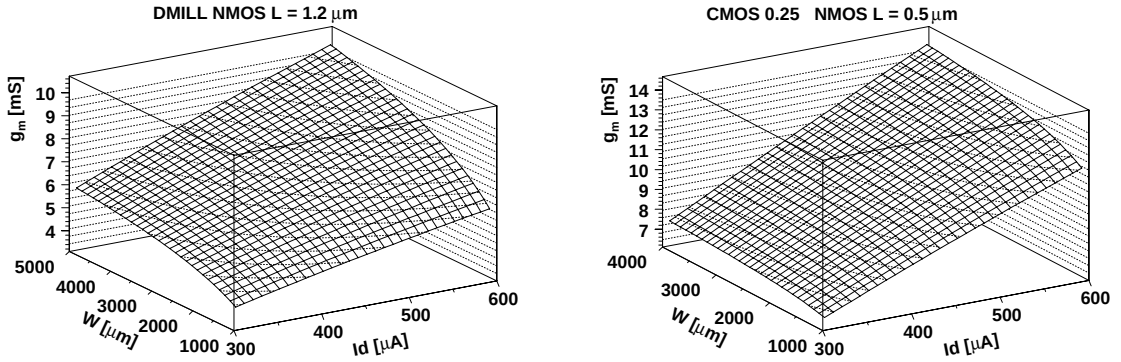
$$g_m = G(I_f) \cdot \frac{I_D}{n \cdot U_T} \tag{3.42}$$



(a) *(b)*

Figure 3.16: Transconductance of a DMILL (a) and CMOS 0.25μm NMOS transistor versus drain current.

The comparisons between transconductance simulated with the EKV model and measured for a DMILL NMOS transistor 2000/1.2μm and IBM 0.25μm NMOS 2000/0.5μm working in weak and moderate inversion regions are shown in Figures 3.16a and 3.16b respectively. Figure 3.17 shows the transconductance as a function of transistor width and drain current (a) for the 1.2μm channel length of a DMILL NMOS transistor, and (b) for the case of the 0.5μm channel length NMOS device in the IBM 0.25μm process.



(a) *(b)*

Figure 3.17: Transconductance of a DMILL (a) and IBM 0.25μm (b) NMOS transistor as a function of drain current and gate width.

3.4.2. Modelling of the gate capacitances

To calculate the ENC for FE amplifier built with relatively large MOS transistors one has to accurately model the gate capacitance of the input transistor for any region of inversion. For a MOS transistor working in saturation the intrinsic gate capacitance is the sum of the intrinsic capacitances gate-to-source and gate-to-bulk. Using the EKV capacitance model one can estimate [3.4]:

- Unitary Gate-to-Source capacitance per gate area:

$$C_{GSU} = C_{OXU} \cdot \left(\frac{1}{I_f \cdot G(I_f)} + \frac{3}{2} \right)^{-1} \qquad \text{where} \qquad C_{OXU} = \frac{\varepsilon_{OX}}{t_{OX}} \tag{3.43}$$

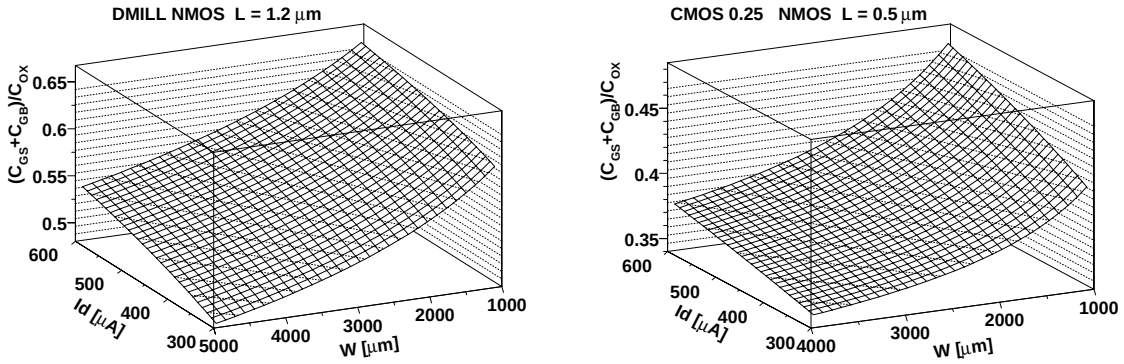
- Unitary Gate-to-Bulk capacitance per gate area:

$$C_{GBU} = C_{OXU} \cdot \frac{n-1}{n}\left(1 - \frac{I_f \cdot G(I_f)}{1+\frac{3}{2}\cdot I_f \cdot G(I_f)}\right) \tag{3.44}$$

Therefore the total capacitances Gate-to-Source C_{GS} and Gate-to-Bulk C_{GB} for a transistor of given dimensions will be respectively:

$$C_{GS} = C_{GSU} \cdot W \cdot L \qquad \text{and} \qquad C_{GB} = C_{GBU} \cdot W \cdot L \tag{3.45}$$

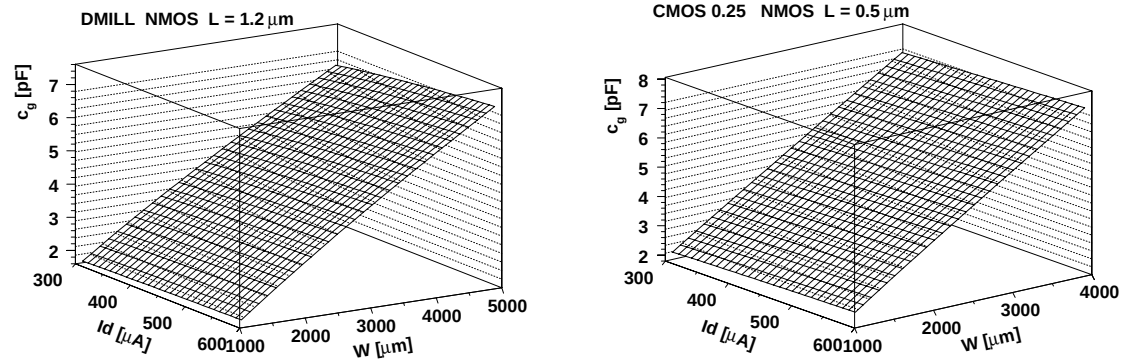
The normalized intrinsic capacitances per gate area for DMILL and CMOS 0.25μm NMOS transistors are shown in Figure 3.18.



(a) *(b)*

Figure3.18: The normalized intrinsic capacitances per gate area for DMILL (a) and IBM 0.25μm (b) NMOS transistor as a function of inversion order.

There are two overlap capacitances, gate-to-drain and gate-to-source, which one has to take into account while estimating the total gate capacitance. For IBM 0.25μm technology the gate-to-diffusion overlap capacitance is in the range of 0.4fF/μm and it is a large fraction of the total gate capacitance for NMOS transistor with gate length of 0.5μm. For DMILL NMOS device it is of about 0.1fF/μm.



(a) *(b)*

Figure 3.19: The total gate capacitance for DMILL (a) and IBM 0.25μm (b) NMOS transistor as a function of device dimension and bias current.

The total gate capacitance figures as a function of transistor dimensions and bias current for the NMOS transistors in DMILL and IBM 0.25μm technologies are shown in Figure 3.19.

3.5. Noise sources in MOS Transistors

Noise phenomena in induced channel MOS devices have been described in many papers [3.3], [3.7], [3.8].

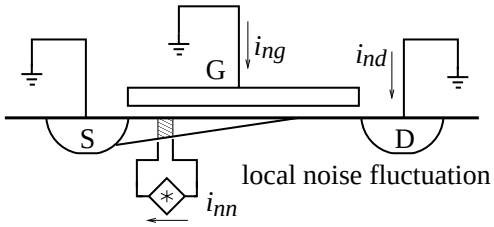


Figure3.20: A cross-section of the MOS device showing the propagation of a local noise fluctuation.

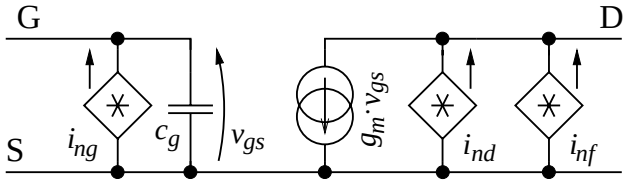


Figure 3.21: An equivalent schematic of the MOS transistor working in common source configuration including the noise sources.

For thermal noise simulation of Front-End amplifiers built with MOS devices we will use a model proposed by Van Der Ziel [3.3], but slightly modified for weak and moderate inversion regions [3.4]. We will consider the MOS transistor working in saturation. The classical theory describing the thermal noise in MOS devices considers the channel as a non-uniformly distributed transmission line, in which noise generation is due to the thermal motion of the charge carriers. Summing infinitesimal contributions of local noise fluctuation in the channel i_{nn} (see Figure 3.20) one can obtain a global variation of the drain current i_{nd}. The local fluctuations of the current in the transistor channel are coupled with the C_{GS} capacitance to the transistor gate, generating the AC noise current (Gate Induced Current noise) with the spectral density i_{ng}. The traditional model analyzes the transistor built as a discrete component working with bulk connected to the gate. In a MOS device realized in integrated circuit the bulk has to be separated from the transistor gate. Therefore one has to distinguish the gate (g_m) and the bulk (g_{mb}) transconductances, both contributing to the channel thermal noise. Consequently the spectra density of the thermal noise in the MOS transistor can be described by the following equation [3.4]:

$$\overline{i_{nd}^2} = 4 \cdot k \cdot T \cdot G_{Nth} \Delta f \qquad \text{where} \qquad G_{Nth} = \gamma \cdot (g_{mb} + g_m) = \gamma \cdot n \cdot g_m \tag{3.46}$$

The bias dependent parameter γ takes values from 1/2 to 2/3 for the ideal transistor operating from weak to strong inversion. The described model works well for long channel devices. The excess noise observed in short channel devices can be modeled using numerical methods based on a hydrodynamic formulation of the charge mobility [3.9]. A more practical approach introduces the excess noise factor Γ, which can be incorporated together with an interpolating function $F(i_f)$ determining the γ factor for a given inversion order (see [3.4] and [3.10]):

$$\gamma = F_n(I_f) \cdot \Gamma \qquad \text{where} \qquad F_n(I_f) = \frac{1}{1+I_f} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot I_f \right) \tag{3.47}$$

Defined in this way the excess noise factor Γ has to be parameterized for a given channel length of the MOS transistor implemented in a particular technology.
The spectral density of the high frequency Gate Induced Current (GIC) noise was originally derived for an ideal MOS transistor working in saturation and strong inversion

[3.3]. According to [3.9], the high frequency GIC excess noise rises together with the excess thermal noise in the same proportion. This could be expected since the origin of the GIC noise is the coupling of fluctuations of current thermal noise from the transistor channel. Consequently the gate induced current noise for a non-ideal device working in any order of inversion can be estimated according to [3.3] as follows:

$$\overline{i_{ng}^2} = 8 \cdot \gamma \cdot k \cdot T \cdot g_{gs} \Delta f \quad \text{where:} \quad g_{gs} = \frac{4}{45} \cdot \frac{\omega^2 \cdot C_{OX}^2}{n \cdot g_m} \quad \text{and} \quad C_{OX} = C_{OXU} \cdot W \cdot L \tag{3.48}$$

For complete evaluation of thermal noise in the MOS transistor one has to take into account the correlation between channel thermal noise i_{nd} and gate induced noise i_{ng}. The correlation term adjusted by the excess noise γ factor is described by the equation (3.49).

$$\overline{i_{ng} \cdot i_{nd}^*} = \frac{\gamma}{6} \cdot j \cdot \omega \cdot C_{OX} \cdot 4 \cdot k \cdot T \Delta f \tag{3.49}$$

Therefore the correlation factor c_{cor} can be denoted as:

$$c_{cor} = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\left(\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}\right)^{1/2}} = j \cdot \left(\frac{5}{32}\right)^{1/2} \approx j \cdot 0.395 \tag{3.50}$$

Another source of noise in the MOS device is the so-called flicker noise. This noise is also named 1/f noise, since its power spectra density is proportional to the inverse of the frequency. The theory of flicker noise relates it to surface phenomena, namely trapping and releasing of carriers at the silicon-oxide interface states. This hypothesis agrees well with the fact that 1/f noise is much lower in the buried channel devices. The usual model of flicker noise places the current noise generator with power spectra density given by equation (3.51) in-between the drain and source of the MOS transistor.

$$\overline{i_{nf}^2} = \frac{K_a}{f} \cdot \frac{g_m^2}{C_{OXU}^2 \cdot W \cdot L} \Delta f \tag{3.51}$$

The technology-dependent parameter K_a expresses the noise characteristic of a given process. It should be constant for devices of the same type within a given technology, however it may vary between different production batches. As already mentioned the parameter K_a has a tendency to degrade after ionizing radiation, therefore for the noise analysis one should take the worst case observed value of that parameter. The equivalent schematic of the MOS transistor including all mentioned noise sources is shown in Figure 3.21. The thermal noise in the channel and the flicker noise can be represented by the equivalent voltage noise sources connected to the gate with spectra densities described respectively by equations:

Equivalent input thermal noise: $\overline{v_{nd}^2} = \frac{\overline{i_{nd}^2}}{g_m^2}$ (3.52)

Equivalent input flicker noise: $\overline{v_{nf}^2} = \frac{\overline{i_{nf}^2}}{g_m^2}$ (3.53)

3.5.1. Evaluation of the noise parameters for DMILL and CMOS 0.25μm technologies

The excess noise factor Γ for MOS transistors designed in the IBM 0.25μm technology may be found in [3.6]. For the NMOS transistor working in moderate inversion with gate length around 0.5μm, the Γ factor has values in the range of 1.3 and does not improve with increased gate lengths.

The Γ factor for DMILL transistors may be extracted from data presented in [3.5]. In that report one finds the equivalent input noise spectra density v_{nd} measured at 3MHz for NMOS transistors of dimensions W/L=5000μm/3μm and W/L=2000μm/1.2μm working in moderate inversion (biased with 100μA) to be 2.6nV/√Hz and 2.85nV/√Hz respectively. For a 100μA bias current one finds the following values for I_f, $F_n(I_f)$ and g_m:

$I_f = 0.365$, $F_n(I_f) = 0.54$, $g_m = 2\text{mS}$

From these values we find the Γ factors for transistors with W/L dimensions of 5000/3 and 2000/1.2:

$$\Gamma = \frac{v_n^2 \cdot g_m}{4 \cdot k \cdot T \cdot n \cdot F_n(I_f)} = 1 \qquad \text{for NMOS 5000/3 and}$$

$$\Gamma = \frac{v_n^2 \cdot g_m}{4 \cdot k \cdot T \cdot n \cdot F_n(I_f)} = 1.2 \qquad \text{for NMOS 2000/1.2}$$

As expected, the excess noise increases for channel lengths below 3μm. The Γ factor reaches a value of 1.2 for the transistor with channel length equal to1.2μm. The choice of the gate length for the input transistor in the case of DMILL technology will be driven by a trade-off between the excess noise Γ factor and the overall gate capacitance, which degrades the equivalent noise charge of a charge sensitive amplifier. The increase of noise by 20% corresponding to the use of a shorter gate length will still be reasonable if one takes into account the increase of total gate capacitance for the transistors with longer channel length. For example the total gate capacitance of an NMOS transistor with W/L=5000μm/3μm is about 18pF, compared with 3.5pF gate capacitance for the shorter channel length transistor having the same W/L ratio, W/L=2000μm/1.2μm. For the noise analysis of the DMILL version of the MOS preamplifier we consider NMOS transistors with gate length equal to 1.2μm.

The flicker noise coefficient K_a for the IBM 0.25μm technology can be found in [3.6]. The worst-case value after 10Mrad irradiation is less than 6×10^{-27} [C^2/m^2]. The flicker noise coefficient for DMILL NMOS transistors can be extracted from the input voltage noise measured at 100Hz and presented in [3.5]. Assuming that the flicker noise is dominant at that frequency one can calculate the value of K_a to be around 1×10^{-26} [C^2/m^2]. The summary of the noise parameters for DMILL and IBM 0.25μm NMOS transistor is presented in table 3.3.

Table 3.3: Summary of the noise parameters used in calculation for DMILL and IBM 0.25μm technologies.

Symbol	Parameter description	Value	Technology
Γ	Excess noise factor	1.2	DMILL NMOS L=1.2μm
		1.3	IBM-0.25/NMOS L≥0.5μm
		1.25	IBM-0.25/PMOS L≥0.4μm
K_a	Flicker noise coefficient	1×10^{-26} [C^2/m^2]	DMILL/NMOS
		6×10^{-27} [C^2/m^2]	IBM-0.25/NMOS
		1×10^{-27} [C^2/m^2]	IBM-0.25/PMOS

3.6. Calculation of the output noise for the MOS transimpedance preamplifier

Having all noise sources and correlation terms defined, one can calculate the output noise of the preamplifier stage built with a MOS device using the same method as for the bipolar circuit.

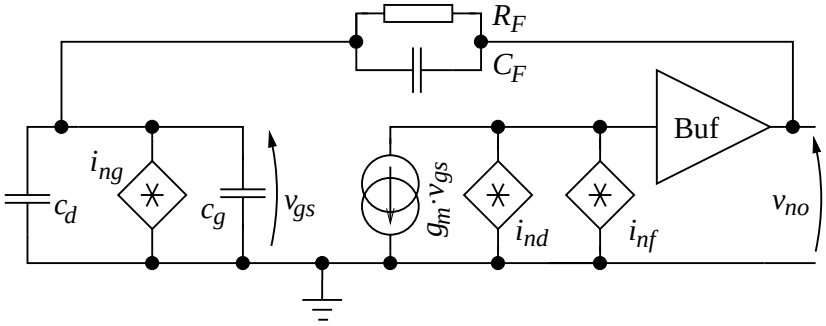


Figure 3.22: Equivalent schematic of the transresistance preamplifier with MOS input transistor including the noise sources.

Figure 3.22 shows the equivalent schematic of the preamplifier stage built with the MOS transistor and including the noise sources. For the analysis we assume the same feedback configuration as for the BJT preamplifier and we will consider the noise sources related only to the input transistor. The detailed analysis of the propagation of all noise sources to the preamplifier output has been performed in the Appendix. The admittances of the feedback loop, detector and transistor input are described as follows:

$$Z_F = \frac{1}{Y_F} = \frac{R_F}{1 + j\cdot\omega\cdot\tau_f},\ Y_d = j\cdot\omega\cdot c_d\ ,\ Y_g = j\cdot\omega\cdot c_g,\ \tau_f = R_F\cdot C_F \tag{3.54}$$

Capacitance c_g represents both intrinsic capacitances C_{GS} and C_{GB} as well as parasitic gate overlap capacitances. Describing all noise quantities at the output of the preamplifier in the time domain we obtain the following expressions for the output noise related to the relevant noise source:
The contribution from the channel thermal noise v_{no_ind}

$$v_{no\_ind}(t) = \frac{i_{nd}(t)}{g_m}\cdot Z_F\cdot\left(Y_F + Y_g + Y_d\right) \tag{3.55}$$

The contribution from the gate induced current noise v_{no_GIC}

$$v_{no\_GIC}(t) = i_{ng}(t)\cdot Z_F \tag{3.56}$$

The contribution from the flicker noise v_{no_f}

$$v_{no\_f}(t)=\frac{i_{nf}(t)}{g_m}\cdot Z_F\cdot\left(Y_F+Y_g+Y_d\right) \tag{3.57}$$

The final noise fluctuation at the output of the preamplifier can be calculated as following:

$$v_{no}(t)=v_{no\_ind}(t)+v_{no\_GIC}(t)+v_{no\_f}(t) \tag{3.58}$$

As in the case of the analysis of the bipolar circuit the noise spectra density of the output noise will be calculated using the Wiener-Khintchine theorem. The approach presented allows for accurate calculation of the correlation between channel thermal noise and GIC noise. The analysis presented in Appendix 7.4 yields the following expressions for the spectra density of the output noise.

$$\frac{\overline{v_{no}^2}}{\Delta f}=\frac{\overline{v_{no\_id}^2}}{\Delta f}+\frac{\overline{v_{no\_GIC}^2}}{\Delta f}+\frac{\overline{v_{no\_f}^2}}{\Delta f}+\frac{\overline{v_{no\_corr}^2}}{\Delta f} \tag{3.59}$$

The noise spectra densities related to the previously discussed noise sources are as follows:

$$\frac{\overline{v_{no\_id}^2}}{\Delta f}=\frac{4\cdot k\cdot T\cdot\gamma\cdot n}{g_m}\cdot\left(\omega^2\cdot\left(c_d+c_g+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.60}$$

$$\frac{\overline{v_{no\_GIC}^2}}{\Delta f}=\frac{32}{45}\cdot k\cdot T\cdot\gamma\cdot\frac{\omega^2\cdot C_{OX}^2}{n\cdot g_m}\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.61}$$

$$\frac{\overline{v_{no\_f}^2}}{\Delta f}=\frac{K_a}{f\cdot C_{OXU}^2\cdot W\cdot L}\cdot\left(\omega^2\cdot\left(c_d+c_g+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.62}$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f}=\frac{8}{6}\cdot\frac{\gamma\cdot k\cdot T}{g_m}\cdot\omega^2\cdot C_{OX}\cdot\left(c_d+c_g+C_F\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.63}$$

Considering the real parts of the input-feedback admittances in the expressions (3.20) and (3.21) for the output noise in case of bipolar preamplifier can be justified. For low detector capacitance and certain regions of biases the r_e (β/g_m) of the input transistor makes a significant contribution to the final value of ENC. In the case of the $r_{bb'}$ contribution for low detector capacitances, the real and imaginary part of feedback admittance Z_F have comparable contributions to the output noise as well. In the case of the CMOS version of the preamplifier the feedback conductance Y_F ($1/R_F$) can be completely ignored in comparison with detector and gate admittance, the latter being at list an order of magnitude higher than the admittance of the feedback capacitor C_F (see Figure 3.19). Therefore one can simplify the equations (3.60) and (3.62) to the following ones:

$$\frac{\overline{v_{no\_id}^2}}{\Delta f}=\frac{4\cdot k\cdot T\cdot\gamma\cdot n}{g_m}\cdot\omega^2\cdot\left(c_d+c_g+C_F\right)^2\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.64}$$

$$\frac{\overline{v_{no\_f}^2}}{\Delta f}=\frac{K_a}{f\cdot C_{OXU}^2\cdot W\cdot L}\cdot\omega^2\cdot\left(c_d+c_g+C_F\right)^2\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{3.65}$$

3.7. Calculation of the ENC for amplifiers built with MOS transistors working in transresistance configuration with triple integrator CR-(RC)^3

Assuming the shaper stage is a triple integrator with the time constant matching the time constant of the preamplifier feedback ($\tau_i = \tau_f = t_{peak}/3$) one can find the expression for the rms noise at the shaper output using the same methodology as for the bipolar circuit:

$$\sigma_{nfo}=\left(\int_0^\infty\frac{\overline{v_{no}^2}}{\Delta f}\cdot\frac{1}{\left(1+\tau_f^2\cdot\omega^2\right)^3}\,\partial f\right)^{\frac{1}{2}} \tag{3.66}$$

where $\frac{\overline{v_{no}^2}}{\Delta f}$ is described by equation (3.59). The equivalent noise charge in electron charges will be equal to:

$$ENC\,[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\sigma_{nfo}=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty\frac{\overline{v_{no}^2}}{\Delta f}\cdot\frac{1}{\left(1+\tau_f^2\cdot\omega^2\right)^3}\,\partial f\right)^{\frac{1}{2}} \tag{3.67}$$

Each term of expression $\overline{v_{no}^2}$ corresponding to different noise sources can be integrated separately to find the partial contributions to the equivalent noise charge.

3.7.1. ENC contribution from the channel thermal noise

The ENC contribution from the channel thermal noise can be obtained by solving the following definite integral:

$$ENC_{Id}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty\frac{4\cdot k\cdot T\cdot\gamma\cdot n}{g_m}\cdot\omega^2\cdot\left(c_d+c_g+C_F\right)^2\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.68}$$

which gives the following expression for ENC in electrons:

$$ENC_{Id}[e-]=\frac{e^3}{12\cdot\sqrt{3}}\cdot\sqrt{\frac{4\cdot k\cdot T\cdot n\cdot\gamma}{g_m}}\cdot\frac{c_d+c_g+C_F}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.69}$$

For a given value of peaking time the ENC due to the channel thermal noise is proportional to the total input capacitance and it decreases with the square root of the transconductance g_m of the input transistor.

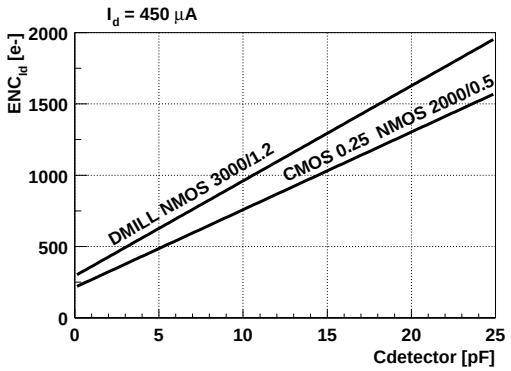


Figure 3.23: ENC contribution from thermal noise versus input capacitance for DMILL and CMOS 0.25μm NMOS transistors.

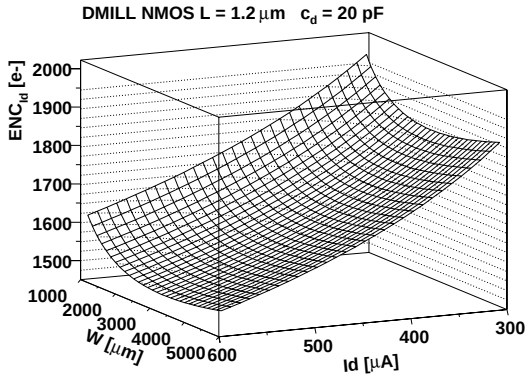


Figure 3.24: ENC contribution from thermal noise as a function of transistor width and bias for 20pF detector capacitance for DMILL NMOS.

Figure 3.23 shows the simulated ENC slopes plots originating from thermal channel noise for two examples of NMOS transistors from the DMILL and CMOS 0.25μm technologies. As we might expect from the simulation of the transconductance of those devices, comparing transistors working under the same bias condition we find that the noise performance in modern technologies is much better due to the higher g_m. Figure 3.24 shows the simulated ENC for DMILL NMOS transistors, with 20pF detector capacitance, as a function of the device width and bias. It can be seen that for a given input capacitance c_d there is an optimum width of the transistor that minimizes the ENC level. This is the result of the trade-off between achievable transconductance at a given transistor drain current and the total gate capacitance depending on the device dimensions.

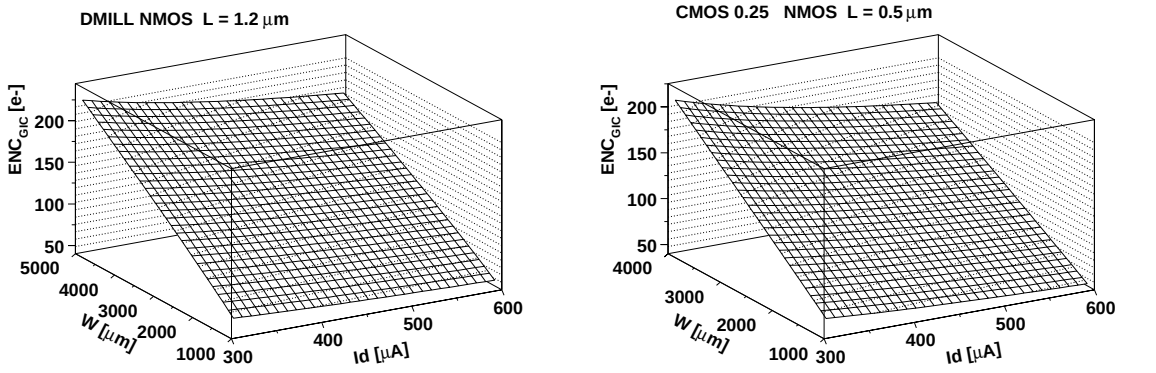
3.7.2. ENC contribution from the gate induced current noise

The contribution from the GIC noise can be found by solving the following definite integral:

$$ENC_{GIC}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{32\cdot k\cdot T\cdot\gamma}{45\cdot n\cdot g_m}\cdot\omega^2\cdot C_{OX}^2\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.70}$$

which yields:

$$ENC_{GIC}[e-]=\frac{e^3\cdot\sqrt{2}}{9\cdot\sqrt{15}}\cdot\sqrt{\frac{k\cdot T\cdot\gamma}{n\cdot g_m}}\cdot\frac{C_{OX}}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.71}$$



(a) *(b)*

Figure 3.25: ENC contribution from the gate induced current noise for DMILL (a) and CMOS 0.25μm (b) NMOS transistor versus device dimensions and bias current.

Figures 3.25a and 3.25b show the contribution to the ENC from the gate induced current noise for DMILL and IBM NMOS transistors respectively. It can be seen (equation (3.71)) that the value of the ENC_{GIC} depends on the transconductance of the transistor and gate-to-channel capacitance C_{OX} and does not depend on the detector capacitance. Although the unitary gate-to-channel capacitances for DMILL and IBM transistors are very different, for the dimensions of the devices considered the total gate capacitance is comparable (see Figure 3.19). This explains the similar levels of ENC in these cases.

3.7.3. ENC contribution from the correlation term

The contribution of the correlation between channel thermal noise and GIC noise can be calculated by solving the definite integral in:

$$ENC_{corr}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{8\cdot k\cdot T\cdot\gamma}{6\cdot g_m}\cdot\omega^2\cdot C_{OX}\cdot\left(c_d+c_g+C_F\right)\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.72}$$

which finally gives:

$$ENC_{corr}[e-]=\frac{e^3}{18}\cdot\sqrt{\frac{k\cdot T\cdot\gamma}{g_m}}\cdot\frac{\sqrt{C_{OX}\cdot(c_d+c_g+C_F)}}{\sqrt{t_{peak}}}\cdot\frac{1}{q} \tag{3.73}$$

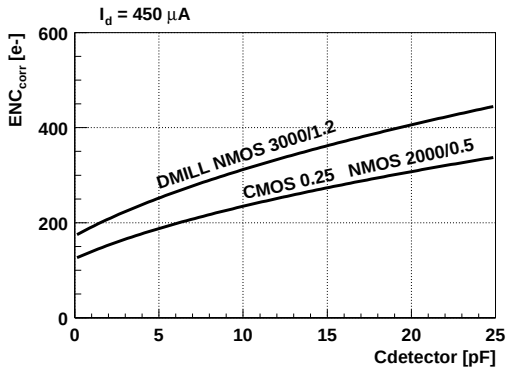


Figure 3.26: The ENC contribution from the correlation term versus detector capacitance for DMILL and IBM 0.25μm NMOS transistors.

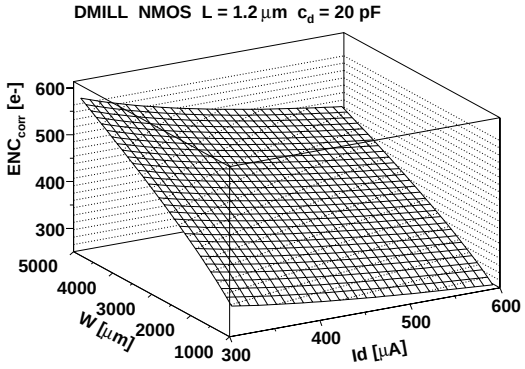


Figure 3.27: The ENC contribution from the correlation term as a function of transistor width and bias current; simulated for 20pF detector capacitance and a DMILL NMOS transistor.

Figure 3.26 shows the correlation ENC as a function of input capacitance for DMILL and IBM 0.25μm NMOS transistors. Note (equation (3.73)) that the ENC value originating from the correlation term depends on the square root of the product of the detector capacitance and gate capacitance C_{OX}. Because of its dependence on the detector capacitance, the correlation term makes a non-negligible contribution to the final value of the ENC, especially for larger transistors having higher gate capacitance (see Figure 3.27).

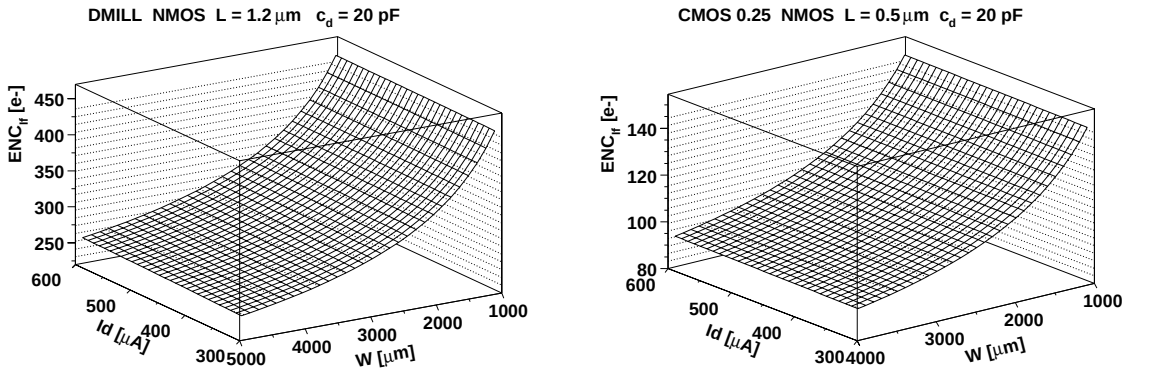
3.7.4. ENC contribution from flicker noise

The ENC contribution from flicker noise can be obtained by solving the following integral:

$$ENC_{If}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^{\infty}\frac{K_a}{f\cdot C_{OXU}^2\cdot W\cdot L}\cdot\omega^2\cdot\left(c_d+c_g+C_F\right)^2\cdot\frac{R_F^2}{\left(1+\tau_f^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{3.74}$$

which gives:

$$ENC_{If}[e-]=\frac{\sqrt{2}\cdot e^3}{9\cdot\sqrt{3}}\cdot\sqrt{\frac{K_a}{W\cdot L}}\cdot\frac{c_d+c_g+C_F}{C_{OXU}}\cdot\frac{1}{q} \tag{3.75}$$



(a) *(b)*

Figure 3.28: The contributions from flicker noise to the ENC for DMILL (a) and IBM 0.25μm (b) NMOS transistors simulated for 20pF detector capacitance.

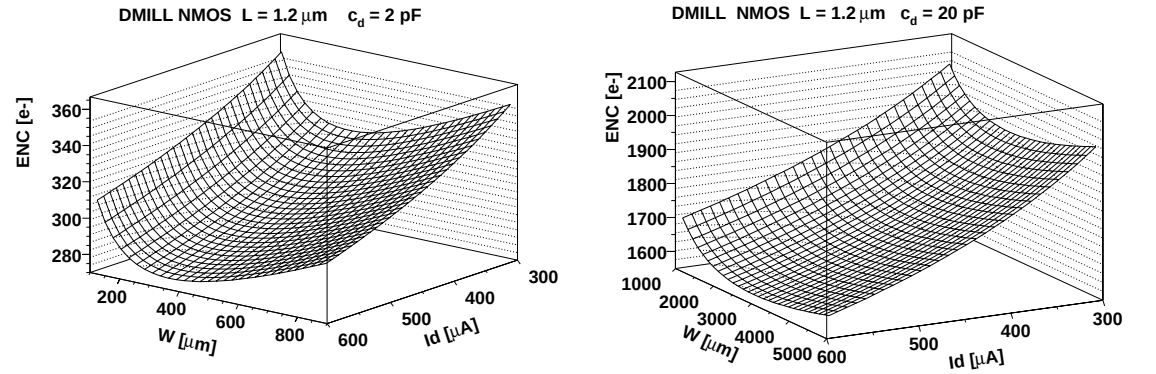
Figure 3.28a and 3.28b show the contribution of the 1/f noise to the ENC for DMILL and IBM 0.25μm NMOS transistors simulated for a 20pF detector capacitance. It can be seen (see expression (3.75)) that the ENC component due to flicker noise does not depend on the time constant of the CR-RC shaper[3]. For a detector capacitance c_d higher than the gate capacitance c_g, improved noise performance is obtained by use of a larger transistor (see Figure 3.28a and 3.28b). The visible difference between the noise performances of the transistors shown in the example is due mainly to the different values of the C_{OXU} parameter for DMILL and IBM technologies (see equation (3.75)).

3.7.5. Final ENC figure for the MOS preamplifier

The final ENC figure taking into account all previously considered noise sources can be obtained by quadratic summing of the partial contributions:

$$ENC = ENC_{Id} \oplus ENC_{GIC} \oplus ENC_{corr} \oplus ENC_{If}$$

The final plots showing the ENC versus bias condition and transistor width for two different values of the detector capacitances are presented in Figure 3.29.



(a) *(b)*

Figure 3.29: The Equivalent Noise Charge for the MOS DMILL transresistance amplifier with 20ns peaking time versus different bias condition and transistor width for low (a) and high (b) detector capacitances.

[3] However it does depend on the order n of the CR-$(RC)^n$ filter.

The calculation has been performed assuming 20ns peaking time of the FE amplifier. One notices an optimum width of the DMILL NMOS transistor loaded with 20pF input capacitance of around 3000µm (Figure 3.29b). For low input capacitance the capacitance of the transistor gate dominates and consequently the optimum is obtained for a smaller transistor width in the range of 300 to 400µm (Figure 3.29a).

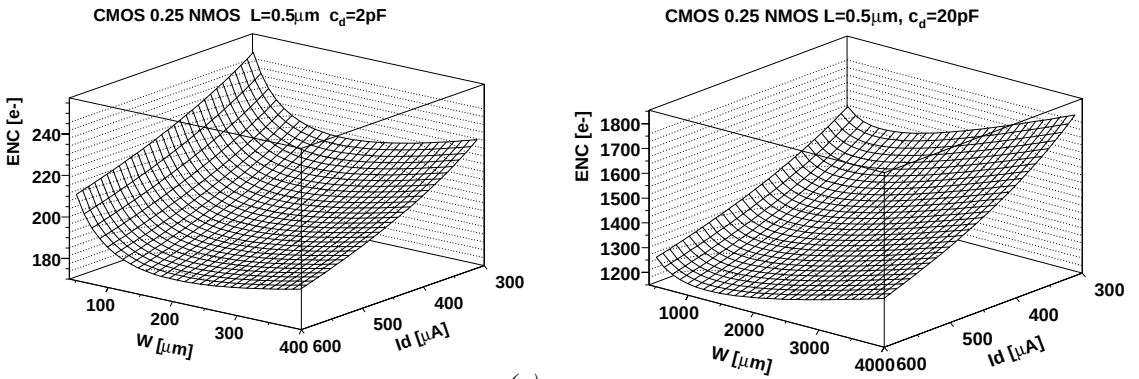


Figure 3.30: The Equivalent Noise Charge as a function of bias condition and transistor width for a MOS transresistance amplifier having 20ns peaking time and implemented in modern CMOS 0.25µm technology. The two cases shown are for low (a) and high (b) detector capacitance.

One observes a significant improvement of the noise performance for devices implemented in the modern IBM 0.25µm technology. Although they have, for the dimensions in the examples, a comparable gate capacitance, the submicron devices offer for the same bias current roughly 30% better noise performance (Figure 3.30a and 3.30b) due to the much higher transconductance.

3.8. Summary

By comparing amplifiers built with DMILL BJT and MOS input transistors working with high, 20pF detector capacitances (see Figure 3.15 and 3.29) one observes an advantage of the bipolar device in terms of noise performance and dissipated power. Even taking into account smaller geometry BJTs, which have a base spread resistance of the order of 180Ω, one can see that for 20pF input capacitance and the bias current around 250µA the expected noise is in the range of 1600e^-, which is comparable with the noise predicted for an NMOS device with W/L=3000µm/1.2µm working with a 600µA bias current. In addition, one should consider the superior frequency characteristic of the BJT devices, which have an f_t in the range of 5GHz. As will be shown later, the preamplifiers developed in DMILL technology with a bipolar transistor as an input device have a gain bandwidth product in the range of 1GHz. This provides the required speed and low input impedance of the front-end amplifier (which is not achievable for the structure using the previously mentioned NMOS transistor (W/L=3000µm/1.2µm)).

Taking into account all the arguments presented, the bipolar transistor was an obvious choice for further development of the fast front-end amplifiers optimized for long strip silicon detectors in DMILL technology. Bearing in mind the very high radiation doses in the LHC experiments, a reasonable compromise between noise performance and the radiation hardness of the device has been made by selecting transistor with emitter dimensions of 10µm×1.2µm. It should be stressed that, for applications that do not require extreme radiation hardness, e.g. where the dose levels are order of magnitude lower, a solution would be to increase the emitter size of the transistor, which

consequently would lower the base spread resistance and would improve the noise performance of the front end amplifier.

Looking at the results of the noise analysis made for the IBM 0.25μm technology (Figure 3.30), one should not forget that this technology only became available to us in the year 2000, i.e. five years after the start of the development of the early prototypes of the SCTA and ABCD chips. In the next chapter the results from the first prototype of the front end amplifier and comparator in the IBM 0.25μm process will be presented together with the results of the bipolar front-ends implemented in the final versions of the SCTA and ABCD DMILL chips.

4. Implementations of fast transimpedance Front End amplifiers in Bipolar and CMOS technologies

This chapter presents the designs of three examples of fast front-end amplifiers for readout of silicon strip detectors under LHC conditions. Two designs implemented in radiation hard BiCMOS DMILL technology have been employed in the SCTA128VG and ABCD3T readout chips, which are 128-channel ASICs representing analogue and binary readout architectures for silicon strip detectors at LHC experiments. In addition to the evaluation of the basic parameters of the chips results are presented showing that the performance of the fully equipped detector modules is compatible with ATLAS specifications.
The ABCDS-FE chip, which is the most recent CMOS implementation of the fast transimpedance amplifier and comparator in the IBM-0.25 process, demonstrates the potential of the technology to build fast front-ends optimized for long strip silicon detectors. The results presented are from the first, 64-channel prototype of this chip.

4.1. Requirements for the analogue performance of the front-end amplifier

The specifications for the analogue performance of the front-end amplifiers for tracking applications can be summarized by saying that the readout chip must provide the complete functionality for processing the signals received from the silicon sensors in terms of integration, amplification and noise filtering, while satisfying the requirements on speed and signal-to-noise ratio, within a limited power budget. For the application at the LHC experiments one has to add the additional requirement for the radiation hardness of the design.

As shown in Chapter 1, an important parameter of the detector influencing the noise performance and possible cross talk between electronic channels is the capacitance and its geometrical distribution within the sensor. The designs presented in this thesis were optimized for the readout of silicon strip detectors designed for the ATLAS SCT. The silicon sensors are p^+-on-n with a strip-to-backplane capacitance of around 0.3pF/cm and an interstrip capacitance of 1.03pF/cm, increasing to 1.4pF/cm after the full radiation dose[1] expected during the lifetime of the ATLAS experiment. The total length of the two daisy-chained detectors is equal to 13cm, which results in a total capacitive load at the input of one electronic channel in the range of 18pF before and 22pF after the full radiation dose. For those capacitances the front-end amplifier should provide an ENC below 1500e^- before and 1800e^- after the irradiation. The level of noise after irradiation includes the contribution from the detector leakage current shot noise, which is specified as 2μA maximum per detector strip.

The value of the peaking time, specified to be around 20ns, allows correct data association to the originating Bunch Cross Over (BCO) number and permits a double pulse resolution of the order of 50ns, when the shaper has a semigaussian response. An additional specification concerning the speed of the comparator has been applied in the case of the bipolar architecture. The time walk of the comparator connected to the front-end amplifier should be less than 16ns for the nominal setting of the threshold voltage at 1fC and signal charges from the detector ranging between 1.25 and 10fC. Thus, all timing

[1] Full radiation dose after 10 years of the experiment has been estimated as 10Mrad of ionizing radiation and 2×10^{14} n/cm^2 1MeV equivalent.

effects, namely the peaking time of the amplifier and the response delay of the comparator have been combined into one number**.**
By limiting the dynamic range of the front-end amplifier to 10fC the channel gain could be set at around 50mV/fC. This relaxes the requirements for the performance of the analogue memory and the matching of the comparator offsets, measured relatively to the gain of the front-end amplifier. The required linearity is in the range of 5%, which is a rather typical value for the electronics for tracking applications. More attention has been paid to providing a good matching of the analogue parameters within a chip. For analogue architecture this concerns mostly the matching of gain, which has an impact on the spatial resolution in case of finding the centre of gravity of the cluster signals. In case of binary electronics working with a single threshold voltage for all the channels, in addition to the matching of gain, one has to minimize the spread of the comparator offsets, which together with the noise may degrade the efficiency versus noise occupancy figure. In order to provide the required performance of the ATLAS SCT detector, the spread of the comparator offsets must be kept below 5% of the 1fC response. For a designed amplifier gain in the range of 50mV/fC the sigma spread of the comparator offsets should be below 2.5mV rms.

The power consumption was already mentioned as an important issue in the tracking applications. In the case of the ATLAS silicon tracker, over 6 million electronic channels are packed in a small volume, and this sets an upper limit of 2.5mW for power dissipated by a single electronic channel.

In addition to the requirements concerning the noise, speed, linearity and power consumption, another basic constraint for large detector readout systems is the stability. The stability problem of the transimpedance preamplifier working with a capacitive load was already mentioned in Chapter 1, where we discussed the response in the time domain. A more general approach to the analysis of the stability, taking into account also non-dominant poles of the amplifier, is presented by the Nyquist theorem [4.1 p597]. The parameter defining the stability of the feedback amplifier is the phase margin. The standard practice usually requires a phase margin of the order of 60°, which provides optimum bandwidth in the closed loop configuration for the preamplifier[2].
Non optimum working conditions, such as resistive power and ground lines, a high number of channels placed in the same chip and sharing the same bonding connections multiplied by a high number of chips serving the same detector module may significantly degrade the phase margin obtained for a single channel. This may lead to the unstable operation of a large, multi-channel system. Consequently, in case of readout electronics designed for tracker applications a larger phase margin, usually in the order of 70 to 80° is required.

4.2. Divergences from the ideal CR-(RC)^3 characteristic of the shaper

Although all the front-end amplifiers we discussed can be approximated by the CR-(RC)^3 filter, the real transfer function of the processing chain will diverge from that idealized characteristic. The first limitation will be introduced by the preamplifier frequency characteristic, namely the bandwidth, and the required value of the phase margin. The required value of the compensating capacitor in the preamplifier feedback, which also defines together with the feedback resistance the differentiating time constant of the filter,

[2] The importance of maximizing the preamplifier bandwidth was discussed in Chapter 1 in the light of minimizing of the cross-talks signals.

does not necessarily match with the desired value of the peaking time of the shaper. One has to keep in mind that the value of the feedback capacitance defines also the charge gain of the preamplifier, which should be kept as high as possible in order to limit the noise contribution from the following stages.

The limited bandwidth of the preamplifier will introduce at least one integrating time constant**,** which for the required speed of the electronics has to be taken into account. Therefore, the time constants of the following shaper stages have to be matched in order to obtain the final required value of the response peaking time, the basic parameter defining the timing performance of the system and cutoff frequency of the noise filter. The correction factors to the noise formulas describing the behavior of the ideal CR-$(RC)^3$ filter will be derived for the considered front-end amplifiers taking into account different time constants of the following blocks of the processing chain, also including time constants of the AC coupling used in between the stages. As will be shown later, the correction factors are in the range of a few percent only, which justifies the use of the CR-$(RC)^3$ approximation for the noise analysis presented in Chapter 3.

4.3. Bipolar Transimpedance Front-End amplifier employed in the SCTA128VG chip

The schematic diagram of one channel of the SCTA128VG front-end amplifier is shown in Figure 4.1. A single channel consists of three main blocks: the transimpedance preamplifier, a shaper providing amplification and integration of the signal, and the output stage driving the signal into the analogue memory.

4.3.1. Architecture of a single channel of the front-end amplifier

The input stage formed by the transistor T1 and loaded with a PMOS current source is followed by a common collector buffer and the feedback loop is built with resistor R_F and capacitor C_F. In the DMILL technology we have at our disposal all three types of transistors, JFET, MOSFET and BJT, which can be used as input devices.

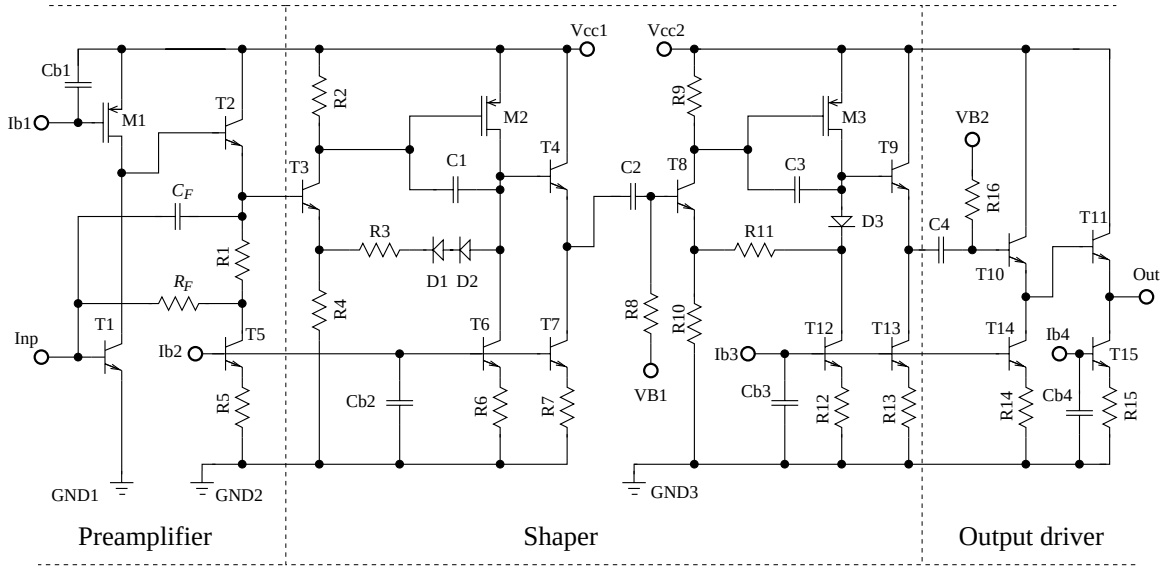


Figure 4.1: Schematic diagram of one channel of the SCTA128VG chip.

The choice of the type and geometry of the input device was driven not only by the noise performance discussed in Chapter 3, but also by the superior frequency characteristic of

the bipolar transistors offered by DMILL technology. The GBP (gain-bandwidth product) of 1GHz, which is obtained easily with a bipolar input transistor, will not be available with an NMOS transistor having optimal dimensions for the noise performance. The open loop gain of the input stage is around 65dB depending slightly on the bias of the input transistor (see Figure 4.2).

The size of the input transistor was finally set to 1.2μm×10μm which is a reasonable compromise between the value of the base spread resistance[3], which limits the noise performance, and the current density in the emitter, which influences the radiation hardness of the device. The relatively high output resistance of the BJT allowed the input stage to use a single common emitter amplifier loaded with a current source built with a single PMOS device.

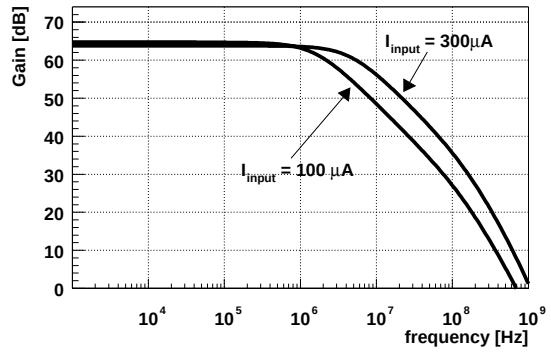


Figure 4.2: Simulation of open loop characteristic of the bipolar preamplifier from Figure 4.1 for two values of input transistor bias.

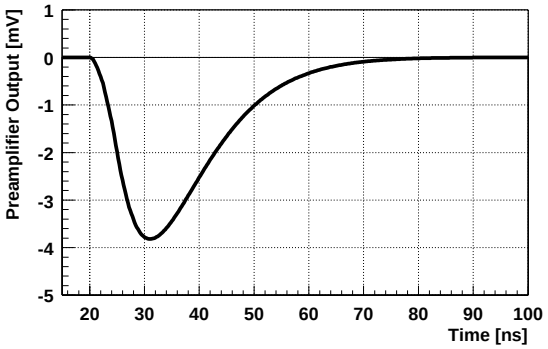


Figure 4.3: Transient simulation of the preamplifier response to 1fC signal charge for nominal bias (200μA) and 20pF input load capacitance.

The bias current of the input transistor has to be optimized for a given input capacitance taking into account the value of current gain, which depends on the actual process parameters and the degradation due to radiation damage. A reasonable noise performance of the preamplifier for values the beta parameter ranging from 350 to 40 and for an input capacitance of 20pF could be obtained by setting the bias current in the range 120 and 300μA.

The pulse gain at the preamplifier output, determined mostly by the feedback capacitor C_F and the preamplifier bandwidth, is in the range of 4mV/fC. The response of the preamplifier to a 1fC input charge when it is loaded with 20pF input capacitance and biased with nominal settings is shown in Figure 4.3. The time constant of the pulse decay defined by the R-C constant of the feedback elements C_F and R_F is comparable with the peaking time of the response pulse, which is equal to 10ns. Therefore, for the nominal load and bias condition, one can approximate the transfer function of the preamplifier stage by a CR-$(RC)^1$ filter with 10ns time constant. In order to achieve the desired gain of the order of 50mV/fC, an additional amplification stages are necessary.

The feedback capacitor C_F of value 120fF provides for nominal 20pF capacitive input load and a wide range of biases with the phase margin above 70° (see Figure 4.4). For the nominal bias of the input transistor around 200μA, the phase margin is above 80°, which

[3] The measurement of the base spread resistance for the DMILL 1.2×10μm BJT can be found in the Appendix. The value of the $r_{bb'}$ for the mentioned transistor has been estimated to be around 180Ω.

provides an extra safety margin for the stability of the chip working in a non-ideal environment.

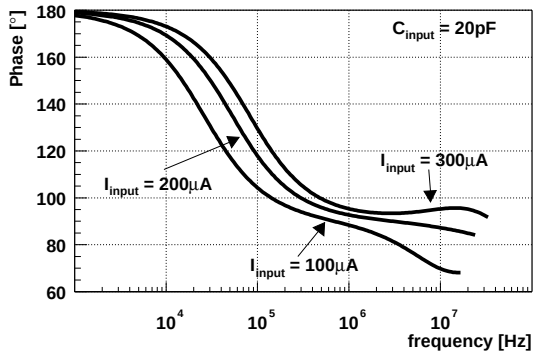


Figure 4.4: Simulation of the phase of the signal at the feedback loop output for loop gain higher than 0dB. End points of the figures define phase margins. Simulation done for 20pF nominal input load capacitance, nominal process parameters and full range of input transistor bias.

The importance of lowering the amplifier input impedance was discussed in Chapter 1, in the light of minimization of the cross talk between electronic channels connected to strip detectors. Figure 4.5 shows the results of the AC simulation of the amplifier input impedance. For the low frequency region, the DC open loop gain and the feedback resistor R_F of value 80kΩ result in the input impedance of the amplifier being in the range of 50Ω. Towards higher frequencies the input impedance increases proportionally to the reduction of gain because of bandwidth limitation, and it finally saturates for the region where the imaginary part of the input impedance related to the feedback capacitance is dominant. For the central frequency of the shaper around 8MHZ, the input impedance for the nominal bias condition is between 120 and 150Ω.

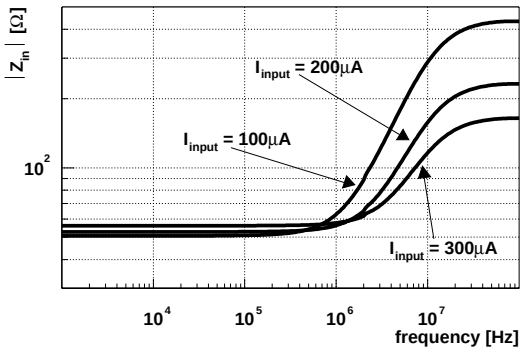


Figure 4.5: AC simulation of the amplifier input impedance frequency characteristic for various bias currents of the input transistor.

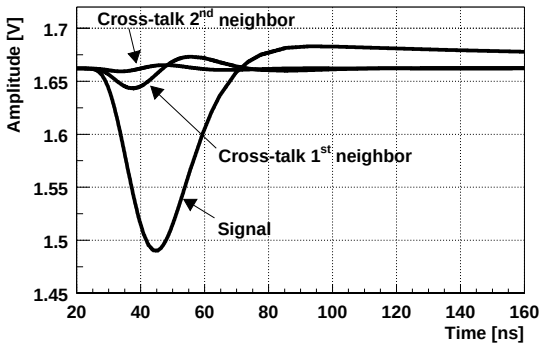


Figure 4.6: Transient simulation of the preamplifier and shaper responding to 3.5fC signal charge and loaded with silicon strip detector. The nominal value of bias (200μA) and nominal value of interstrip capacitance (c_{is}= 7pF) has been used. Effective capacitance loading the input of the amplifier is in the range of 18pF.

The nominal value of the interstrip capacitance for the ATLAS type silicon sensor is around 1.03 pF/cm, which gives for two 13cm, neighboring strips a coupling capacitance

c_{is} in the range of 7pF. Figure 4.6 shows the results of a transient simulation of the preamplifier and shaper when loaded with the detector, assuming nominal values of interstrip capacitances and biased with nominal currents. The maximum amplitude of the cross talk is in the range of 8%. For the further processing of the signals in the SCTA chips, when the peak values of the output pulses are sampled into the analogue memory, the cross talk signals can be mostly neglected, since at that moment they are crossing the baseline level (see Figure 4.6). On the other hand, the cross talk signals will have higher importance when the front-end amplifier is connected to the amplitude discriminator employed in the binary readout architecture, which will be discussed later in the case of the ABCD chip.

A DC coupled amplifier (Figure 4.1) built with transistors *T3* and *M2* is the first stage of the shaper providing amplification and integration of the signal. Negative feedback determined by the resistive network built with resistors *R3* and *R4* ensures good stabilization of the closed loop gain with respect to the technological parameters, temperature and power supply, and also ensures high bandwidth for relatively small power consumption (250µW for nominal bias). Capacitor *C1* optimizes the bandwidth of the stage responsible for effective integration of the signals with a time constant around 4.7ns. The closed loop DC-gain of the stage has been limited to 4[V/V] in order to deal with drift of the DC potential at the base of *T3* due to changes of the *T1* base current[4], which can result in up to 400mV voltage drop on the feedback resistor R_F for the nominal bias conditions. These drifts can be slightly compensated by a voltage drop on the resistor *R1* adjusted by the *T5* current source, which stabilizes the DC potential at the amplifier input.

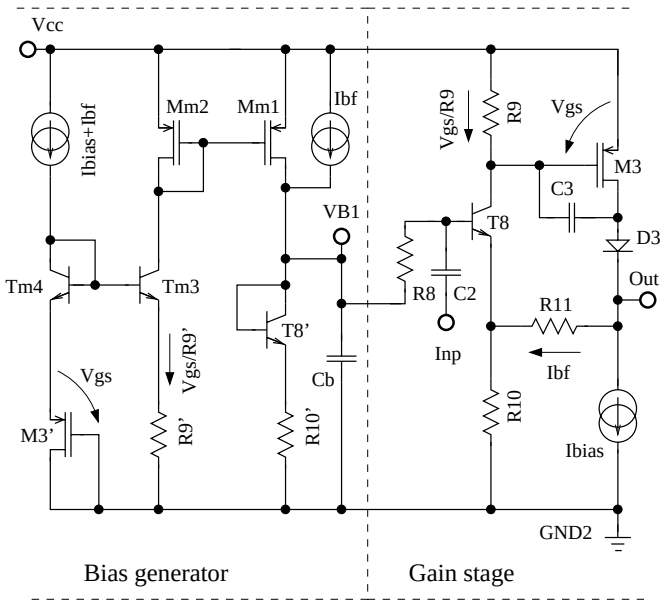


Figure 4.7: Simplified schematic diagram of the voltage generator biasing the second stage of the shaper.

The same structure is repeated in the next shaper stage, which is AC coupled to the previous one in order to prevent propagation of DC offsets implied by the drifts of the DC potential at the shaper input. In order to fully control the DC operating point of the second amplifier a special voltage generator has been employed (see Figure 4.7). It generates the

[4] The change of the base current is a function of collector current of the input transistor adjusted for optimum noise performance (150 - 300µA) and variation of the beta factor (40 – 350).

DC bias voltage *VB1* using the desired value of the currents in the feedback (current *Ibf* flowing in *R11*) and in the second stage of the amplifier (*Ibias*). Since the devices used in the bias generator are replicas of the devices in the amplifier stage, the bias generator will track possible technology process variation and drifts of the parameters after radiation damage. Overall pulse gain of the front-end stage including the preamplifier and two-stage shaper is in the range of 55mV/fC. Two stages of the shaper integrate the signal with time constants around 4.7ns, which together with the preamplifier integrating and differentiating the signal with a 10ns time-constant, effectively results in a semi-gaussian pulse with a peaking time of 20ns. The small undershoot, of the order of 12%, is caused by two AC couplings used in the shaper stage (see Figure 4.6).

In order to provide a well defined DC level at the output of the front end channel before the analogue memory an extra AC coupling is used in the front of the output buffer built with the transistors *T10* and *T11*. Note the separation between grounds and supplies lines, especially the extra connection for the emitter of the input transistor – the most sensitive node of the circuit – to avoid parasitic coupling via the common inductances of the bond wires. The bias lines used in various parts of the amplifier are separated and filtered to avoid parasitic coupling of the high dynamic range signals to the more sensitive front part of the circuit.

4.3.2. Sensitivity of the circuit to the spread of the technological parameters

Presumably due to the fact that the DMILL production volumes are relatively moderate because of price and the specialized application fields, the maximum spreads of the device parameters guaranteed by the foundry from run to run as well as matching are poorer than for standard CMOS technologies.

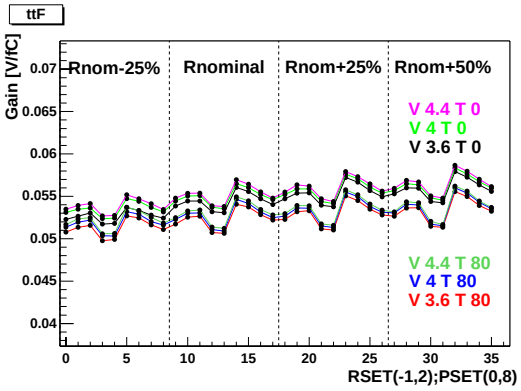


Figure 4.8: Simulation of pulse gain of the full chain as a function of process parameter variations (resistors from –25% to +50%: RSET -1÷2, CMOS corner parameters: PSET 0÷8, temperature from 0 to 80°C, power supply ±10%). The variations of the parameters are from batch to batch. For a given batch the matching of the device parameters on chip/wafer is much better.

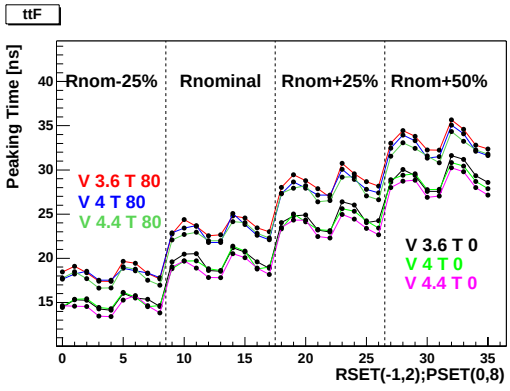


Figure 4.9: Simulation of the peaking time as a function of process parameter variations (resistors from –25% to +50%, CMOS corner parameters, temperature from 0 to 80°C, power supply ±10%).

The dispersion of the beta parameter for the BJT was already mentioned. In addition to that, one can expect from run to run, the dispersion of the threshold voltages for the

PMOS transistor to be in the range of -0.69V to -1.15V, slightly lower spread for NMOS devices from 0.69V to 1.05V and ±25% spread for the value of the resistors[5].

Special attention is needed in order to provide stable operating points of the devices, which are affected by the high spread of the parameters and their drifts after irradiation. In the particular case of DC coupled gain stages, the drifts of the offsets implied by the parameter spreads could be propagated and amplified, thus moving biases of the sub-circuits out of the operating points.

During the optimization of the circuit special attention has been paid to reduction of possible variations in the circuit parameters with operating conditions (temperature and power supply) and the variations of process parameters from run to run mentioned before. In order to illustrate possible effects a parametric simulation, taking into account all possible variation of the process parameters combined with the variation of temperature and power supply, has been setup. Figures 4.8 and 4.9 show simulation results for gain and peaking time respectively for various combinations of power supply (±10%), operating temperatures (0 and 80°C) and corner parameters (RSET and PSET) defined by the DMILL vendor.

4.3.3. Additional noise sources and second order effects affecting the noise performance of the SCTA128VG chip

The equivalent schematic of the bipolar preamplifier including all noise sources is shown in Figure 4.10.

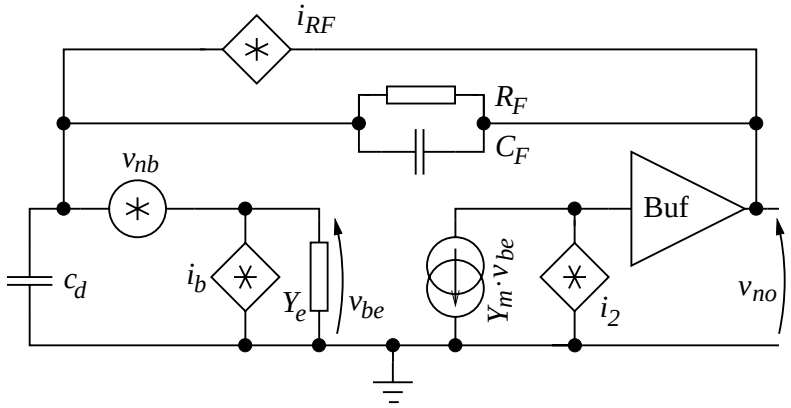


Figure 4.10: Equivalent schematic of the transimpedance amplifier including all noise sources.

It contains all noise sources related to the input transistor as in the model described in Chapter 3, and in addition an equivalent current noise source i_{RF} related to the feedback resistor described by spectrum:

$$\overline{i_{RF}^2} = \frac{4 \cdot k \cdot T}{R_F} \Delta f \qquad (4.1)$$

As one can see, the noise spectrum is inversely proportional to the value of the resistor, and therefore for the case of transimpedance amplifiers, the resistor noise has to be taken into account for the final calculation of the ENC. The contribution of the feedback current noise source to the final value of the preamplifier output noise can be described by the equation:

[5] To some extent the quoted spreads are correlated since they include the drifts of the parameters after the irradiation.

$$\frac{\overline{v_{no\_iRF}^2}}{\Delta f}=\frac{4\cdot k\cdot T}{R_F}\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2}=\frac{4\cdot k\cdot T\cdot R_F}{1+\tau_f^2\cdot\omega^2} \tag{4.2}$$

Assuming as in case of the previous analysis that the overall shaping function of the preamplifier and shaper is equivalent to the CR-RC^3 type of filter, one can find the expression for the ENC related to the feedback resistor value as:

$$ENC_{iRF}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty\frac{\overline{v_{no\_iRF}^2}}{\Delta f}\cdot\frac{1}{\left(1+\tau_f^2\cdot\omega^2\right)^3}\partial f\right)^{\frac{1}{2}} \tag{4.3}$$

And finally:

$$ENC_{iRF}[e^-]=\frac{e^3}{36}\cdot\sqrt{\frac{5}{3}}\cdot\sqrt{t_{peak}}\cdot\sqrt{\frac{4\cdot k\cdot T}{R_F}}\cdot\frac{1}{q} \tag{4.4}$$

For the actual values of the feedback resistance of 80kΩ and peaking time of 20ns one finds that the contribution of the feedback resistor to the overall noise for CR-(RC)^3 shaper is about 290e$^-$ ENC.

For all calculations of the ENC of the front-end amplifiers performed until now we have assumed an ideal CR-(RC)^3 shaping function. Although the pulse shape of the front-end amplifier response is very similar to the ideal CR-(RC)^3, one should expect an influence of the non-equalized time constants of the preamplifier and shaper stages as well as AC couplings on the noise filtering and the amplitude of the response.

Although there is no universal analytical solution for the response amplitude in case of accurate shaping function, the correction factors can be found numerically for a given amplifier type. As it was already mentioned, the accurate shaping function of the SCTA128VG amplifier can be represented by one stage of CR-(RC)^1 filter with time constant τ_d equal to 10ns, followed by two stages of integrators with time constant τ_i equal to 4.7ns and two AC coupling with time constant τ_{AC} close to 300ns. Numerical calculations show that the response amplitude of such a shaper is 1.2486 times higher than the case of the ideal CR-(RC)^3 filter providing 20ns peaking time (time constant τ_{id} equal to 6.666ns).

Solving the following integrals for parameters of the SCTA128VG amplifier and comparing the results with the numbers derived for an ideal CR-(RC)^3 filter one can find correction factors for ENC contributed by series and parallel noises.

$$ENC_{Ser\_CRRC3}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty\overline{v_{ns}^2}\cdot\frac{c_d^2}{C_F^2}\cdot\frac{\tau_{id}^2\cdot\omega^2}{\left(1+\tau_{id}^2\cdot\omega^2\right)^4}\partial f\right)^{\frac{1}{2}} \tag{4.5}$$

$$ENC_{Ser\_SCTA128VG}[C]=\frac{2\cdot e^3\cdot C_F}{9\cdot 1.2486}\cdot\left(\int_0^\infty\overline{v_{ns}^2}\cdot\frac{c_d^2}{C_F^2}\cdot\frac{\tau_d^2\cdot\omega^2}{\left(1+\tau_d^2\cdot\omega^2\right)^2}\cdot\frac{1}{\left(1+\tau_i^2\cdot\omega^2\right)^2}\cdot\frac{\tau_{AC}^4\cdot\omega^4}{\left(1+\tau_{AC}^2\cdot\omega^2\right)^2}\partial f\right)^{\frac{1}{2}} \tag{4.6}$$

$$ENC_{Par\_CRRC3}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty \frac{\overline{i_{np}^2}}{C_F^2}\cdot\frac{\tau_{id}^2}{\left(1+\tau_{id}^2\cdot\omega^2\right)^4}\,\partial f\right)^{\frac{1}{2}} \tag{4.7}$$

$$ENC_{Par\_SCTA128VG}[C]=\frac{2\cdot e^3\cdot C_F}{9\cdot 1.2486}\cdot\left(\int_0^\infty \frac{\overline{i_{np}^2}}{C_F^2}\cdot\frac{\tau_d^2}{\left(1+\tau_d^2\cdot\omega^2\right)^2}\cdot\frac{1}{\left(1+\tau_i^2\cdot\omega^2\right)^2}\cdot\frac{\tau_{AC}^4\cdot\omega^4}{\left(1+\tau_{AC}^2\cdot\omega^2\right)^2}\,\partial f\right)^{\frac{1}{2}} \tag{4.8}$$

Finally the correction factors for ENC contributed by series and parallel input noises, *CFS* and *CFP*, will be as follows:

$$CFS=\frac{ENC_{Ser\_SCTA128VG}}{ENC_{Ser\_CRRC3}}=1.035 \tag{4.9}$$

$$CFP=\frac{ENC_{Par\_SCTA128VG}}{ENC_{Par\_CRRC3}}=1.064 \tag{4.10}$$

The remaining question will be the value of the correction factor for the correlation term. Comparing the output noise spectra for collector current shot noise and for correlation term (equations 3.21 and 3.23) one can notice that the frequency characteristic is identical in both cases. Therefore the correction factor for the correlation term will be equal to the correction factor for series noise.

Although the effect of non-equal time constants is visible, its magnitude is limited to the range of a few percent. Therefore, the approximation of the amplifier transfer function by CR-$(RC)^3$ filter for qualitative analysis is fully acceptable. For the comparison of the SCTA128VG measurement data with the predicted numbers we will use a model described in Chapter 3 and supplemented with the correction factors for the corresponding noise sources.

4.3.4. Results of the evaluation of the SCTA128VG front-end amplifier

The general architecture of the SCTA128VG chip was presented in Chapter 1. The 128 outputs of the front-end amplifiers are connected to the Analogue Delay Buffer (ADB) followed by the analogue multiplexer (AMUX) and output buffer.

Since there is no direct access to the outputs of the amplifiers, the evaluation of the front-end part has to be done by measurement of the response of the full signal chain including preamplifier, shaper, ADB, AMUX and output buffer. The gain of the front-end amplifier is about 55mV/fC. The gain of the output buffer of the analogue multiplexer is in the range of 0.8[V/V]. Therefore the final gain of the whole read-out chain is roughly 44mV/fC. All figures in this section showing the measured data for gain and linearity refer to the full signal chain (front-end amplifier, ADB and AMUX).

The dynamic range of the amplifier is designed for input charges of up to 12fC, which together with the gain of 44mV/fC gives a full swing at the output of the chip in the range of 530mV. The current in the input transistor is controlled by an internal DAC and can be set within the range 0 to 320µA.

The basic parameters of the chip have been evaluated using internal calibration circuitry. The internal calibration circuitry provides a well-defined voltage step at the input of the calibration capacitors connected to every channel. Since the characteristic of the calibration DAC can be measured, the inaccuracy of the electronic calibration is related only to the deviation of calibration capacitors from the nominal value and the mismatch of the resistors used for scaling of the calibration voltage. For comparison with the results obtained with the electronic calibration, the absolute calibration of the chip in the set-up with a silicon pad detector and beta source is also presented.

The basic parameters of the amplifier are speed, gain, linearity and noise performance. The pulse shape at the output of the front-end amplifier has been evaluated by scanning the delay of the calibration signal with respect to the 40MHz-sampling clock for the analogue pipeline. In order to normalize the results to the absolute time scale the measurement has been repeated for two consecutive values of the trigger delay. The polarity of the signal (see Figure 4.5) is inverted in the ADB readout stage.

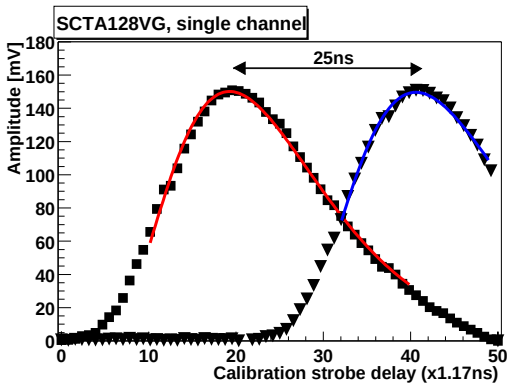


Figure 4.11: Pulse shapes at the output of the multiplexer obtained from the delay scan for two consecutive trigger delays.

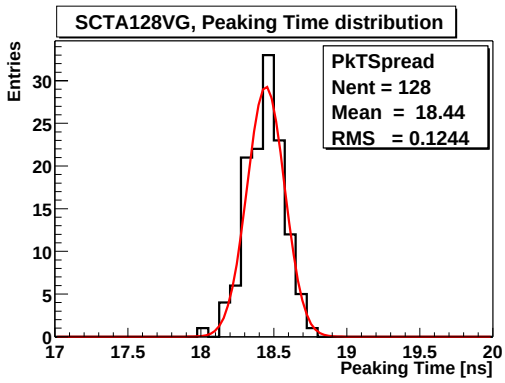


Figure 4.12: Distribution of the channel peaking times in one SCTA128VG chip. The rms spread is about 0.6%.

Figure 4.11 shows the example of the measurement done for one typical channel of the SCTA128VG chip. The injected charge was 3.5fC. The 18ns peaking time obtained for open channel inputs is in the range expected when considering the variations of the process parameters. The distribution of the peaking times in one SCTA128VG chip is shown in Figure 4.12. The rms spread of the peaking times is in the range of 0.6%.

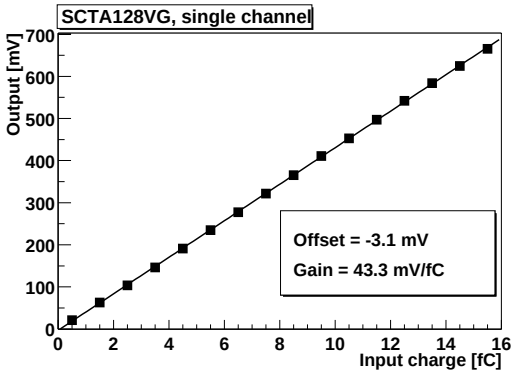


Figure 4.13: Gain linearity for one channel of the SCTA128VG chip.

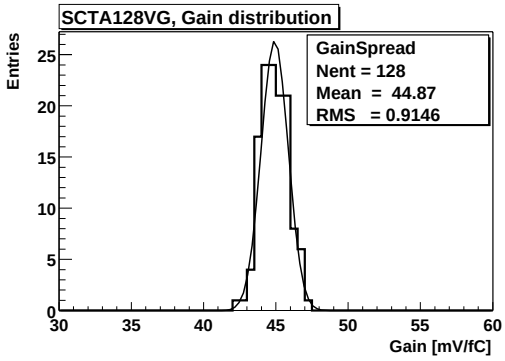


Figure 4.14: Distribution of channel gains in one SCTA128VG chip. The rms spread is in the range of 2%.

Figure 4.13 shows the gain and the linearity for one channel in the chip. The gain is 43mV/fC and maximum integral non-linearity error is less than 2% for a signal range up to 16fC, which is the maximum scale of the calibration DAC. The overall distribution of the gain in one SCTA128VG chip is presented in Figure 4.14. The rms spread of the gains is about 2%, which is sufficiently good for tracking applications.

The noise measurements have been made for the whole chip working with a 40MHz clock sampling data into the analogue memory and for random readout of ADB cells. In this way any pedestal variation between ADB cells and switching noise will contribute to the measured noise performance of the front-end. The distributions of the ENC in one SCTA128VG chip for various input transistor biases are shown in Figure 4.15. For the input transistor current ranging from 120µA up to 300µA the equivalent noise charge varies between 480 and 630e-. The rms spreads of the ENC are in the range of 2 to 2.5%.

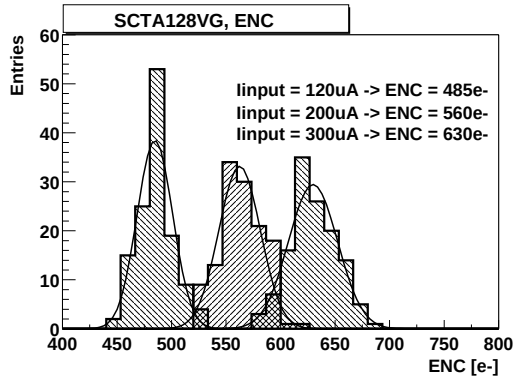


Figure 4.15: Distribution of ENC in a single SCTA128VG chip for different bias current in the input transistor. The spread of the equivalent noise charge is in the range of 2 to 2.5%.

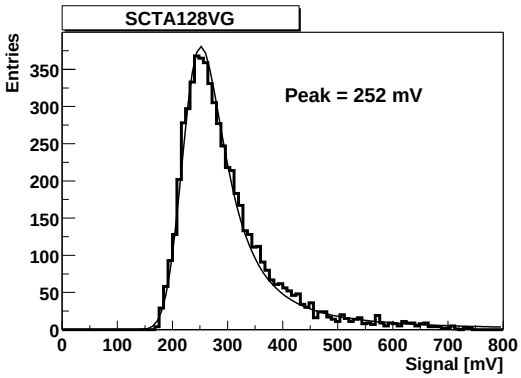


Figure 4.16: Histogram of data taken with silicon pad detector and a ^{106}Ru beta source showing Landau distribution with most probable value at 252mV.

In order to verify the measurements made with the internal calibration signal a set-up with a detector and beta source has been built. The SCTA128VG chip was connected to a SINTEF Silicon pad detector of thickness of 530µm. The detector bias voltage was set to 400V, 265V above the depletion voltage, providing sufficiently fast charge collection from the pads. The SCTA128VG chip was operating under nominal bias condition with the input transistor current set to 200µA. Figure 4.16 shows the signal distribution from the detector exposed to beta particles.

The gain extracted from this signal distribution, assuming the most probable value of the Landau distribution corresponding to a charge of 6.18fC [4.4], is 40.8mV/fC. This has to be compared with the gain of 45.6mV/fC measured with internal calibration circuitry for the channel connected to a detector pad. A difference of 10% between the results of the two measurements can be explained not only by the tolerance of the calibration capacitors and the inaccuracy of the band-gap reference, but also by a ballistic deficit for charge collected from the detector. The difference between charge collection time from the detector and charge injected from the calibration circuitry is in the range of 8 to 10ns, which is not negligible for a front-end amplifier with 18ns peaking time.

Figure 4.17 shows measurements of the noise performance of the amplifier loaded with various capacitances and performed for several input transistor bias current. The measurement points (markers) are in good agreement with the predicted noise figures (lines) obtained using the noise model described in Chapter 3 after correction with the

factors, *CFS* and *CFP*, and the addition of the contribution from the feedback resistor and spread of the ADB pedestals (~1.1mV rms equivalent to 150e- ENC, see Figure 6.5). The overestimation of the noise figure for capacitances above 22pF is probably due to the increase of the peaking time for higher capacitive loads (see Figure 4.18) causing longer shaping and improving the noise filtering. Comparing the simulated and the measured noise figures one has to take into account the dispersion of the measured ENC (see Figure 4.15) due to the variation of parameters influencing the analogue performance of the amplifier such as spread of the bias currents and the beta parameters for the input transistors. Taking all these effects into account, one can say that the measured and predicted numbers are in quite good agreement.

Figure 4.18 shows the dependence of the peaking time of the amplifier-shaper on the input capacitive load as a function of bias of the input transistor. Higher degradation of the peaking time for the lower, below nominal, value of the transistor bias (120µA) agrees with the simulation result of the input impedance characteristic. For the nominal biases and load capacitance of about 20pF the obtained peaking time is very close to 20ns, which is a simulated value for the nominal process parameters.

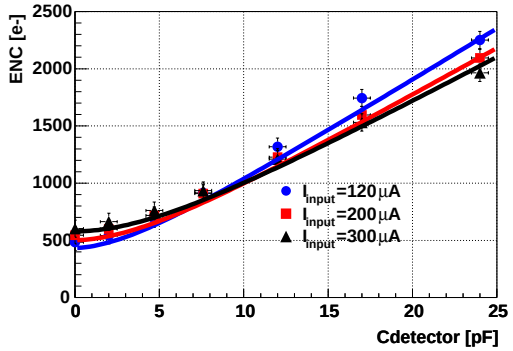


Figure 4.17: ENC of the front-end amplifier for various capacitive loads and bias conditions. The measurement points (markers) and the predicted noise figures using the model from Chapter 3 supplemented with the correction factors (lines) are shown.

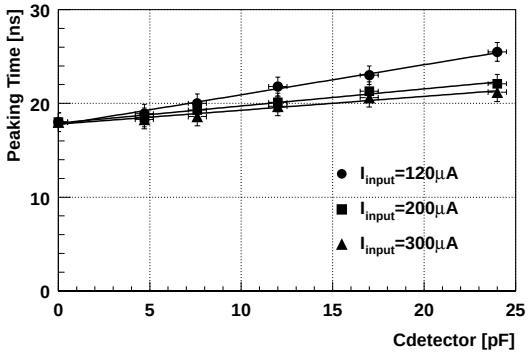


Figure 4.18: Peaking time of the front-end amplifier as a function of load capacitance and bias current of the input transistor.

Although the SCTA128VG chip is realized in DMILL radiation-hard technology the radiation effects in the devices cannot be ignored. The critical parameter is the noise in the front-end amplifier. A second order effect is possible degradation of matching, which may affect the uniformity of the channels in terms of gain and speed. The irradiations have been performed at CERN using a facility providing 10keV energy X-Rays at two dose rates: 8 and 33krad/min. No annealing has been applied. During the irradiation the analogue parameters: gain, noise and peaking time have been evaluated.

Figure 4.19 shows the distribution of ENC in one SCTA128VG chip before and after irradiation. The increase of parallel noise due to degradation of the BJT beta is as expected and can be neglected for a chip connected to a strip detector, in which case the serial noise due to the capacitive load is dominant. Figure 4.20 shows the distribution of channel gain in the SCTA128VG chip before and after irradiation. After irradiation one can observe a 7% decrease of gain and an increase of gain spread from 2 to 3%. The peaking time was unaffected by the X-Ray irradiation.

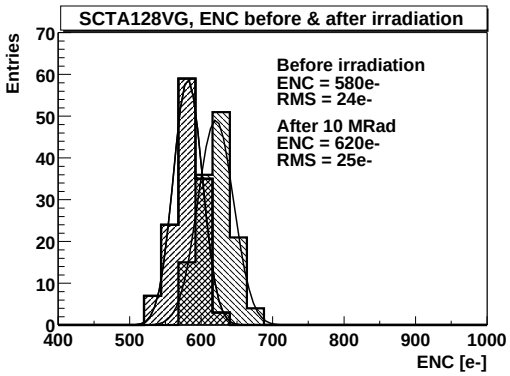


Figure 4.19: Distribution of ENC before and after 10Mrad. After irradiation the ENC increases by about 6%. The measurements are performed for 200μA bias current of the input transistor.

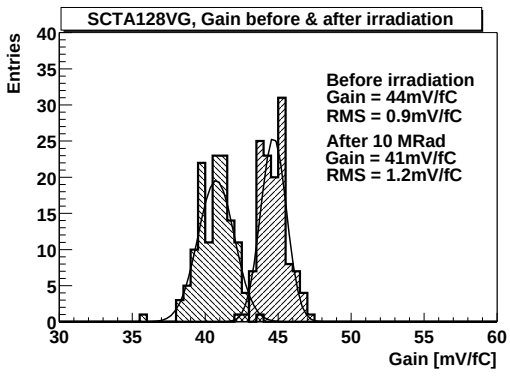


Figure 4.20: Distribution of channel gains before and after 10Mrad. After irradiation there is a noticeable drop of gain in the order of 7%, and an increase of gain spread from 2 to 3%.

4.4. Bipolar Transimpedance Front-End amplifier for ABCD3T chip

The schematic diagram of one channel of the ABCD3T front-end amplifier and comparator is shown in Figure 4.21. Each channel consists of three main blocks: the transimpedance preamplifier, the shaper providing amplification and integration of the signal, and the comparator providing amplitude discrimination and simple yes/no hit information.

4.4.1. The architecture of the front-end amplifier and comparator

The input stage of the ABCD3T amplifier is identical to the preamplifier and the first stage of the shaper implemented in the SCTA128VG chip[6]. The frequency characteristic and the input impedance of the preamplifier, as well as key issues concerning the design and optimization of the second stage amplifier have already been discussed in the section describing the SCTA front-end.

The pulse gain of the preamplifier and first stage of the shaper built with transistors T3 and M2 is in the range of 14mV/fC. The second amplifying stage of the shaper consists of a differential amplifier built with transistors *T16* and *T17* loaded with resistors *R18* and *R19*. The differential gain of the stage is around 5V/V, which results in an overall gain for the analogue chain of the order of 70mV/fC at nominal bias condition and 20pF capacitive input load. The differential amplifier works without any degeneration, which causes a small dependence of the gain on the shaper bias current (see Figure 4.27).

[6] The final version of the preamplifier employed in the SCTA128VG and ABCD3T chips was originally implemented in the ABCD2T chip, a prototype of the ABCD3T.

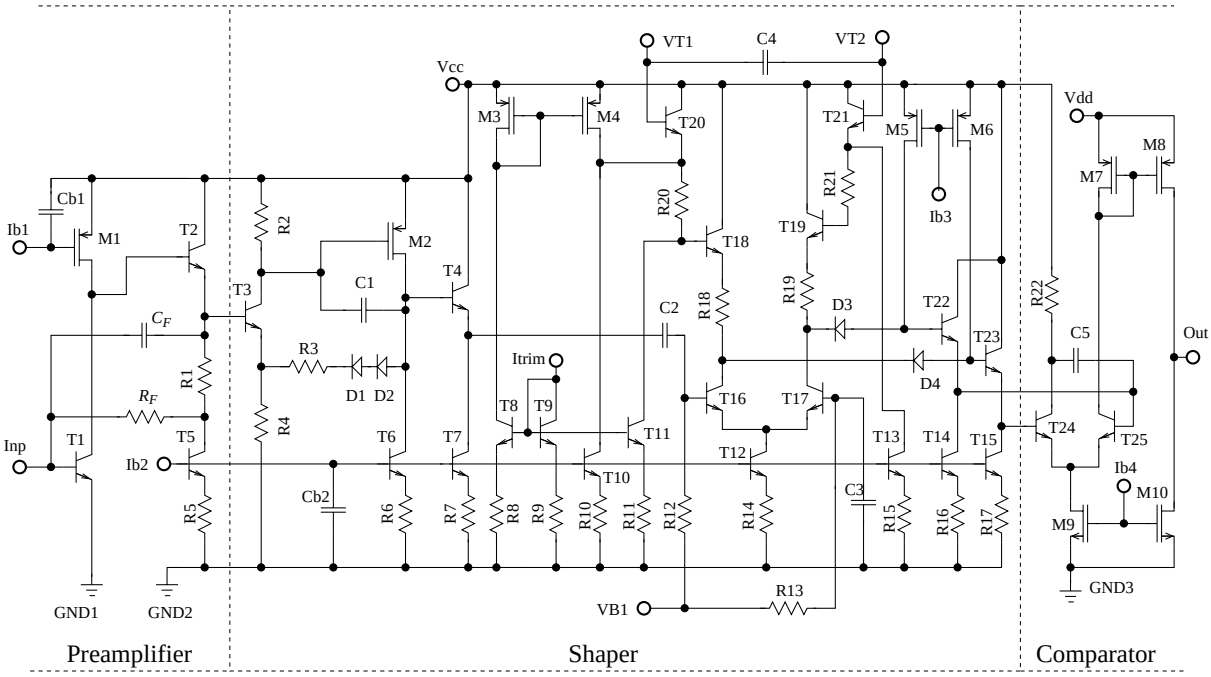


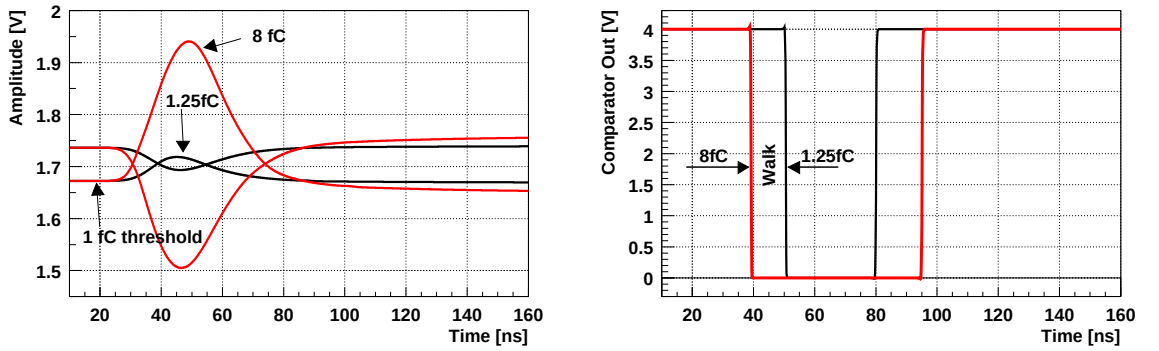
Figure 4.21: Schematic diagram of one channel amplifier-comparator implemented in the ABCD3T chip.

The bandwidth of the differential stage is identical to the bandwidth of the preceding amplifier, which provides basically the same shaping function as in the case of the SCTA128VG front-end. The use of only one AC coupling with a time constant of about 250ns modifies slightly the correction factors for series and parallel noise derived for the SCTA128VG front-end and causes an insignificant increase of the peaking time by about 2% (for nominal bias and load condition the peaking time is about 20.4ns). For the ABCD3T preamplifier/shaper the noise correction factors are:

$$CFS = \frac{ENC_{Ser\_ABCD3T}}{ENC_{Ser\_CRRC3}} = 1.015 \tag{4.10}$$

$$CFP = \frac{ENC_{Par\_ABCD3T}}{ENC_{Par\_CRRC3}} = 1.039 \tag{4.11}$$

The threshold voltage applied differentially (*VT1-VT2*) to the bases of transistors *T20* and *T21* through the transistors *T18* and *T19* appears on the load resistors *R18* and *R19*. Consequently the differential threshold voltage is applied to the input of the comparator together with the amplified detector signals (Figure 4.22a). Currents flowing through the transistors *T20* and *T21* are stabilized by the current sources *T11* and *T13*. This solution ensures stable operating points of transistors *T20* and *T21* i.e. well defined v_{be} voltage and consequently better matching. Diodes *D3* and *D4* biased with part of the shaper bias current ($I_{b3} = I_{b2}/6$) compensate the voltage drop (v_{be}) on the emitter followers (*T22* and *T23*) buffering the signals before the comparator input.



(a) (b)

Figure 4.22: ELDO simulation of amplifier/comparator response to 1.25 and 8fC signal charge for nominal bias condition (I_{input}=200μA, I_{sh}=30μA. V_{th}=1fC). (a) Differential signal as seen by the comparator input at bases of T24 and T25 and (b) comparator output.

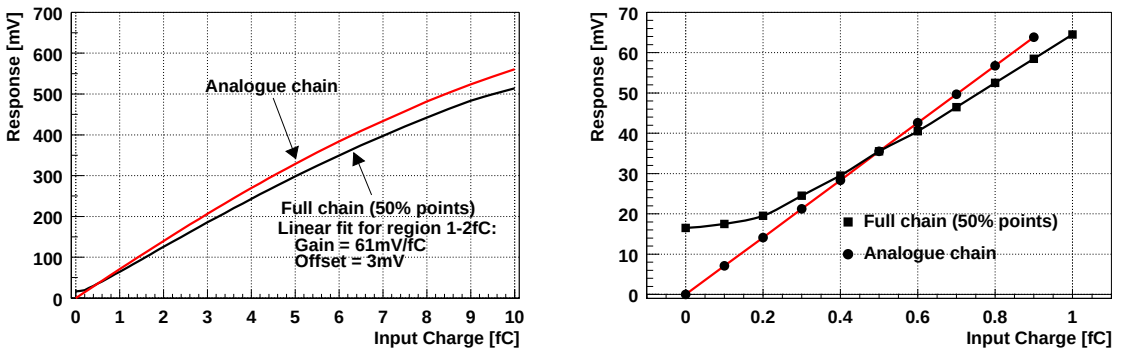
As already mentioned, one of the most critical issues of the binary architecture is the matching of gain and comparator offsets since a common threshold for 128 channels is used. The matching of the preamplifier gain depends mostly on the matching of feedback components C_f and R_f across a whole chip. In the case of the comparator, which is a fully differential structure, the offset spread depends on local matching of bipolar transistors (usually good) and of resistors.

It has been found [1.22] that the matching of the resistors available in DMILL technology is not sufficient to guarantee that the ATLAS SCT requirements regarding the threshold spread can be met by using a simple differential scheme for the discriminator. Further more, the already inadequate matching of the comparator offsets is significantly degraded after irradiation. Taking into account these aspects a scheme with individual threshold correction per channel has been implemented. This is realized by 4-bit DAC (TrimDAC), with four switchable ranges, implemented in each channel of the ABCD3T chip. The TrimDAC range, which is common for a whole chip, can be selected as 60, 120, 180 or 240mV. This allows precise trimming for the chips before irradiation by using the first range, and sufficient coverage for the larger offset spreads after the irradiation by using the higher DAC ranges. This solution is a compromise between achievable trimming accuracy and available space for the layout implementation.

The correction current I_{trim} supplied by the TrimDAC and mirrored by the transistor pairs *T8*, *T9*, *M3* and *M4* develops a correction voltage on resistor *R20* and finally is sunk by transistor *T11*. This effectively adjusts the potential on the base of *T16* and consequently the differential DC voltage on the comparator input since the common threshold voltage is applied on node *VT2*.

The discriminator is designed as a differential comparator in the Schmitt trigger configuration with the capacitive positive feedback provided by *C5*. The threshold voltage together with the input signals is applied differentially, which limits the matching issues to the preceding stage. An important parameter of the comparator determining the timing performance of the binary system is its time walk. In our case the time walk is defined for the comparator connected to the Front-End amplifier. Therefore, all timing effects, peaking time of the amplifier and response delay of the comparator itself are combined into one number. The time walk is defined as the increase of the delay of the comparator response as a function of the amplitude of the input charge for one, specified value of the comparator threshold voltage.

For the ATLAS SCT it is required that for the nominal threshold setting corresponding to 1fC charge, the time walk is below 16ns for input signals ranging from 1.25 to 8fC. The collector current of transistor *T25* is converted into a full swing output voltage signal in the buffer consisting of transistors *M7*and *M8* loaded with the transistor *M10* biased with 1/3 of the current flowing through transistor *M9*. For the nominal threshold polarity transistor *T25* is switched OFF (Out = LOW) and in response to the signal exceeding the threshold is switched ON (Out = HIGH).



(a) *(b)*

Figure 4.23: Comparison of transfer function of the full chain (amplifier and comparator) measured as a median (50% points) of the S-curves obtained from threshold scans for various input charges and transfer function of the analogue chain measured as a response amplitude as seen by the comparator input in: (a) range 0 to 10fC, (b) zoomed range 0 to 1fC; at nominal bias condition. ELDO simulation.

In the ABCD3T chip there is no access to analogue signals to measure directly gain and noise. Therefore the gain, noise and offset of the front-end have to be evaluated by scanning the discriminator threshold for various input charges applied by the calibration circuitry. For each threshold value a series of pulses is applied and the fraction of pulses, which fire the comparator, is measured. The threshold scan for a given input signal gives the so-called S-curve, i.e. counting rate[7] as a function of the threshold (see Figure 4.24a). Provided the noise has a Gaussian amplitude distribution, the S-curve is described by the complementary error function. The 50% points of the S-curve corresponds to a threshold equal to the signal amplitude, while the width of the S-curve contains information about the rms value of the noise. By performing these measurements for several values of the input charge one can extract the gain of all circuitry preceding the discriminator and the discriminator input offset i.e. build the transfer function of the full processing chain including the comparator.

Figure 4.23 shows simulation results for the transfer functions of the full chain including the comparator, obtained by scanning of the threshold voltage for various input charges, and the transfer function of the analogue chain alone. Ideally, these two characteristics should be identical. However, there are few effects that cause the two functions to differ. The positive feedback that ensures the fast response of the comparator depends on the amplitude of the pulse and its rise time, and is degraded for the smaller signals. As a consequence one observes a lower gain for input signals below 0.4fC, which should not be considered as a draw back of the design, since the nominal threshold is around 1fC (Figure 4.23b). The fixed offset of about 18mV is due to the misbalance of the bias currents of transistors *M9* and *M10*, which in fact is necessary to ensure the full swing for

[7] The counting rate can be normalized to the total number of triggers and presented as efficiency versus threshold figure (see Figure 4.22).

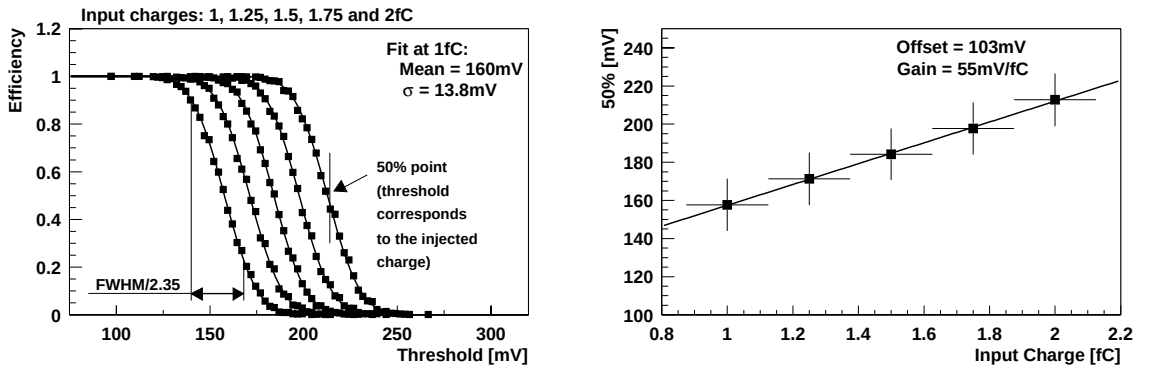
the output signals. For nominal bias condition and the circuit in equilibrium the difference between these bias currents is in the range of 20μA, which together with the input characteristic of the BJT explains the observed offset. The increase of the signal overdrive needed to switch the comparator at higher threshold values results in the lowering the overall gain of the full chain. That effect is linear and the non-linearity of the full chain for higher input signals follows the non-linearity of the differential shaper stage (Figure 4.23a).

Taking into account all effects causing non-linearity of the transfer function for low and higher input charges, the optimum region of the operation which should be used for the characterization of the front-end is between 0.5 and 4fC.

4.4.2. Measurements results for ABCD3T front-end

The general architecture of the ABCD3T chip has been discussed in Chapter 1. As was mention before, there is no access to the analogue signals to permit evaluation of the analogue performance of the front-end. All data must be processed through the whole chip including the Front-End, digital pipeline (multiplexed FIFO), derandomizer buffer and data compression unit, working with 40MHz clock which produces switching noise in the chip as well as in the external system. Providing the low-noise setup for the evaluation of the noise figure of the front-end amplifier loaded with the external capacitors connected directly to the ground is quite challenging. For that reason, for the noise evaluation of the ABCD3T chip, instead of standard capacitors a silicon strip detector of different strip length has been used (Figure 4.26).

As in the case of the SCTA128VG chip, the ABCD3T chip is equipped with calibration circuitry allowing for testing with internally generated pulses. Each channel of the front-end is equipped with a capacitor of 100fF allowing injection of test pulses. The test signals are distributed across the whole chip by four calibration lines, such that every fourth channel is connected to one line. The amplitude of the pulse can be set between 0 to 160mV, which corresponds to 16fC signal range. The strobe of the calibration signal can be delayed with respect to the clock phase within a range of about 50ns with 5-bit resolution. Since the delay circuit is realized as a series of inverters the overall delay is dependent on the process variation and therefore it has to be cross-calibrated using the external clock period.



(a) *(b)*

Figure 4.24:Examples of the S-curves taken during the threshold scans for 1,1.25, 1.5, 1.75 and 2fC input charges for single channel of the ABCD3T chip connected to 13cm Si detector (a) and the response function extracted from the 50% points of the S-curves (b).

Figure 4.24 shows examples of the S-curves acquired during the threshold scan for signals from 1 to 2fC range - the linear region of operation - for one typical channel of the

ABCD3T chip connected to 13cm silicon strip detectors and trimmed to 100mV threshold value (offset equal 103mV). The output noise for that particular channel extracted from the S-curve (Figure 4.24a) was equal to 13.8mV, which for the gain of 55mV/fC (Figure 4.24b) gives ENC of 1550e^-.

Figure 4.25 shows measured response curves of the front-end for 128 channels of the ABCD3T chip. The non-linearity above 4fC and below 0.5fC, as well as mean value of the offsets, being in the range of 20mV, agrees well with the simulated curve presented in Figure 4.23.

Figure 4.25: Response curves for 128 channels in one ABCD3T chip before threshold correction.

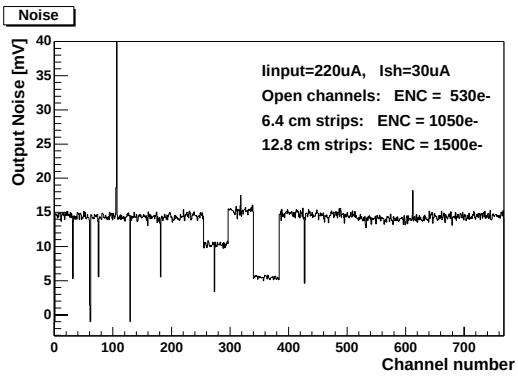


Figure 4.26: Output noise distribution across the 6-chip detector module.

In order to evaluate the noise of the ABCD chip a special module with six chips and two daisy-chained silicon strip detectors has been built. Five chips were fully bonded to 13cm long strips, while for one chip in the center of the module 1/3 of the strips were bonded to 13cm strips, 1/3 were bonded to one detector and 1/3 were left opened. The rms of the output noise across the module is shown in Figure 4.26. Combining the extracted value of output noise with the gain extracted from the threshold scans for various input signals gives average ENC values of 530, 1050 and 1500 electrons for 0, 6.5 and 13cm strips (which correspond roughly to 0, 9 and 18pF load capacitance respectively). These numbers are in good agreement with the noise model developed for the bipolar front-end.

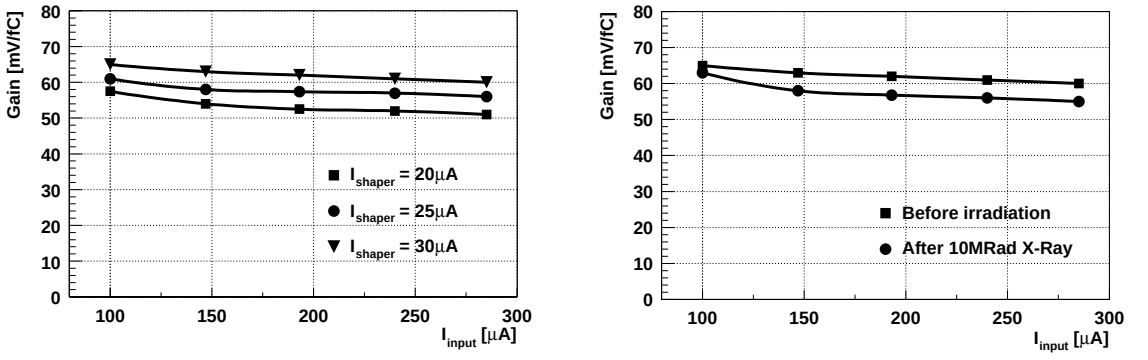


Figure 4.27: Gain of the ABCD3T chip as a function of the input transistor current for different bias condition of the shaper stage (a) and different beta factor of the BJT being degraded after the X-Ray irradiation (b).

Figure 4.27a shows the measurement of the front-end gain as a function of the input transistor current for wide range of bias conditions of the shaper stage. One can notice a

slight degradation of the pulse gain with increasing current in the input transistor, most probably due to the lowering open loop gain and over-compensation of the preamplifier. As expected, the front-end gain is influenced slightly by the shaper bias current affecting the gain of the differential amplifier in front of the comparator. Figure 4.27b shows the degradation of the gain of the front-end due to degradation of beta of the input transistor. It shows that after X-Ray irradiation the front-end can still operate over the whole range of the preamplifier bias current in high gain (high shaper current) region.

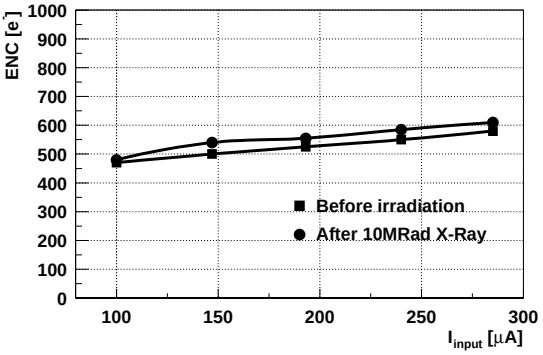


Figure 4.28: Noise as a function of the current in the input transistor before and after X-Ray irradiation.

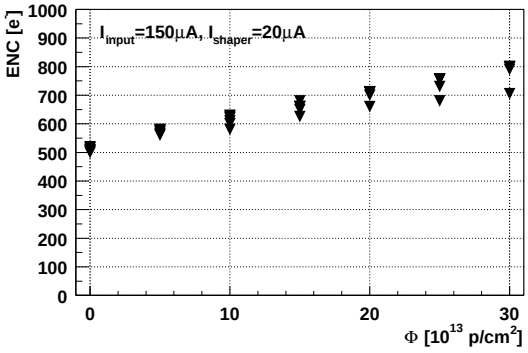


Figure 4.29: Increase of the parallel noise vs. particle fluence for proton irradiation.

Figure 4.28 shows the noise as a function of the collector current of the input transistor. Since the measurements show the results for the chips working with open inputs, the input capacitance can be neglected in a first approximation. Thus, the equivalent noise is determined by the parallel noise sources, i.e. thermal noise of the feedback resistor and the shot noise of the base current. Since the contribution of the noise from the feedback resistor is independent of the bias and irradiation, one can associate the variation of the ENC with the variation of the base current i.e. change of the bias and degradation of beta after the irradiation. After X-Ray irradiation one observes a small increase of noise as expected - because in this case we do not expect a large degradation of beta. Figure 4.29 shows the evolution of the parallel noise versus the particle fluence during the proton irradiation. Each marker represents the average of 128 channels of one ABCD chip irradiated on the 6-chip hybrid.

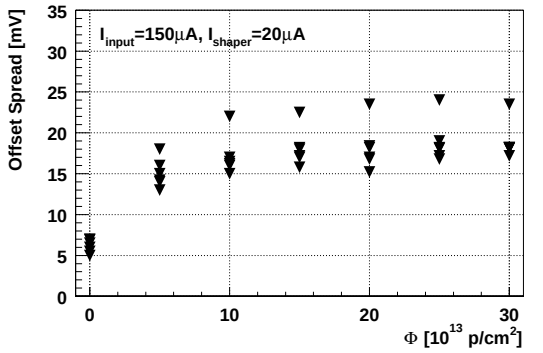


Figure 4.30: Increase of the discriminator offset spread vs. proton fluence.

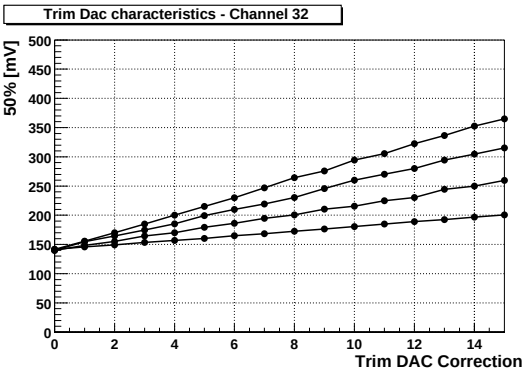
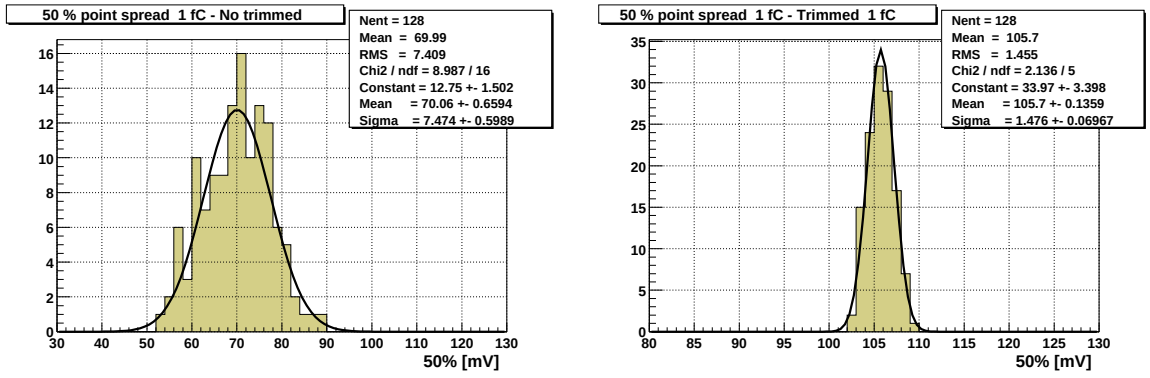


Figure 4.31: Characteristics of the TrimDAC in a single channel for four different range sets.

As mentioned, the initial, already significant spread of the comparator offsets is further degraded after irradiation with particles (pions, neutrons and protons). An example of

offset spread evolution as a function of the proton fluence is shown in Figure 4.30. The value of 3×10^{14} p/cm^2 at the end of the irradiation corresponds for SCT electronics to the total radiation dose after 10 years of the ATLAS experiment's expected operation. The increase of the original spread of the comparator offsets from 7 to 20mV rms can still be trimmed using the second range of the TrimDAC providing roughly 8mV step and final spread in the range of 3-4mV rms (~step/√12). The response curves of the TrimDAC for one typical channel of the ABCD chip for the four ranges measured with 2.5fC signal charge are shown in Figure 4.31. The ranges are very close to the designed value and the characteristics are linear over the whole DAC scale.



(a) *(b)*

Figure 4.32: Distribution of the 1fC thresholds for 128 channels in one ABCD3T chip before (a) and after the threshold correction (b). Note the different x-axis scale in the two cases.

The distribution of the comparator thresholds equivalent to 1fC charge is shown in Figure 4.32a. The spread is dominated by the offset spread since the gain dispersion is usually negligible. The threshold spread at 1fC after applying the trimming procedure is shown in Figure 4.32b. The obtained rms value of the spread is below 1.5mV, which agrees with the theoretical number defined by the step of the TrimDAC. For the gain of 60mV/fC it provides threshold uniformity better than 3%.

The time walk of the discriminator can be evaluated by scanning the delay of the calibration pulse with respect to the clock phase. For a given input charge the fraction of pulses which fire the discriminator is measured as a function of the calibration pulse delay. In order to provide better absolute accuracy the presented results were obtained using an external pulse generator instead of the internal calibration circuitry. The edge of the calibration pulse was set around 8ns, which simulates the realistic charge collection time in the silicon detector and reproduces the proper pulse shape with longer, ~24ns, peaking time. The result of the delay scans for a single channel loaded with a 13cm Si strip detector, working with threshold corresponding to 1fC and for various input signal is shown in Figure 4.32a. One can notice lower efficiency of the S-curve measured for 1.25fC input charge. This can be explained by the small overdrive of the input signal, which is in the range of one sigma noise (0.25fC equivalent to 1500e$^-$). From the delay scans as shown in Figure 4.32a one can extract the time walk of the comparator. The values of the time walk are plotted in Figure 4.32b. The measured time walk of the comparator for a channel loaded with a 13cm Si strip detector is around 15ns, which satisfies the ATLAS SCT requirements.

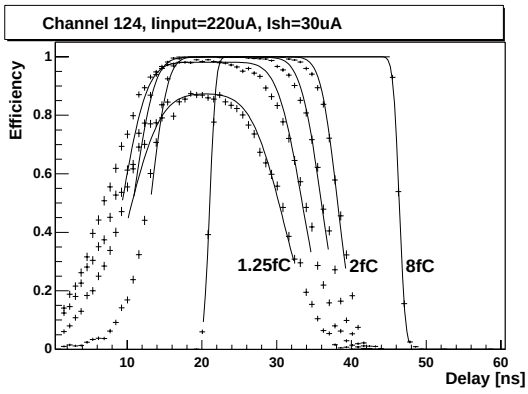


Figure 4.33: Delay scans for a single channel for input signals of 1.25, 1.5, 1.75, 2 and 8fC at a threshold corresponding to 1fC.

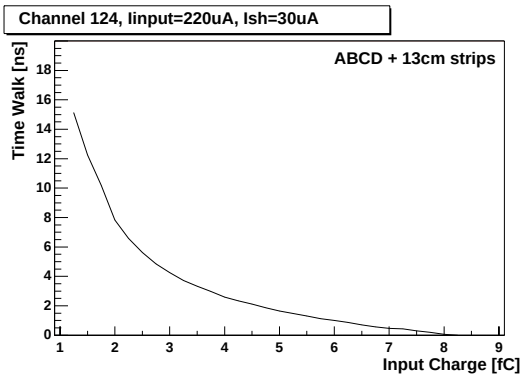


Figure 4.34: Walk time for a single channel of ABCD3T chip loaded with 13cm detector working with nominal bias conditions.

In the chip working with a common threshold applied to all channels, one can expect the spread of the time walks to be due to the spread of the comparator offsets discussed before. Keeping in mind the relatively high sensitivity of the time walk to effective overdrive for low input signals one can better see the importance of keeping the spread of the comparator offsets below the specified 0.05fC value.

4.5. CMOS implementation of the transimpedance preamplifier

An ABCDS-FE test chip has been designed and prototyped to investigate performance of a deep submicron process when applied for the fast binary front-end required for the ATLAS Semiconductor Tracker [1.11]. The prototype chip comprises 64 channels of front-end amplifiers and comparators and an output shift register. The design has been implemented in a 0.25μm IBM technology using the radiation hardening design method.

The schematic diagram of one channel of the ABCDS-FE chip is shown in Figure 4.35.

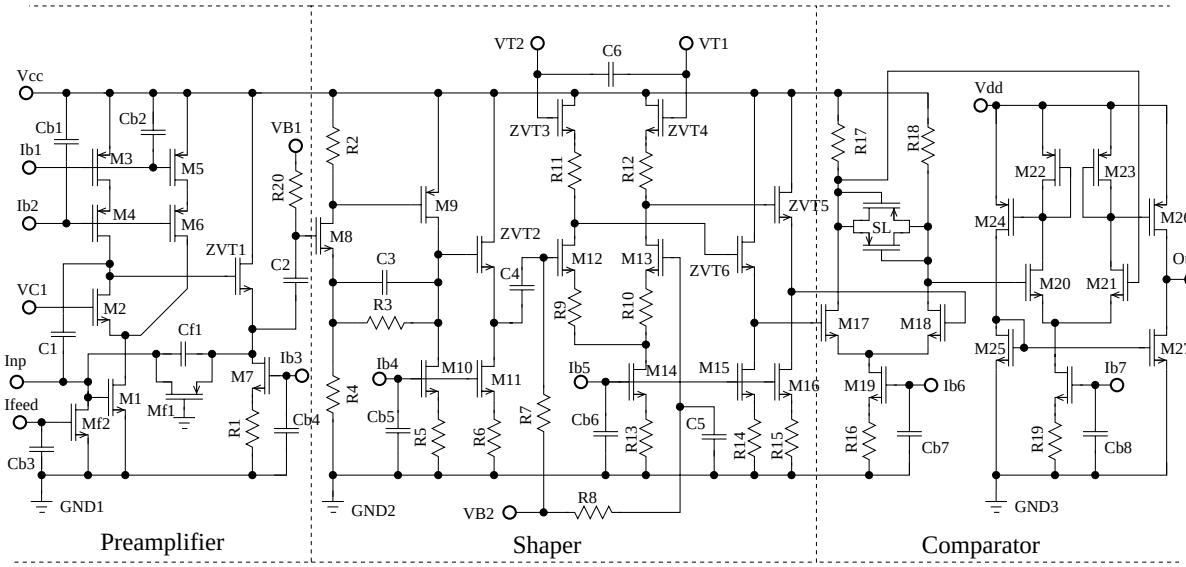


Figure 4.35: Schematic diagram of one channel of the ABCDS-FE chip.

A channel consists of three basic blocks: a fast transimpedance preamplifier with 14 ns peaking time, a shaper providing additional amplification and integration of the signal and a differential discriminator stage. The preamplifier stage is designed as a fast

transimpedance amplifier employing an active feedback circuit. The choice of architecture was determined by the possibility to obtain a much higher bandwidth of the preamplifier stage than in the case of simple resistive feedback using low-resistivity polysilicon resistors available in the process used.

The cascode amplifier employed in the preamplifier stage is a classical structure with an NMOS input device *M1* of dimensions 3000µm/0.5µm and PMOS cascode current source load. The dimensions of the input transistor allow for operating the device close to weak inversion, which is necessary to keep the excess noise factor Γ low, at about 1.3 [4.2]. The total gate capacitance of the input transistor including Gate-to-Source and Gate-to-Drain overlap capacitances is in the range of 6pF.

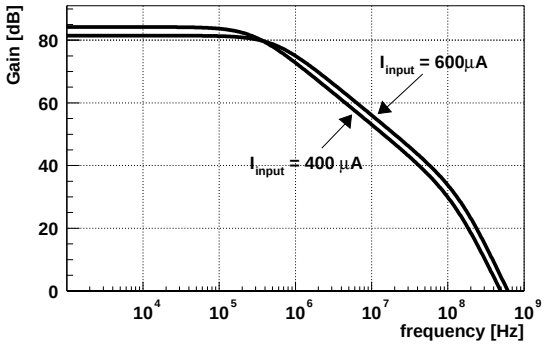


Figure 4.36: Simulation of the open loop gain for different bias conditions of the input transistor.

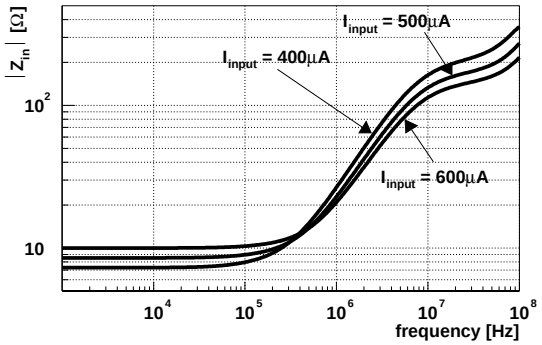


Figure 4.37: The input resistance of the preamplifier for various bias of the input transistor as a function of frequency.

An additional branch of the current source (transistors *M5* and *M6*) connected directly to the input transistor provides the desired bias current without degradation of the cascode output impedance and improves the open loop gain. In addition, the decrease of the nominal current in the main branch of the cascode allows us to decrease the sizes of the transistors used in the current sources, which limits the parasitic capacitances and increases the bandwidth of that stage. The configuration provides open loop gain of about 83 dB and the gain-bandwidth product in the range of 600MHz over a wide range of the input transistor bias conditions (see Figure 4.36).

The dimensions of the PMOS transistors used in the current sources allow biasing the input transistor up to 800µA, at the worst-case technology corner (highest Vt) and the lower limit for the voltage supply (-10% with respect to the nominal value of 2.5 V). The bias current ranging from 400 to 700 µA provides roughly 9 to 16mS transconductance of the input transistor, which is sufficiently high to obtain the desired noise performance for high input capacitance. High gain together with wide bandwidth of the amplifier helps to keep the input resistance low over a wide frequency range as shown in Figure 4.37.

For the bias of the input transistor with currents between 400µA and 600µA the input resistance is in the range of 100 to 150Ω at 10MHz, which is close to centre frequency of the shaper band. This ensures small cross talk and relatively small loss of input charge due to the detector interstrip capacitance. The simulation result of a full front-end loaded with the silicon strip detector with interstrip capacitance c_{is} equal to 7pF (roughly 20pF total load capacitance) is shown in Figure 4.38. The cross talk at the comparator input is less than 6% of the amplitude.

The phase compensation of the preamplifier stage is provided by two metal-to-metal capacitors *Cf1* and *C1* with a total capacitance of 190fF, which also decreases the input impedance for high frequencies. A large phase margin, above 80 degrees, is obtained for a wide range of bias conditions of the preamplifier and the feedback circuit. The phase margin can be further improved if needed, by controlling the feedback current i.e. decreasing the transconductance of the feedback transistor with the penalty of a slight increase of the width of the response pulse. The phase margin and preamplifier response for different bias conditions and nominal input capacitance of 20pF are shown in Figure 4.39 and Figure 4.40 respectively.

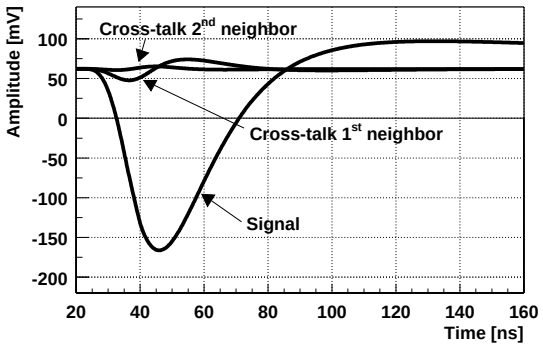


Figure 4.38: Results of transient simulation of the full Front-End responding to 3.5fC signal charge in one of the channel. The value of the interstrip capacitance was set to 7pF (effective load capacitance in the range of 20pF).

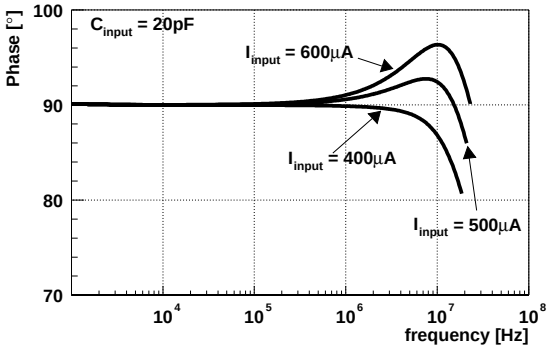


Figure 4.39: Simulation of the phase of the signal at the feedback loop output for loop gain higher than 0dB. End points of the figures define phase margins. Simulation done for 20pF nominal input load capacitance, nominal process parameter, 1μA feedback current and full range of input transistor bias.

The principle of the Active Feedback Preamplifier (AFP) is described in [4.3]. Transistor *Mf1* is placed in the feedback path of the cascode stage instead of conventional feedback resistor in a classical transresistance amplifier. Transistor *Mf1* works in saturation and is biased in moderate inversion by a current source built of transistor *Mf2*. Therefore, *Mf1* acts as a cascode stage across the feedback path. The transconductance g_m of that transistor determines the effective feedback resistor in an equivalent classical design. For the nominal bias current of 1μA, the transconductance of *Mf1* is about 8.5μS, which is equivalent to a 120kΩ feedback resistor in a classical design. The chosen value of the feedback current provides high linearity over a wide range of input signals, and fast response time (14.5ns peaking time for 20pF of input capacitance and nominal bias condition). The gain of that stage for a nominal bias condition (550μA in the input transistor, 1μA in the feedback transistor) and input capacitance of 20pF is of about 4mV/fC (see Figure 4.40).

The shaper stage consists of two AC-coupled amplifiers. The first amplifier is built in a single-ended configuration of two cascaded common source stages (transistors *M8* and *M9*). The closed loop DC gain is set by the ratio of resistors *R3* and *R4*. The stage integrates the signal up to about 20ns. The pulse gain is defined by resistive feedback and by the compensation capacitor *C3* of 130fF. The closed loop pulse gain of that stage is about 6 V/V, while the open loop gain of the stage is in the range of 50dB, which provides excellent linearity up to a signal of 40fC. The low power consumption of the stage (175μW without the buffer) makes this solution very attractive for many applications.

The second stage of the shaper is built as a differential amplifier (transistors *M12* and *M13*) and serves two purposes. First, it amplifies and converts the single-ended signal to a differential one. The differential gain of that stage is 2.5 V/V. In addition it interfaces the threshold voltage VT1-VT2 for the comparator, which is applied differentially through the gates of the transistors *ZVT3* and *ZVT4* connected as source followers. The same voltage appears on the load resistors *R11* and *R12* (the NMOS devices are "zero Vt" type) and produces a differential voltage at the outputs of the differential pair. The degeneration resistors *R9* and *R10* limit the gain of the stage and provide very good linearity over a range up to 12fC.

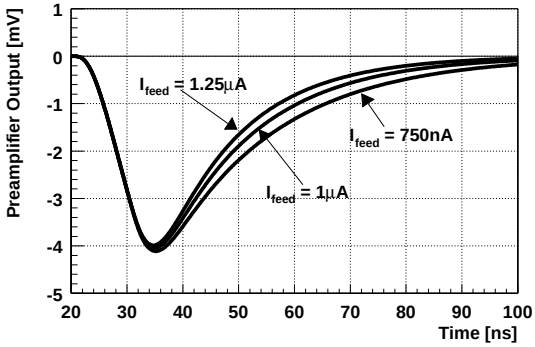


Figure 4.40: Preamplifier responses to 1 fC signal charge for various feedback currents, nominal input transistor bias (550 μA) and 20pF input load capacitance.

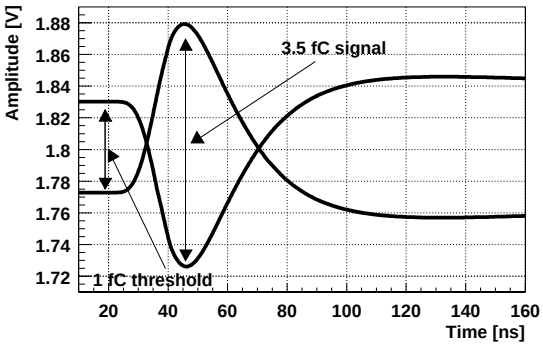


Figure 4.41:Response of the analogue chain to 3.5fC signal charge for nominal bias condition

The total gain of the analogue chain of the front-end preamplifier and shaper is about 60mV/fC. The response pulse is semigaussian, with 20ns peaking time. The simulated response to a 3.5fC signal with the threshold set at 1fC (nominal operating condition of the binary electronics for ATLS SCT) is shown in Figure 4.41.

The differential signal from the output of the shaper is buffered by two NMOS source followers and transferred to the first differential pair (*M17* and *M18*). The differential gain of the comparator input stage is 28dB. A high gain in combination with threshold input voltage ranging from 0 to 800mV might lead to the saturation of the stage. To prevent the saturation a swing limiter based on PMOS devices has been employed. The second section of the comparator is a classical two-stage amplifier with very high DC gain (~72dB). The current switched during the transitions is limited by the current source, which biases that stage. The last stage is supplied from the digital power supply. It has been found that this configuration of the power supply provides good separation (rejection of about 56dB) between noisy digital power supply lines and the comparator inputs.

Several components will contribute to final spread of the comparator offset:

- Offset of the M12 and M13 differential pair amplified by the gain of that stage (~2.5)
- Offsets of the transistors used in the threshold circuit (*ZVT3*&*ZVT4*), NMOS source followers and comparator stage
- Voltage mismatch due to the mismatch of the *R11* and *R12* resistors (14.7kΩ). For the used dimensions the matching of the resistors is estimated to be 0.5%.

Assuming a value of 1mV rms for the threshold voltage spread in transistor pairs employed and nominal bias of 2x30μA for transistors *M12* and *M13*, one can estimate the value of the comparator offset spread to be around 4.5mV rms.

An important parameter is the minimum overdrive of the comparator for fast pulses delivered from the shaper. For the nominal bias condition, the comparator requires at least 3mV overdrive in order to produce a full swing pulse at the output (the width of the input signal is in that case around 5 ns).

Another critical parameter of the discriminator is the time walk. As for the ABCD3T chip, the time walk is defined for the comparator connected to the Front-End amplifier. Thus, all timing effects, namely the peaking time of the amplifier and the response delay of the comparator itself are combined into this parameter. Time walk is defined as the delay of the comparator response to input charges of 1.2fC with respect to the response to 10fC, while the comparator threshold is set at 1fC. For a nominal input load and bias of the Front-End the total time walk has been simulated to be 12ns.

4.5.1. Noise performance of the active feedback CMOS FE amplifier

In real amplifiers one has to take into account the contribution of the noise from the feedback devices as well as impact of the real frequency characteristic of the shaper on noise filtering efficiency.

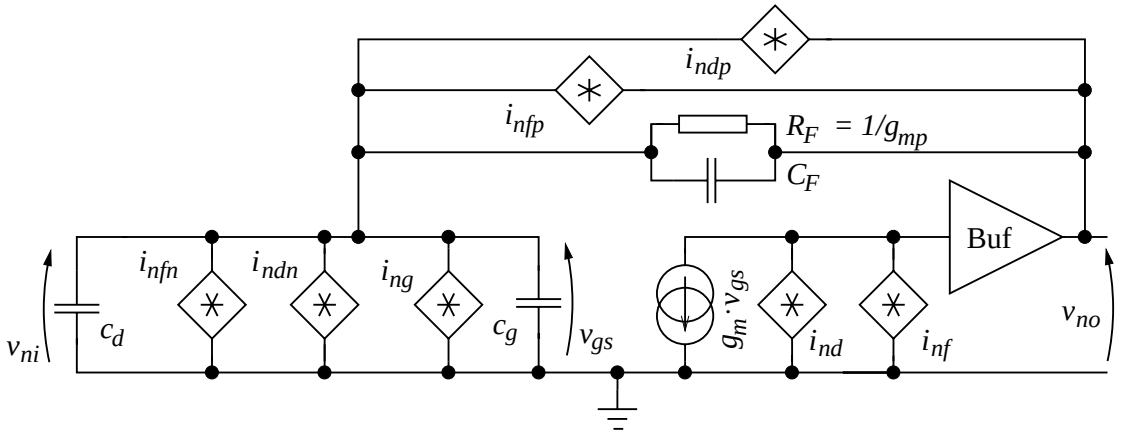


Figure 4.42: Equivalent schematic of the MOS transimpedance preamplifier with active feedback including all noise sources.

Figure 4.42 shows the equivalent schematic of the amplifier including the noise sources associated with the feedback PMOS transistor and the NMOS current source setting the feedback current. Both components will contribute channel thermal noise (i_{ndp} and i_{ndn}) as well as flicker noise (i_{nfn} and i_{nfp} sources). The total ENC of the real amplifier will be the sum of the ENC related to the input transistor noise sources described by equation (3.94) and the ENC corresponding to the current noise generators of the feedback circuit. As for the analysis done in Chapter 3 one may depict the noise fluctuation related to the feedback circuit $v_{no\_feed}(t)$ at the preamplifier output as:

$$v_{no\_feed}(t) = Z_F \cdot \left(i_{nfn}(t) + i_{nfp}(t) + i_{ndn}(t) + i_{ndp}(t) \right) \tag{4.12}$$

The channel thermal noise of the NMOS and PMOS transistors (noise sources i_{ndn} and i_{ndp}) can be evaluated accordingly to:

$$\overline{i_{ndn}^2},\ \overline{i_{ndp}^2} \ = 4 \cdot k \cdot T \cdot \gamma \cdot n \cdot g_m \, \Delta f \tag{4.13}$$

The g_m is the transconductance of the NMOS or PMOS device and γ is the noise factor calculated for the PMOS and NMOS transistors according to equation 3.47. The

contributions of the flicker noise from the PMOS and NMOS feedback transistors can be calculated as follows:

$$\overline{i_{nfn}^2},\ \overline{i_{nfp}^2} = \frac{K_a}{f}\cdot\frac{g_m^2}{C_{OXU}^2\cdot W\cdot L}\Delta f \tag{4.14}$$

Substituting the g_m, K_a, W and L with the parameters related to the PMOS and NMOS transistors from the feedback circuit one obtains expressions for the partial noise contributions from those devices.

Given that all mentioned noise sources are uncorrelated the output noise spectra density will be the following sum of terms related to NMOS and PMOS feedback transistors:

$$\frac{\overline{v_{no\_feed}^2}}{\Delta f}=\frac{R_F^2}{1+\tau_f^2\cdot\omega^2}\left(\overline{i_{nfn}^2}+\overline{i_{nfp}^2}+\overline{i_{ndn}^2}+\overline{i_{ndp}^2}\right) \tag{4.15}$$

Assuming a CR-(RC)^3 shaping type of the preamplifier-shaper chain one can write the expression for the equivalent noise charge related to the feedback circuit as:

$$ENC_{feed}[C]=\frac{2\cdot e^3\cdot C_F}{9}\cdot\left(\int_0^\infty\frac{\overline{v_{no\_feed}^2}}{\Delta f}\cdot\frac{1}{\left(1+\tau_f^2\cdot\omega^2\right)^3}\partial f\right)^{\frac{1}{2}} \tag{4.16}$$

Computing the integral and analyzing the flicker and thermal noise separately for NMOS and PMOS transistors one can obtain the expressions for the corresponding ENC contributions from each noise sources. The ENC contributions from the thermal noise of the feedback transistor is given as:

$$ENC_{th}[e-]=\frac{e^3}{18}\cdot\sqrt{\frac{5}{3}}\cdot\sqrt{k\cdot T\cdot n\cdot\gamma\cdot g_m\cdot t_{peak}}\cdot\frac{1}{q} \tag{4.17}$$

One can notice that the definite integrals of the components related to the flicker noise of feedback devices do not converge for frequencies decreasing toward zero. That is to say the CR-(RC)^n type shaper does not efficiently filter the flicker noise originating from the feedback transistors. This example shows the extra advantages obtained from the AC coupling between preamplifier, shaper and discriminator stages, which helps to filter that noise. Assuming the real time constant of the AC coupling in the presented ABCDFE chip, which is about ten times higher than the peaking time of the circuit, one can obtain the following expression for the ENC related to the flicker noise of the feedback transistors.

$$ENC_{1/f}[e-]=2.13\cdot g_m\cdot t_{peak}\cdot\sqrt{\frac{K_a}{W\cdot L}}\cdot\frac{1}{C_{OXU}}\cdot\frac{1}{q} \tag{4.18}$$

One can show that in the case of one stage AC-coupled the ENC related to the flicker noise of the feedback devices would be higher only by about 10%.

Figure 4.43 shows the ENC (left axis) and the equivalent feedback resistance (right axis) as a function of the feedback current. The same plot shows the comparison between noise of the AFP and equivalent passive resistive feedback. The operating region of feedback current providing the value of the feedback resistance in the range of 100kΩ is between 0.8 and 1.2μA. For that region of operation the parallel noise due to the AFP circuit is in

the range of 350 to 380e$^-$ ENC, whereas the noise in the case of use of a passive resistor in the feedback is below 200e$^-$. As already mentioned, the use of AFP instead of simple resistive feedback was determined by the possibility of obtaining a much higher bandwidth of the preamplifier stage than in the case of a simple resistive feedback. The relatively high parallel noise of the AFP circuit still has negligible influence for detector capacitances above 15pF, where the series noise due to the capacitive load dominates.

Figure 4.44 shows the total ENC of the active feedback and the partial contribution from various noise sources. One can see that the dominant noise source is the thermal noise of the transistors in the feedback and current source. In principle the transconductance of the NMOS transistor working as a current source could be reduced. However in practice, keeping the enclosed geometry layout rules in order to provide radiation hardness, the minimum aspect ratio for the NMOS devices is about 2.5. This keeps the minimum achievable transconductance of the device for a given current at a relatively high level. In the ideal case of the PMOS and NMOS transistor working in weak inversion and without excess noise, the noise performance of the AFP will be still higher compared to the simple resistive feedback circuit - by a factor equal to the sub-threshold slope *n* (see equation 4.17). The flicker noise filtered by two AC couplings in-between preamplifier, shaper and discriminator stages can be practically neglected in the analysis.

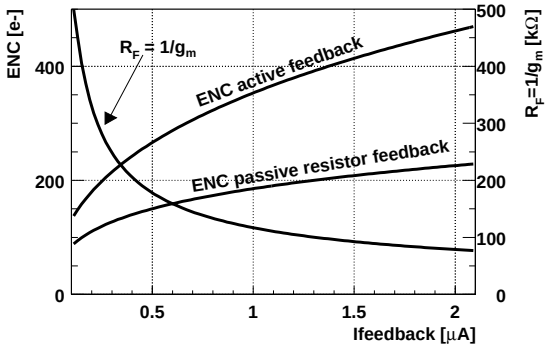


Figure 4.43: Comparison between ENC of the active feedback and equivalent passive resistor. Left axis shows ENC value and right axis shows equivalent feedback resistance.

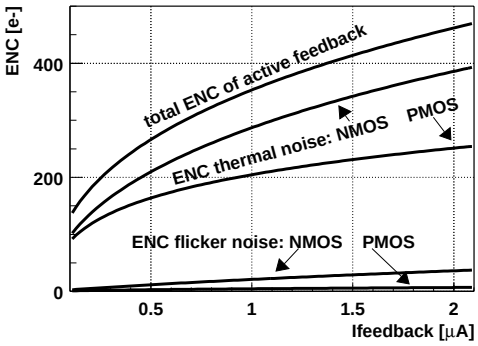


Figure 4.44: A total ENC of the feedback circuit and the partial contributions from various components.

The bandwidth of the ABCDS preamplifier compared to the bipolar design is about 30% lower. This results in a longer response pulse of the stage. Calculating the parameters of the preamplifier for feedback current around 1μA, one finds that the stage can be modeled by a single CR-RC stage with 14.5ns time constant. The integration time constant of the two stages of the shaper is in the range of 2.9ns. Together with 350ns time constant of two AC coupling it provides a 20ns peaking time, semigaussian pulse at the output of the shaper stage. Using the same approach as for the bipolar front-end one can obtain the following correction factors for series and parallel noise sources:

$$CFS = \frac{ENC_{Ser\_ABCDS}}{ENC_{Ser\_CRRC3}} = 0.999 \tag{4.19}$$

$$CFP = \frac{ENC_{Par\_ABCDS}}{ENC_{Par\_CRRC3}} = 1.16 \tag{4.20}$$

The Gate Induced Current (GIC) noise is typically represented by the equivalent input parallel noise source. However, examination of its spectrum at the preamplifier output and comparing with the spectrum of the channel thermal noise, shows that both frequency characteristics are identical (see eq.3.64 and eq.3.61). The same applies for the correlation term, which has exactly the same frequency behavior as the channel thermal noise at the preamplifier output (equation 3.63). Consequently for the GIC noise as well as for the correlation term one should use a correction factor derived for the series input noise. Although the flicker noise does not play a big role in the overall noise figure, in order to provide a full description and using the same approach one can show that the correction factor for that noise source is roughly 1.07.

4.5.2. Test results

The basic analogue parameters of the amplifier, such as pulse shape, gain, linearity and the noise performance were evaluated in detail for different bias and input capacitance loads using eight analogue test channels available on the chip. The gain, offset and noise of the full chain has been evaluated by scanning the discriminator threshold for a given input charge as described for the ABCD3T measurements.

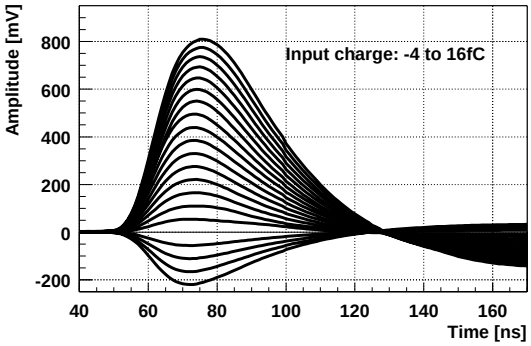


Figure 4.45: Response of the amplifier biased with nominal currents to the input charges from –4 to 16fC.

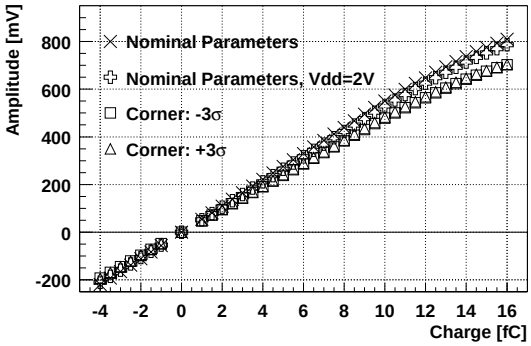


Figure 4.46: Linearity of the front-end amplifier for various process parameters as well as for nominal and limited power supply.

The ABCDS-FE chip includes fifty-six complete channels equipped with preamplifier, shaper and comparator readout by shift register. Figure 4.45 shows the measured response of the amplifier channel as seen by the input of the comparator for input charges from –4 to 16fC. The dynamic range and linearity of the analogue chain for nominal as well as for corner process parameters and decreased voltage supply is shown in Figure 4.46. As one can see, the good linearity is kept up to 12 fC range in all measured FE amplifiers. One can observe a few-percent change in gain for the chips from the corner runs and almost no difference for lowered power supply compared to the nominal one.

The gain, speed and the noise of the amplifier are functions of the bias, especially of the feedback current, which defines the transconductance of the feedback loop. The performance of the amplifier has been tested for wide range of the biases of the input transistor (between 400 and 700 μA) as well as feedback current (0.4 and 1.6 μA). The plots of the peaking time and gain for analogue channels are shown in Figures 4.47 and 4.48. Depending on the input bias current and feedback bias current the gain seen on the comparator input is between 50 and 65 mV/fC. The peaking time varies between 18 and 22 ns depending on the value of the feedback current.

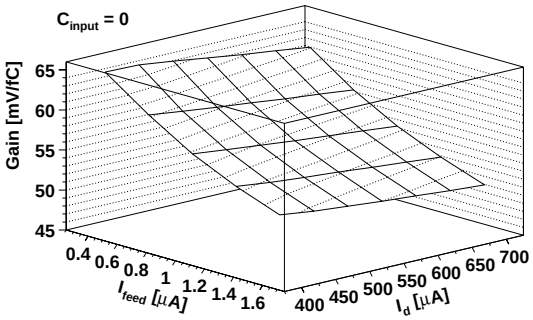


Figure 4.47:Front-end gain as a function of bias currents of the feedback transistor (I_{feed}) and the input transistor (I_d).

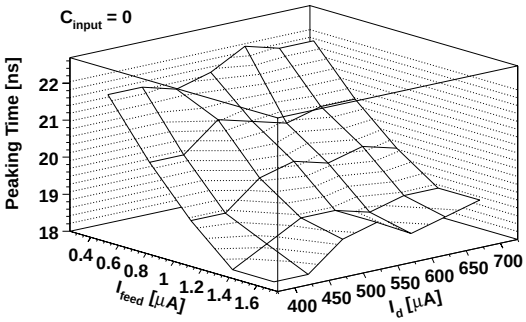


Figure 4.48: Peaking time as a function of bias currents of the feedback transistor (I_{feed}) and the input transistor (I_d).

The dependence of the peaking time on the input capacitance for various values of the feedback current is shown in Figure 4.49. The small variation of the peaking time with respect to the load capacitance confirms the low value of the input resistance of the preamplifier.

The comparison between the measured noise of the ABCDS-FE chip and the noise figure calculated using the model describing the CMOS transimpedance amplifier and supplemented with the correction factors is presented in Figure 4.50. The comparison has been made for the values of the biases used for the calculation of correction factors.

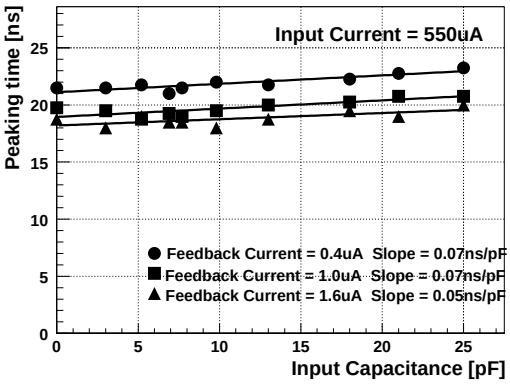


Figure 4.49: Peaking time as a function of input capacitance for various feedback currents.

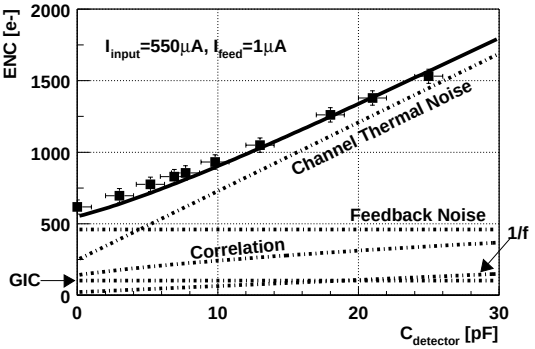


Figure 4.50: ENC of the ABCDS-FE chip measured for 550μA input current and 1μA feedback current (markers) and the calculated figure (line) showing all noise components obtained using model supplemented with the correction factors.

According to the model there are two significant noise sources: thermal noise of the channel and the parallel noise from the feedback circuit, the latter playing a role for lower input capacitances. The agreement between the model and measurement is excellent for the medium range of the input capacitances. A slight overestimation of the calculated number for the highest value of the input capacitance (25pF), is probably due to the increase of the peaking time (See Figure 4.49), which is not considered by the model. A discrepancy of approximately 8% for zero input capacitance remains an open question. For open inputs high sensitivity of the noise to the value of the feedback current (see Figure 4.51) suggests that the above-mentioned excess noise originates from the feedback

circuit. The noise performance of the Front-End for various biases and loaded with different capacitances is shown in Figure 4.51.

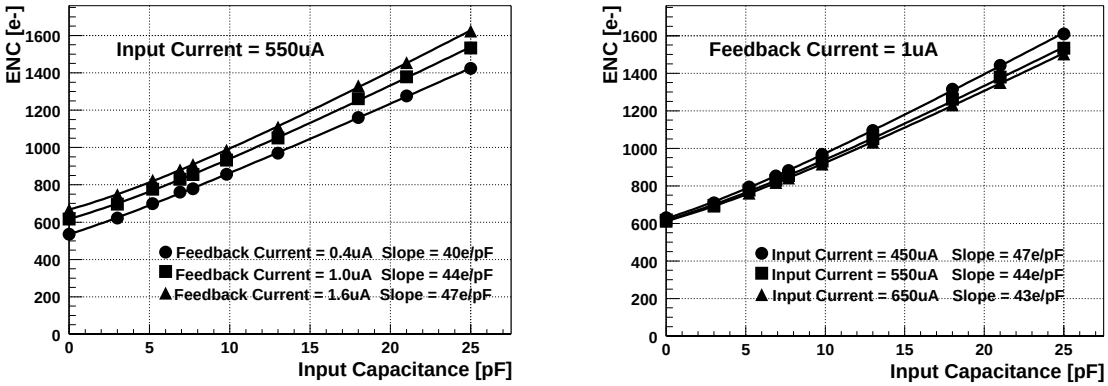


Figure 4.51: The noise figures as a function of the input capacitance measured for various biases of the input and feedback transistors. The measured points are fit to a function described by simplified noise model from Chapter1 (Figure 1.14 and equation 1.21). Slope factors describe the contribution of the series noise source.

The measurements of the full chain of the FE amplifier were focused on evaluation of matching of the parameters like gain and comparator offsets, as well as on the timing performance of the comparator. A single setting of the bias currents, namely 550μA for the input transistor and 1μA for the feedback circuit, has been used.

Figure 4.52 shows the response curve for the full chain of the front-end including the comparator. The complete agreement with the response curve of the analogue chain requires a comment, since one would expect to observe a similar gain reduction as for the ABCD3T chip, which was due to the comparator requiring higher overdrive at higher threshold settings. By coincidence, the differential threshold voltage applied on the gates of the transistors *ZVT3* and *ZVT4* working in source follower configuration is attenuated by a proportion that provides exact compensation for the loss of gain on the comparator. The very good linearity is provided up to 14fC of the input signal.

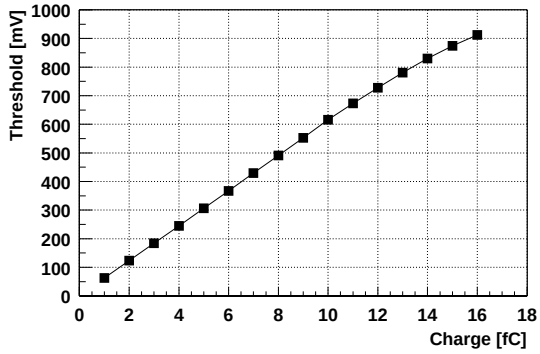


Figure 4.52: Example of the response curve for a typical channel of the ABCDS-FE chip and nominal bias conditions.

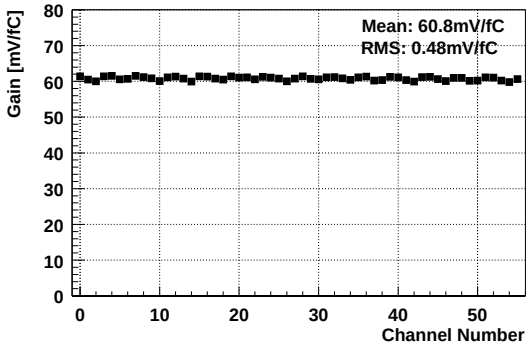


Figure 4.53: Distribution of channel gain across the ABCDS-FE chip biased with nominal current.

The measurements of gain and ENC for the nominal bias conditions agree well with the analogue measurements of a single channel. The distribution of channel gains in one typical ABCDS-FE chip is shown in Figure 4.53. The gain was extracted from the threshold scans made for 1, 2, 3 and 4fC input charge, in the linear region of the

amplifier. The mean value of the gain is 60mV/fC and the spread of the gain is well below 1% rms.

The distribution of the ENC measured for open inputs and nominal bias condition is shown in Figure 4.54. The rms spread is in the range of 3%. The distribution of comparator offsets is shown in Figure 4.55.

The rms value of the offset spread is around 3mV for all chips measured, which is about 5% of the amplitude response to a 1fC charge. The target value of the comparator offset spread for the SCT binary electronics has been achieved without employing the TrimDAC circuitry.

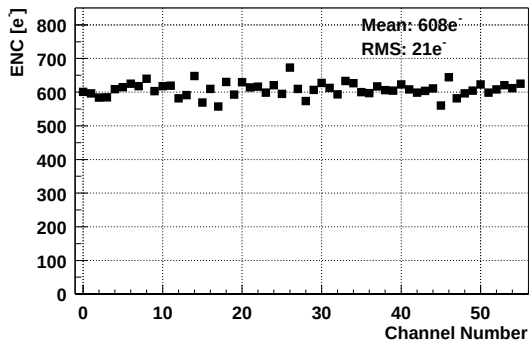


Figure 4.54: Distribution of the ENC measured for open inputs and nominal bias condition.

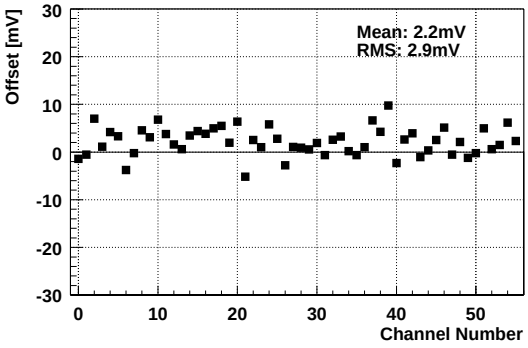


Figure 4.55: Distribution of the comparator offsets across the ABCDS-FE chip for nominal bias condition.

Figure 4.56 shows the delay scans made for the ABCDS-FE chip responding to 1.2 and 10fC signal charges when working with nominal bias and threshold (1fC) conditions. Figure 4.57 shows the distribution of time walk in one typical ABCDS-FE chip. Since a common threshold voltage equivalent to 1fC charge was applied to all channels, we would expect the variation of the measured time walks to be determined by the variation of effective thresholds for each channel. The average value of 12.5ns agrees well with the simulation.

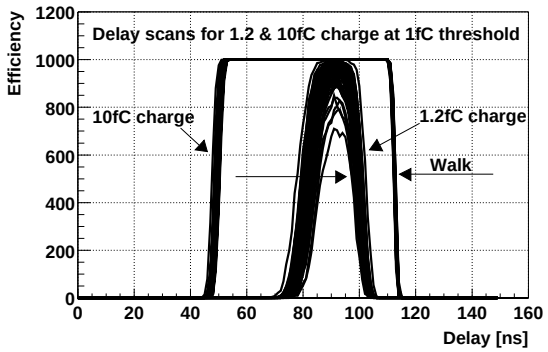


Figure 4.56: Delay scans for 56 complete channels of the ABCDS-FE chip working with nominal bias and threshold conditions (1fC) for 1.2 and 10fC input charge.

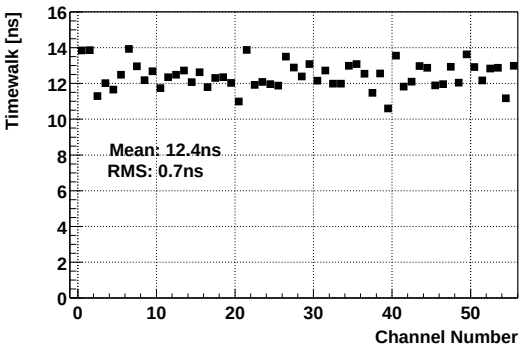


Figure 4.57: Distribution of time walk across one ABCDS-FE chip working with nominal bias conditions.

No noticeable degradation of any of the analogue parameters was observed after X-Ray irradiation up to a dose of 10Mrad.

4.6. Summary of the performance of the presented front-end electronics

All of the front-end amplifiers discussed, both in bipolar as well as in submicron CMOS implementations, meet the basic requirements for the readout electronics for silicon strip detectors for LHC experiments. Although the CMOS version can possible provide better noise performance, one has to remember that it can be achieved only by providing higher current to the input stage i.e. increasing power and especially the current consumption of the front-end. On the other hand the noise performance of the bipolar implementation is limited by the necessity of using relatively small transistors because of radiation hardness considerations. The noise performance is defined in this case by the base spread resistance contribution and can not be improved by increasing the input transistor current.

5. Some design issues related to mixed-mode operation of the Front End ASICs

This chapter deals with some design issues related to the mixed-mode operation of front end electronics working in full-scale systems. As already mentioned the analogue performance of a single front-end channel will suffer from various parasitic effects in real multi-channel systems. These effects will be related mainly to the presence of parasitic feedback paths degrading the phase margin, as well as to the injection of noise and interference from the digital part of the circuit and other digital electronics implemented directly on the detector module. Two levels of optimisation can be made in order to ensure that the performance achieved with a single front-end channel is preserved after integration in a large system. The choice of a robust architecture, which is less sensitive to external pick-up, must go in parallel with properly designed and optimised layout of the chip. Improvement of the critical analogue parameters such as phase margin, increasing as much as possible the Power Supply Rejection Ratio (PSRR) and giving the possibility to adjust the biases (in order to improve to some extent the noise performance), will provide some safety margin for possible degradation of the performance of the circuit operating in a non-ideal environment with resistive power and ground lines, common bias lines and shared inductive bond connections.

5.1. Optimisation of the Power Supply Rejection Ratio

The choice of a single-ended architecture of the preamplifier stages employed in the chips presented in this thesis was the result of a strong requirement to minimize the power consumed by the front-end. This choice is however, by definition non-optimal from the standpoint of providing a good power supply rejection ratio parameter (PSRR). Nevertheless the PSRR still can be kept at a reasonable level if one pays attention to the sensitive points of the design, which are common bias lines, reference voltages and threshold lines for the comparators in the case of the binary architecture chip.

The use of a common biasing network in the case of multi-channel electronics is necessary from the viewpoint of minimisation of the number of control signals in the front-end chip. The bias line, which can be considered as an R-C network consisting of parasitic components and distributed over a whole chip, is in fact quite susceptible to the pick-up of signals from the digital part of the circuit. In order to minimise interference distributed through that path, one should use local decoupling of the bias line to the proper power supply node, made close to each load device (Cb1 to Cb4 capacitors in the schematics of the SCTA and ABCD front-end channels, Figure 4.1 and 4.21). The value of a single decoupling capacitor may vary from 100fF to a few picofarads depending in practice on the available layout space. Finally, for the entire bias line the total decoupling capacitance can reach several hundred picofarads.

During the layout design one should remember to correctly screen the bias lines in order not to create a capacitive divider degrading the PSRR. Typically as a screening layer in DMILL technology a GENPMOS layer, defining the area of the PMOS devices is used. Similarly to the BJT transistor, the PMOS device offers a low-resistive connection to the n+ buried layer, which can be used as a shield. Note that the screen or guard ring designed in this way can either be positively biased or grounded, since the oxide trenches provide DC isolation from the rest of the circuitry (see Figure 5.1). For decoupling of the bias lines to the ground, a p+ diffusion laid out over a unused silicon area may also be used as an effective screening layer (see Figure 5.1).

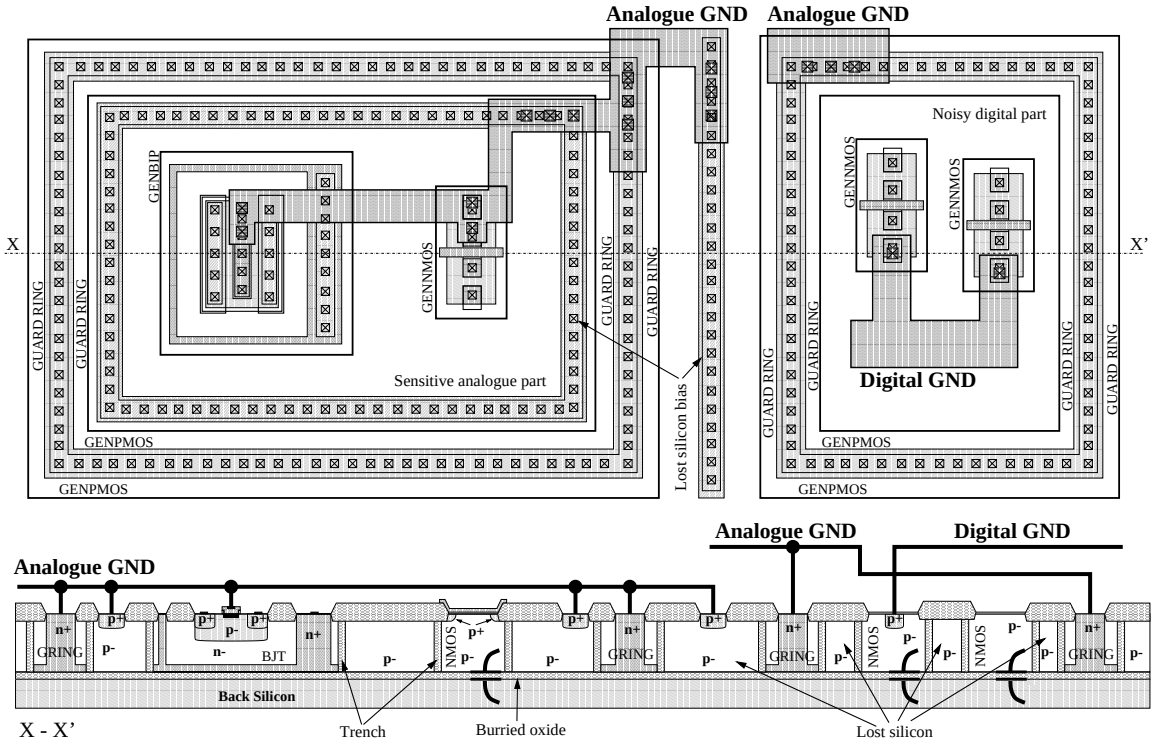


Figure 5.1: Layout and the cross-section of the guard ring structure in DMILL technology. As a guard ring a GENPMOS mask defining the PMOS devices and offering the n+ buried layer is used. The lost silicon area remaining after the definition of the trench-isolated devices is grounded using the p+ diffusion contacts.

The amplitude of the pick-up signals injected in a particular node of the circuit should always to be compared with the actual dynamic range of the readout signals. Therefore more attention, i.e. higher decoupling, should to be applied to the bias line controlling the load of the preamplifier input stage than to the bias lines in the remaining circuitry.

Although the cascode load stage has higher output impedance offering in principle better PSRR compared to the simple active load, its sensitivity to the interference seen from the bias node is practically the same. Consequently the same decoupling technique has to be applied (see schematic of the ABCDSFE chip, Figure 4.35). A similar approach using distributed decoupling capacitances is used to provide the voltage reference signal for the Analogue Delay Buffer in the SCTA chip.

The choice of the differential architecture for the discriminator in the ABCD chip was driven mainly by the matching issues. At the same time it also provides for that stage an good PSRR. The most sensitive lines distributing the threshold voltage for the comparator are routed differentially, employing also decoupling capacitors (capacitor *C4* in the schematic from Figure 4.21). Nevertheless, note that the PSRR of the whole chain is still limited by the input stage and, after applying all mentioned precautions, is in the range of –10 to 0dB for the centre frequency of the shaper (8 to 10MHz), which is roughly the same as for all the front-end circuits presented in this thesis. Towards the lower and higher frequencies the PSRR follows the noise filter characteristic achieving about 20dB attenuation for low and very high frequencies.

The PSRR parameter describes in principle the sensitivity of the chip itself to the interferences propagated through the power supplies. In order to obtain information about how the chip will operate in the real environment, one should also consider the PSRR of the front-end chip when it is connected to a silicon detector. As was already shown

(Figure 1.9) at least a part of the input capacitance representing the detector load is connected to the detector backplane i.e. common analogue ground of the module. Any interference appearing between the analogue ground of the module and the internal analogue ground of the chip connecting to the emitters of the input transistors (GND1 in Figures 4.1 and 4.21) will be amplified together with the detector signal.

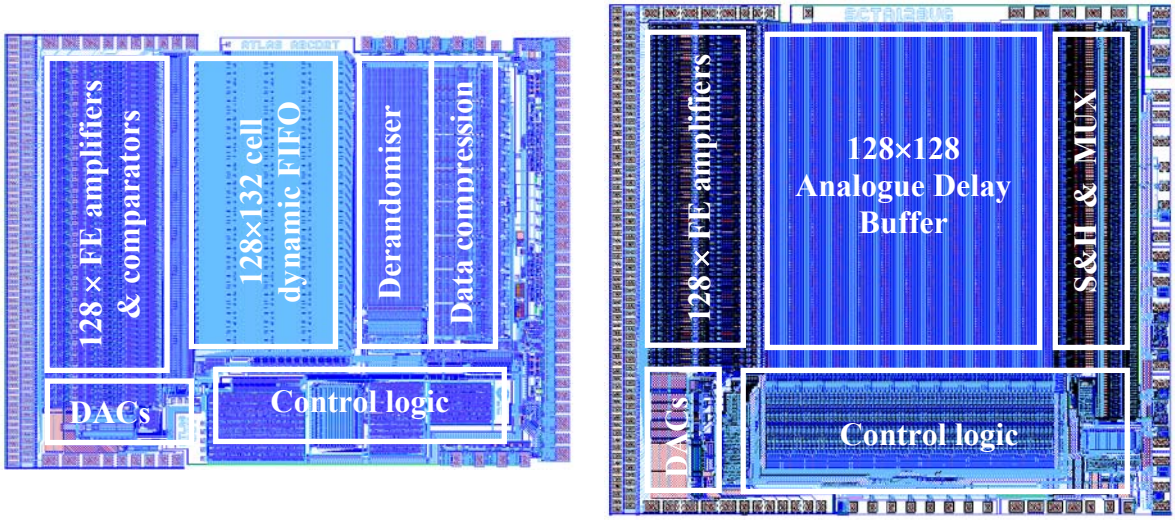
Ensuring a good, low impedance connection between the module's analogue ground and the chip's internal analogue ground is quite challenging, especially if one considers the geometrical dimensions of the hybrid (see Figure 1.2), the dimensions of the detectors and the number of front-end channels (1536 in case of the ABCD3T module for ATLAS SCT). In addition to the proper grounding scheme implemented on the detector module, a front-end chip must provide a low impedance connection from the emitters of the input transistors to the outside of the chip. In the SCTA as well as the ABCD chips the separate analogue ground line providing the connection only for the input transistors is distributed along the front-end channels using a 150μm-width top-metal stripe allowing double bond connections on each side of the chip. Separate, multiple bond connections provide a low impedance path to the external analogue ground, which is not disturbed by the supply currents of the following stages of the front-end, working with larger, amplified signals. One should stress that the problem of providing good quality connections between the ground referencing the silicon detector and the internal ground of the chip remains also in the case of using a fully differential structure for the preamplifier input stage, and it is related to the construction of the silicon strip detector which is intrinsically asymmetric.

5.2. Protection against interference from digital circuitry

The front-end ASICs for readout of silicon detectors at LHC experiments, represented here by the SCTA128VG and ABCD3T chips, are typical examples of mixed-mode circuits that integrate on the same substrate both sensitive analogue circuits and large digital blocks working nominally with a 40MHz clock.

Preventing cross-talk from the noisy digital part to the sensitive analogue front-end circuits is tackled at two levels. Improvement of the PSRR discussed already in the previous section must go hand-in-hand with the minimisation of the injection of digital noise to the chip substrate and good layout separation of the digital and analogue blocks. The use of low-level differential signals (LVDS standard) for the interfacing of the digital signals as well as separate power supply connections for analogue and digital blocks limits the injection of parasitic signals to the chip substrate and power lines suppling the sensitive analogue blocks.

Figure 5.2 (a) and (b) shows the layouts of the ABCD3T and SCTA128VG chips. The physical dimensions of the ABCD3T and SCTA128VG chips are respectively $8.4\times6.5\text{mm}^2$ and $8.8\times8.1\text{mm}^2$. The pure analogue circuits, front-end amplifiers and bias circuit including DACs and voltage references are grouped together and enclosed with a double guard ring structure, which is presented in Figure 5.1. A similar guard ring structure enclosing the digital blocks is connected with the separate bonding pad to the module analogue ground. The guard ring is created using the GENPMOS layer defining the PMOS devices and offering access to the low resistivity n+ buried layer. The "lost-silicon" area remaining after the definition of the trench-isolated active devices is connected using p+ diffusion contacts to the external analogue ground with a separate pad connection.



(a) (b)

Figure 5.2:Layouts of the ABCD3T chip (a) and SCTA128VG chip (b) showing the placement of the principal analogue and digital blocks.The physical dimensions of the ABCD and SCTA chips are respectively 8.4×6.5mm^2 and 8.8×8.1mm^2.

In case of the SCTA chip one can identify a third category of analogue blocks, which are designed using the switched capacitor technique, namely the Analogue Delay Buffer (ADB), the Sample-and-Hold circuit and the output multiplexer. These have an individual guard ring structure connected with separate pads to the external ground of the module.

Although the guard ring structure presented in Figure 5.1 effectively cancels parasitic coupling through the "lost silicon" on the surface of the chip, there is no way to stop the injection of the pick-up from the noisy digital part to the back silicon which acts as a mechanical substrate and is separated from the active epi-layer by the thin, 0.4µm thick buried oxide layer. DMILL technology, like any other SOI (Silicon On Oxide) process, does not offer connection to the mechanical substrate from the top of the chip and in addition does not provide metalisation of the wafer backside. Thinning and metalisation of the wafer backplane, which allows proper grounding of the wafer substrate, reduce significantly the effect of injection to the substrate.

During the development of the SCTA and ABCD families of chips, it has been found that the points of the designs that are most sensitive to parasitic injection are the input pads, which have for the nominal dimensions roughly 250fF parasitic capacitance to the back silicon volume (Figure 5.3, bonding pad A). A modified design of the pad (Figure 5.3, bonding pad B), which uses an n+ buried layer for screening and was accepted by the foundry as an alternative to the default pad structure, reduces the effect of substrate pick-up to a negligible level and allows for stable operation of the DMILL front-end chips without the need for backplane metalisation.

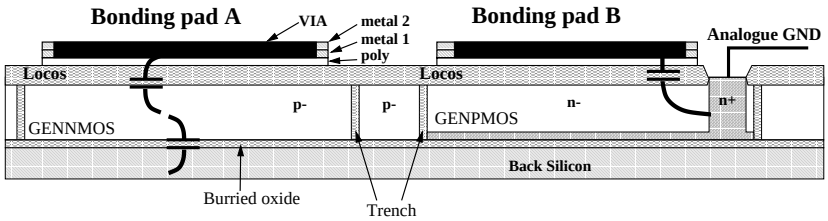


Figure 5.3: Cross-section of the original structure of the bonding pad in DMILL technology (bonding pad A) and the modified structure using the screening layer (bonding pad B).

5.5. Conclusions

The most critical point of the designs is the connection between the analogue ground of the input transistor and the reference ground of the detector. A low impedance path between these points must be provided by the front-end chips as well as by a properly designed hybrid holding the electronics and silicon detectors. Optimisation of the PSRR of the front-end electronics must go hand-in-hand with layout design providing a good separation between the noisy digital circuitry and the sensitive analogue part.

6. Performance of the Front End electronics on the detector modules

This chapter presents the performance of the detector modules built with the two final versions of the front-end ASICs implemented in radiation hard DMILL technology and representing the analogue and binary readout architectures, namely the SCTA128VG and ABCD3T chips respectively. The general architecture and the main applications of both designs were discussed already in the first chapter. The architecture and the analogue performance of the single front-end channels were presented in detail in Chapter 4. In this chapter the performance of the fully populated, multi-channel detector modules working in the real conditions of the experiments is discussed.

6.1. Performance of the SCTA128VG chip working on detector modules

In the case of the analogue readout architecture implemented in the SCTA128VG chip, in addition to the excess noise caused by the digital activity which is propagated through the power supply, bias lines and by the chip substrate, another possible source of excess noise is the non-uniformity of the analogue memory (ADB). One of the most important parameters of the ADB, which will define its contribution to the overall noise performance of the chip, is the uniformity of the DC offsets (pedestals) between memory cells.

The analogue memory employed in the SCTA chip consists of a 128×128 matrix of capacitors sampling the output of the front-end amplifier with a 40MHz clock, storing the analogue data for the trigger latency time and finally being readout by the charge sensitive amplifier. The pedestal spread is mainly caused by the non-uniformity of the parasitic charge injection from the control lines (read and write signals) to the storage capacitors via the NMOS switches.

Minimisation of the injected charge by proper sizing of the storage capacitors and the NMOS switches must go in parallel with the optimum layout design providing best possible matching of the devices as well as high uniformity of the signals controlling the switches. The mean value of the injected signal from the write line in the case of the SCTA128VG memory cell is in the range of 120 to 150mV i.e. much higher than 1fC signal amplitude, while its non-uniformity determining the pedestal dispersion is about two orders of magnitude lower.

Figure 6.4 shows the pedestal map of 128x128 ADB cells in one chip. From this figure one can extract the cell-to-cell variation of the ADB pedestals across all channels of the chip. The distribution of the ADB pedestal spreads for all channels in one particular chip is shown in Figure 6.5. The 1.1mV mean value of the distribution is equivalent to 150e- ENC of extra, non-correlated contribution to the noise generated by the front-end. For a low value of the input current and a low detector capacitance the additional contribution is about 4%. For higher detector capacitance this contribution becomes negligible. It can be seen that the high channel-to-channel uniformity of the analogue memory is confirmed by the narrow (rms ~ 10%) distribution of the pedestal spreads (Figure 6.5).

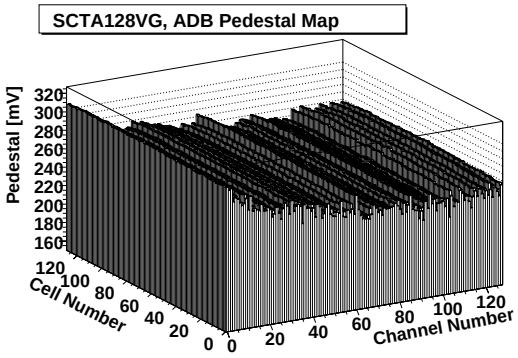


Figure 6.4: ADB pedestal map in one SCTA chip.

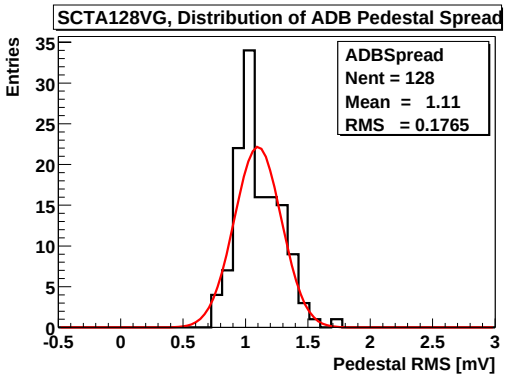


Figure 6.5: Distribution of ADB pedestal spread in each channel, in one SCTA128VG chip. The 1.1mV mean value of the distribution is equivalent to 150e- ENC.

To demonstrate the performance of the SCTA128VG chip reading out long silicon strip detectors, several modules equipped with 12.8cm ATLAS SCT type sensors have been built. A 6-chip ceramic hybrid holding two silicon detectors of size 6.3 x 6.4cm is shown in Figure 6.4.

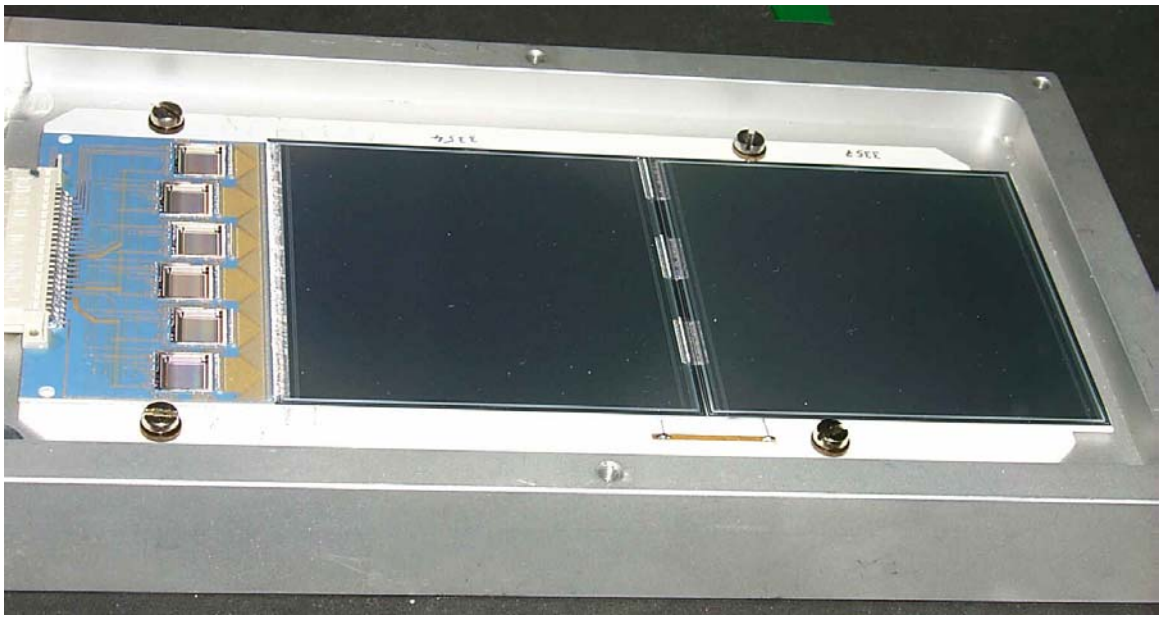


Figure 6.6: Photograph of a 6-chip, 12.8cm strip silicon detector module of the ATLAS type.

The noise performance of the SCTA128VG chip can be optimised according to the detector capacitance by adjustment of the current in the input transistor. Figure 6.7 shows the results of noise measurements of one module with SCTA chips connected to 6.5 and 13cm long silicon strip detectors. The measurement has been made for various bias conditions of the input transistor. Note that the noise performance of the chip connected to 13cm strips could be improved by increasing the bias current of the input transistor. The reduction of ENC is relatively smaller for high currents since the noise of the base spread resistance and the noise of the equivalent strip resistance[1], which for the 13cm

[1] The resistance of the strips in ATLAS SCT detectors is roughly 10 to 12Ω/cm, which for 13cm length strips gives a total resistance in the range of 130 to 160Ω. The analysis presented in [5.4] considering the

end-tap detector module is in the range of 35 to 50Ω, become limiting factors. Figure 6.8 shows a Signal-over-Noise distribution of data taken in a 100GeV pion beam with the SCTA chip connected to a 13cm long and 280µm thick silicon strip detector. The SCTA128VG chip was operated under nominal bias conditions with input transistor current set to 200µA. The ENC of 1850e- extracted from Figure 6.8 has to be compared with an ENC of 1700e- measured with the internal calibration circuit. The difference may be explained by the ballistic deficit and charge loss due to the inter-strip capacitances of the detector.

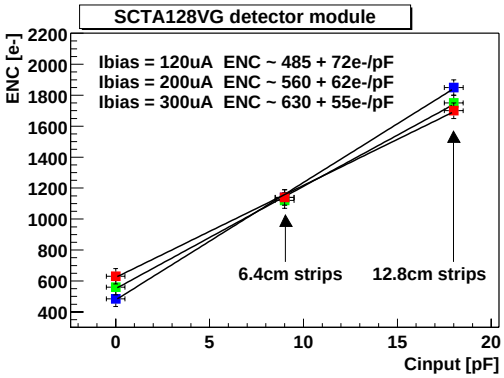


Figure 6.7: ENC for SCTA128VG chips connected to various length silicon strip detectors.

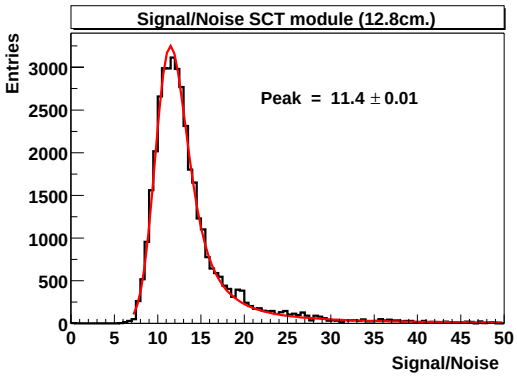


Figure 6.8: Signal over Noise histogram from data taken with a 100GeV pion beam for the 13cm detector module. Measurements were made for 200µA input transistor current.

As already mentioned the SCTA128VG chip is presently used in the NA60 experiment at CERN. The performance of the Silicon Microstrip Telescope employing the SCTA chips is reported in an NA60 status report [5.2]. The performance of the SCTA128VG chip working with diamond detectors is presented in an RD42 status report [5.3].

6.2. Performance of the detector modules equipped with the ABCD3T chips

As already mentioned, the main application of the ABCD3T chip is the readout of silicon strip detectors in the ATLAS SemiConductor Tracker (SCT). The example of the module intended to be used in the barrel part of the SCT has been presented in Figure 1.2. This module consists of four 6.4×6.4cm p-on-n+ silicon strip sensors, two daisy-chained per module side, readout in total by twelve ABCD3T chips. The total capacitance of the daisy-chained detector loading one input of the front-end channel is in the range of 18pF before the irradiation. The equivalent strip resistance contributing to the noise of the front-end amplifier is in the range of 8 to 12Ω [5.4], and fully explains the differences between noise performance of the ABCD3T barrel module (center-tap configuration) and SCTA128VG end-tap module, which uses the same type of silicon sensors (compare ENC extracted from Figure 6.7 for 18pF input capacitance and ENC from Figure 6.9 measured for the same detector connected in the center-tap configuration). A detailed description of the construction and performance of the detector modules for the ATLAS SCT, covering issues regarding the electrical performance of the ABCD chip connected

strip detector as a distributed RC transmission line shows that only a part of that resistance will contribute to the noise of the front-end amplifier.

to the strip detector as well as the mechanical and thermal properties of the final object, can be found in [5.1].

The average noise of the detector module operating at room temperature with nominal 250μA bias current of the input transistor is in the range of 1500e-. The ENC for each individual channel of the ABCD3T module is shown in Figure 6.9. A uniform noise distribution is seen, except for one channel on the module, which is connected only to a 6 cm length of sensor. At the operating temperature of the module in the experiment, which is close to 0°C, the noise is in the range of 1350e-, which corresponds to a Signal-to Noise ratio of about 14.

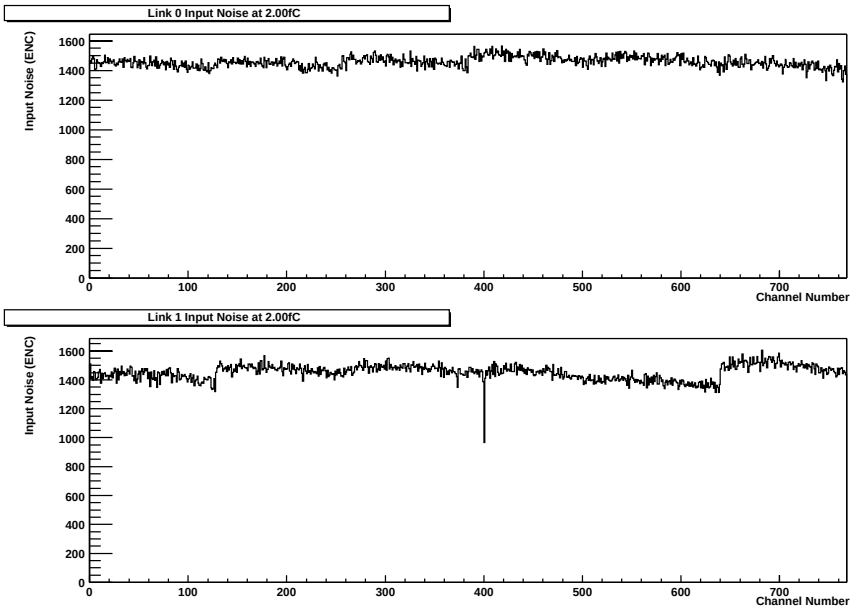


Figure 6.9: Measured ENC values on all channels of ABCD3T module (top and bottom side).

As already shown, the single detector modules meet the requirements in terms of analogue performance and they also demonstrate good electrical stability and a negligible level of excess noise. In order to test the performance of the detector modules in the configuration similar to the planned ATLAS tracker, a system test including several ABCD3T modules working together has been assembled and used to study potential degradation of the module performance as well as to investigate different schemes for the grounding and shielding.

Figure 6.10 shows a photograph of nine barrel modules mounted on a sector prototype of the carbon-fibre cylinder with dimensions close to the innermost layer of ATLAS SCT. Modules are powered and readout via prototype power tapes and optical-links designed for the final SCT detector system.

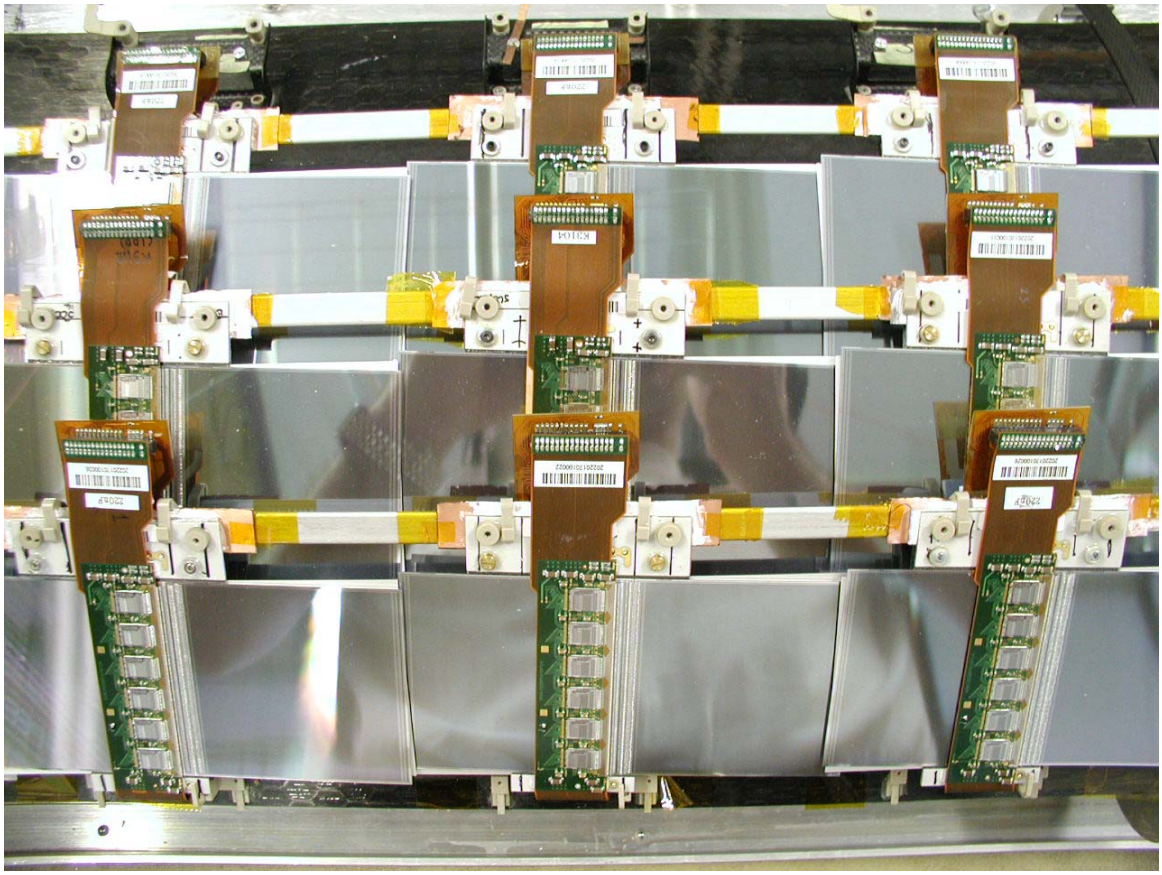


Figure 6.10: Photograph of nine barrel modules mounted on the carbon-fibre structure for a system test.

Figure 6.11 shows the noise performance of ten detector modules operating together on the sector compared to the noise of a stand-alone module measured on the single-module test bench. With the exception of module 0008, which already shows worse performance in the single module test setup, the noise levels of modules operating on the sector are in the expected range. The differences in noise levels between the single module setup and the system test setup are typically in the range of ±50e- ENC (see Figure 6.12).

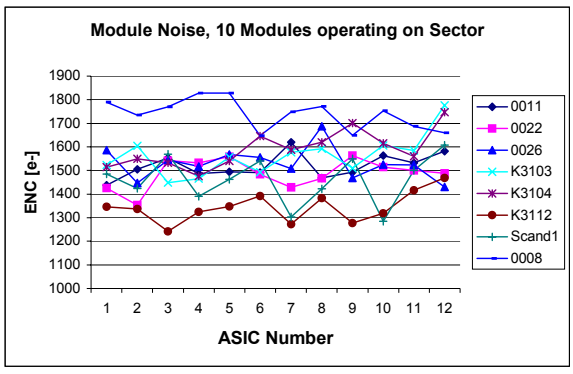


Figure 6.11: The average ENC for each ABCD3T chip with 10 modules operating together on the barrel system test sector.

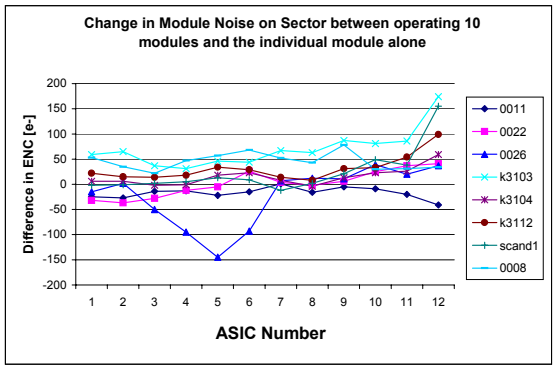


Figure 6.12: Change in the ENC between the set up operating 10 modules together and the operation of a stand-alone module.

6.3. Conclusions

Using the techniques described in the previous chapter, optimising chip layout as well as hybrid design, it was possible to preserve the original parameters of the front-end electronics chips when they are integrated on the detector modules; there is no significant degradation of the analogue performance and electrical stability. All differences in the noise performance between pure capacitive loading and the case of the electronics connected to the silicon strip detectors could be explained by the contribution of the strip resistance as well as by injection of noise from the neighbouring front-end channels via detector inter-strip capacitances [5.5].

Summary and future prospects

This thesis describes the development of a fast, radiation-hard Front End electronics for readout of Silicon Strip Detectors (SSD) to be used in the experiments built at the LHC machine. It discusses in detail the design methodology used, taking into account all requirements for the analogue performance such as speed and noise figures, radiation hardness and power consumption, as well as aspects related to the mixed-mode operation of the complete front-end chips.

Although the final versions of the front-end chips presented in my thesis have been implemented in a particular radiation-hard BiCMOS DMILL process, the whole analysis concerning the design of the preamplifier stage and the noise optimisation of the amplifier-shaper circuit is applicable for designs implemented in any bipolar or CMOS technology.

The harsh radiation environment of the LHC experiments together with the demanding requirements for analogue performance and low power consumption are the driving issues for technology and architecture of the Front End electronics. As shown in Chapter 3, for the CMOS technologies available in 1998, the noise and power consumption figures as well as achievable gain-bandwidth product for the preamplifier were not adequate for the planned Front End electronics. The natural choice, available since 1995, was the BiCMOS DMILL technology qualified by the foundry for the radiation doses required by the LHC experiments.

The ABCD3T and SCTA128VG chips implemented in DMILL technology and using bipolar transistors as input device meet all requirements for radiation hard Front End electronics for silicon strip detectors at LHC. This is discussed extensively in Chapter 4 and 6. The needs of various users for the SCTA128VG chips are covered by the engineering run processed in 2001. The production of roughly 1000 wafers with the ABCD3T chips for the ATLAS Semiconductor Tracker readout was completed in 2002.

As shown in Chapter 4 for the ABCDS-FE chip implemented in IBM CMOS 0.25µm process, the new submicron technologies offer satisfactory performance in terms of speed, noise figure and radiation hardness (achieved by using enclosed geometry layout for the NMOS transistors) of the Front End electronics for SSD, but at the expenses of the current supplied to the input device. Although the higher current consumption of the submicron design is compensated by the lower supply voltage keeping the power consumption at a similar level compared to the bipolar circuit, for some system aspects it is still a significant disadvantage. The gain-bandwidth product obtained in the IBM-0.25 CMOS preamplifier is close to, but still lower by about 20%, the bipolar DMILL implementations.

Nevertheless, bearing in mind the closure of the DMILL production line at the end of 2003, the use of CMOS deep submicron technologies is the only approach available for future developments that must provide excellent radiation hardness together with satisfactory analogue performance for the readout electronics of silicon strip detectors. For the applications requiring high speed, when the noise versus power consumption figure is critical and the radiation hardness of the design is not mandatory, a better solution will be to use a standard BiCMOS process offering both bipolar and MOS devices.

7. Appendix

7.1. Calculation of the output noise for the bipolar transresistance preamplifier

Considering that the circuit is linear one can identify the contributions to the output noise from each source separately. Initially all quantities could be described in the time domain. In order to simplify the calculations the gain of the amplifier is assumed to be constant. That assumption is justified by the further processing of the signal and noise, namely filtering the frequencies outside the amplifier bandwidth.

7.1.1. Analysis of the noise generated by the base spread resistance $r_{bb'}$

The equivalent schematic of the preamplifier built with BJT including the voltage noise source v_{nb} which represents the thermal noise of $r_{bb'}$ is shown in Figure 7.1. The value of the $r_{bb'}$, which is much smaller in comparison to the input impedance of the bipolar transistor $Z_e=1/Y_e$, is not taken into account for calculating the sharing of the generated noise between the detector impedance Z_d and transistor input impedance Z_e.

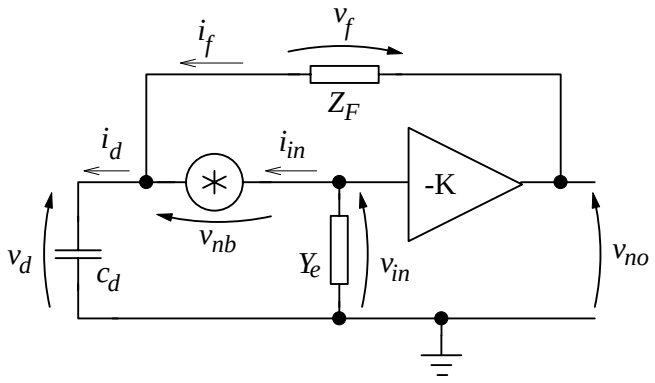


Figure 7.1: Equivalent schematic of the preamplifier including the feedback components and the $r_{bb'}$ noise source.

Summing the currents at the preamplifier input and voltages in the presented circuit one can write the following set of equations.

$$i_{in}(t)+i_f(t)=i_d(t) \quad \text{where} \quad i_{in}(t)=-v_{in}(t)\cdot Y_e \quad i_d(t)=v_d(t)\cdot Y_d \quad i_f(t)=v_f(t)\cdot Y_F \tag{7.1}$$

$$\text{where} \qquad Y_d=\frac{1}{Z_d}=j\cdot\omega\cdot c_d \quad \text{and} \quad Y_F=\frac{1}{Z_F} \tag{7.2}$$

$$v_d(t)=v_{nb}(t)+v_{in}(t) \tag{7.3}$$

$$v_{no}(t)=v_d(t)+v_f(t) \tag{7.4}$$

$$v_{no}(t)=-K\cdot v_{in}(t) \tag{7.5}$$

Solving equation (7.1) and replacing v_d and v_f by the terms extracted from equations (7.3) to (7.5) one obtains:

$$v_{no}(t)\cdot\left(Y_F+\frac{Y_e}{K}+\frac{Y_d}{K}+\frac{Y_F}{K}\right)=v_{nb}(t)\cdot(Y_F+Y_d) \tag{7.6}$$

Assuming sufficient gain and high bandwidth of the input stage i.e. K>>1, the equation (7.6) can be simplified to:

$$v_{no}(t)=v_{nb}(t)\cdot Z_F\cdot(Y_d+Y_F) \tag{7.7}$$

7.1.2. Propagation of collector current shot noise to the preamplifier output

The equivalent schematic of the preamplifier including the detector impedance Z_d, the feedback circuit represented by the impedance Z_F and the input impedance of the bipolar transistor $Z_e=1/Y_e$ is shown in Figure 7.2. The equivalent voltage noise source v_{nc} represents the collector current shot noise transferred to the preamplifier input in accordance with the transconductance of the input transistor.

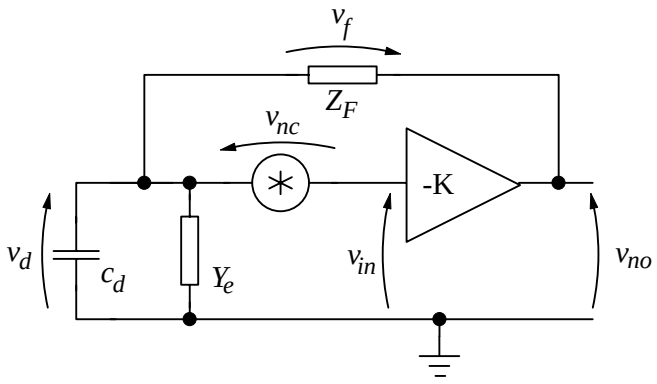


Figure 7.2: Equivalent schematic of the preamplifier including the feedback components and the collector current shot noise source transferred to the preamplifier input.

Making a sum of voltages at the preamplifier input as well as for the whole circuit enclosed with the feedback impedance Z_F one can write the following set of equations:

$$v_{nc}(t)+v_{in}(t)=v_d(t) \tag{7.8}$$

$$v_d(t)+v_f(t)=v_{no}(t) \tag{7.9}$$

$$v_d(t)\cdot(Y_d+Y_e)=v_f(t)\cdot Y_F \tag{7.10}$$

$$v_{no}(t)=-K\cdot v_{in}(t) \tag{7.11}$$

By making simple calculations one can obtain the following:

$$v_{no}(t)\cdot\left(Y_F+\frac{Y_F}{K}+\frac{Y_e}{K}+\frac{Y_d}{K}\right)=v_{nc}(t)\cdot(Y_F+Y_e+Y_d) \tag{7.12}$$

Assuming sufficient open loop gain (K>>1) one can simplify equation (7.12) to:

$$v_{no}(t)=v_{nc}(t)\cdot Z_F\cdot(Y_F+Y_e+Y_d) \tag{7.13}$$

Since the equivalent voltage noise source v_{nc} could be denoted also as $i_2(t)/g_m$, where g_m stands for transconductance of the input transistor, the equation (7.13) can be written also as:

$$v_{no}(t)=\frac{i_2(t)}{g_m}\cdot Z_F\cdot(Y_F+Y_e+Y_d) \tag{7.14}$$

7.1.3. Impact of base current shot noise on the preamplifier output noise

The equivalent schematic of the preamplifier responding to the current base shot noise represented by the current source i_b is shown in Figure 7.3. The noise at the preamplifier output caused by the shot noise of the base current can be calculated as follows.

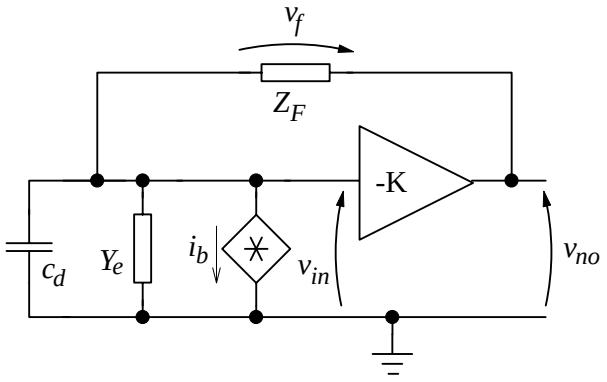


Figure 7.3: Equivalent schematic of the preamplifier including the feedback components and the base current shot noise source.

$$v_{no}(t)=v_f(t)+v_{in}(t) \tag{7.15}$$

$$i_b(t)+v_{in}(t)\cdot(Y_d+Y_e)=v_f(t)\cdot Y_F \tag{7.16}$$

$$v_{no}(t)=-K\cdot v_{in}(t) \tag{7.17}$$

Solving the above equations leads to the following:

$$i_b(t)=v_{no}(t)\cdot\left(Y_F+\frac{Y_F}{K}+\frac{Y_d}{K}+\frac{Y_e}{K}\right) \tag{7.18}$$

Assuming sufficient gain and bandwidth of the preamplifier (K>>1) one finds that the final value of the preamplifier output noise generated by the base current shot noise is given by:

$$v_{no}(t)=i_b(t)\cdot Z_F \tag{7.19}$$

7.2. Fourier analysis of the output noise of the bipolar preamplifier

The noise at the preamplifier output described in the time domain is given by the following equation (3.18).

$$v_{no}(t)=v_{no\_rbb}(t)+v_{no\_i2}(t)+v_{no\_ib}(t) \tag{7.20}$$

The elementary voltage noise sources from expression (7.20) are described by equations (3.15), (3.16) and (3.17).

One can assume that $v_{nb}(t)$, $i_2(t)$, $i_b(t)$ and $v_{no}(t)$ have the following Fourier series representations:

$$v_{nb}(t)=\sum_{n=-\infty}^{\infty}a_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.21}$$

$$i_2(t)=\sum_{n=-\infty}^{\infty}b_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.22}$$

$$i_b(t)=\sum_{n=-\infty}^{\infty}c_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.23}$$

$$v_{no}(t)=\sum_{n=-\infty}^{\infty}d_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.24}$$

Note that we redefine in this way the spectral densities of the noise sources and cross-correlation term shown before in equations (3.2), (3.6), (3.13) and (3.14):

$$\overline{v_{nb}^2}=4\cdot k\cdot T\cdot r_{bb'}\,\Delta f=\overline{a_n\cdot a_n^*}\Delta f \tag{7.25}$$

$$\overline{i_2^2}=2\cdot q\cdot I_C\Delta f=\overline{b_n\cdot b_n^*}\Delta f \tag{7.26}$$

$$\overline{i_b^2}=2\cdot q\cdot\frac{I_C}{\beta}\Delta f=\overline{c_n\cdot c_n^*}\Delta f \tag{7.27}$$

$$\overline{i_b^* i_2}=2\cdot k\cdot T\cdot(-j\cdot\omega\cdot c_c)\Delta f=\overline{b_n\cdot c_n^*}\Delta f \tag{7.28}$$

Using the Fourier representations of the noise quantities for equation (7.20) one can find the following:

$$d_n=a_n\cdot Z_{\mathrm{F}}\cdot(Y_d+Y_F)+b_n\cdot\frac{Z_F}{g_m}\cdot(Y_d+Y_e+Y_F)+c_n\cdot Z_F \tag{7.29}$$

where: (7.30)

$$Z_F=\frac{1}{Y_F}=\frac{R_F}{1+j\cdot\omega\cdot\tau_f},\ Z_e=\frac{1}{Y_e}=\frac{r_e}{1+j\cdot\omega\cdot r_e\cdot c_e},\ r_e=\frac{\beta}{g_m},\ Z_d=\frac{1}{Y_d}=\frac{1}{j\cdot\omega\cdot c_d},\ \tau_f=R_F\cdot C_F$$

For better transparency one can define the following admittances:

$$Y_{DF}=Y_d+Y_F \quad\text{and}\quad Y_T=Y_d+Y_e+Y_F \tag{7.31}$$

Therefore the spectral density of the output noise is as follows:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{d_n\cdot d_n^*}=\overline{\left(a_n\cdot Z_F\cdot Y_{DF}+b_n\cdot\frac{Z_F}{g_m}\cdot Y_T+c_n\cdot Z_F\right)\cdot\left(a_n^*\cdot Z_F^*\cdot Y_{DF}^*+b_n^*\cdot\frac{Z_F^*}{g_m}\cdot Y_T^*+c_n^*\cdot Z_F^*\right)} \tag{7.32}$$

Taking into account the spectral densities of the noise sources and cross-correlation term $\overline{i_b^* i_2}$ only, one obtains (7.33):

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{a_n\cdot a_n^*}\cdot|Z_F|^2\cdot|Y_{DF}|^2+\overline{b_n\cdot b_n^*}\cdot\frac{|Z_F|^2}{g_m^2}\cdot|Y_T|^2+\overline{c_n\cdot c_n^*}\cdot|Z_F|^2-2\cdot\mathrm{Im}\left[\overline{b_n\cdot c_n^*}\right]\cdot\frac{|Z_F|^2}{g_m}\cdot\omega\cdot(c_e+c_d+C_F)$$

Where $\mathrm{Im}\left[\overline{b_n\cdot c_n^*}\right]$ stands for imaginary part of $\overline{b_n\cdot c_n^*}$

Replacing the Z_F, Z_e, Z_d, Y_{DF} and Y_T with its definitions from equation (7.30), (7.31) and using equations (7.25) to (7.28) to find spectral densities for the Fourier series representation and the imaginary part of $\overline{i_b^* i_2}$, one can derive the following expression for the spectral density of the output noise:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\frac{\overline{v_{no\_rbb}^2}}{\Delta f}+\frac{\overline{v_{no\_i2}^2}}{\Delta f}+\frac{\overline{v_{no\_ib}^2}}{\Delta f}+\frac{\overline{v_{no\_corr}^2}}{\Delta f} \tag{7.34}$$

Where the noise spectral densities related to the thermal noise of the r_{bb}', shot noise of the collector and base currents, as well as to the correlation term are described by the following equations:

$$\frac{\overline{v_{no\_rbb}^2}}{\Delta f}=4\cdot k\cdot T\cdot r_{bb'}\cdot\left(\omega^2\cdot(c_d+C_F)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.35}$$

$$\frac{\overline{v_{no\_i2}^2}}{\Delta f}=\frac{2\cdot q\cdot I_C}{g_m^2}\cdot\left(\omega^2\cdot(c_d+c_e+C_F)^2+\left(\frac{g_m}{\beta}+\frac{1}{R_F}\right)^2\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.36}$$

$$\frac{\overline{v_{no\_ib}^2}}{\Delta f}=2\cdot q\cdot\frac{I_C}{\beta}\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.37}$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f}=\frac{4\cdot k\cdot T}{g_m}\cdot\omega^2\cdot(c_d+c_e+C_F)\cdot c_c\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.38}$$

Using the expression (3.4) describing the transconductance of the bipolar device, the equation (7.36) can therefore be transformed to:

$$\frac{\overline{v_{no\_i2}^2}}{\Delta f}=\frac{2\cdot k\cdot T}{g_m}\cdot\left(\omega^2\cdot(c_d+c_e+C_F)^2+\left(\frac{g_m}{\beta}+\frac{1}{R_F}\right)^2\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.39}$$

The collector current shot noise is often denoted as an equivalent series voltage noise source transferred to the amplifier input with the spectral density equal to $2kT/g_m$. The equivalent series noise resistance R_{neq} is therefore described as follows:

$$R_{neq}=\frac{1}{2\cdot g_m} \tag{7.40}$$

7.3. Calculation of the output noise for the MOS preamplifier stage

As in the case of the bipolar preamplifier one can calculated all contributions to the output noise separately and then add them quadratically. The method works well under

the assumptions that the circuit is linear, which is the case for the expected range of the noise level. All noise quantities are considered in the time domain.

7.3.1. Propagation of channel thermal noise

The schematic model of the amplifier built with MOS devices including the equivalent series voltage noise source related to the channel thermal noise is shown in Figure 7.4. The spectral density of the equivalent series noise v_{nt} can be obtained from the spectral density of the current noise generator representing the thermal noise in the model (see Figure 3.21) divided by the transconductance of the device.

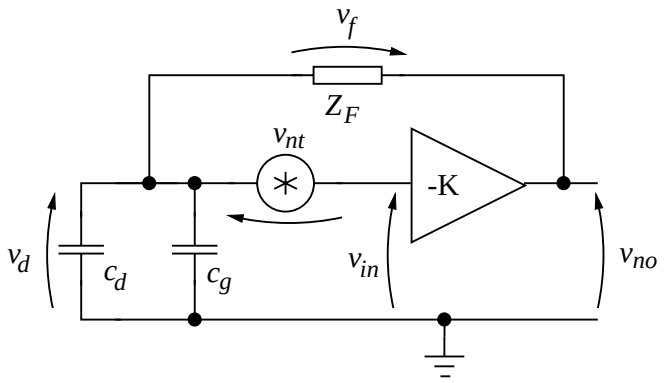


Figure 7.4: Equivalent schematic of the preamplifier including the feedback components and the equivalent channel thermal noise source.

For sufficient open loop gain and amplifier bandwidth one can write the following set of equations:

$$v_{nt}(t)+v_{in}(t)=v_d(t) \tag{7.41}$$

$$v_d(t)+v_f(t)=v_{no}(t) \tag{7.42}$$

$$v_d(t)\cdot(Y_d+Y_g)=v_f(t)\cdot Y_F \tag{7.43}$$

$$v_{no}(t)=-K\cdot v_{in}(t) \tag{7.44}$$

where $Y_d = j\omega c_d$ stands for the detector admittance, $Y_g = j\omega c_g$ and $Y_F = 1/Z_F$.

Making simple calculations one can obtain the following:

$$v_{no}(t)\cdot\left(Y_F+\frac{Y_F}{K}+\frac{Y_g}{K}+\frac{Y_d}{K}\right)=v_{nt}(t)\cdot(Y_F+Y_g+Y_d) \tag{7.45}$$

Assuming sufficient open loop gain (K>>1) one can simplify equation (7.45) to:

$$v_{no}(t)=v_{nt}(t)\cdot Z_F\cdot(Y_F+Y_g+Y_d) \tag{7.46}$$

Since the equivalent voltage noise source v_{nt} could be denoted also as $i_{nd}(t)/g_m$, where g_m stands for transconductance of the input transistor, the equation (7.46) for the channel thermal noise can also be written as:

$$v_{no}(t)=\frac{i_{nd}(t)}{g_m}\cdot Z_F\cdot(Y_F+Y_g+Y_d) \tag{7.47}$$

The flicker noise current generator is placed in the noise model from Figure 3.21 exactly in the same location as the thermal channel noise source. Therefore it propagates to the preamplifier output in the same proportion as thermal noise of the channel. Consequently one can write the following equation describing the output noise of the preamplifier originating from the flicker noise:

$$v_{no\_1f}(t)=\frac{i_{nf}(t)}{g_m}\cdot Z_F\cdot\left(Y_F+Y_g+Y_d\right) \tag{7.48}$$

7.3.2. Effect of the GIC noise at the preamplifier output

The schematic diagram of the preamplifier including GIC current noise generator is shown in Figure 7.5. The set of equations and the final solutions are basically the same as in the case of base current shot noise in the bipolar preamplifier.

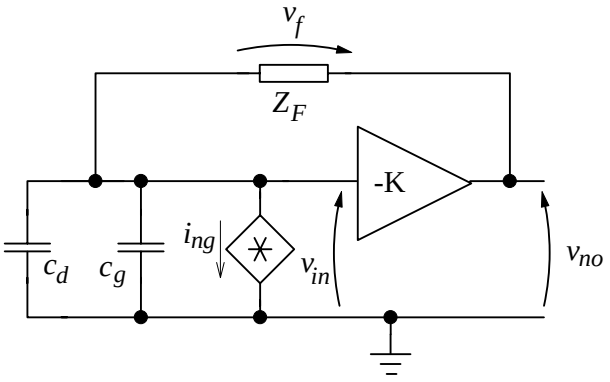


Figure 7.5: Equivalent schematic of the preamplifier including the feedback components and the GIC current noise generator.

$$v_{no}(t)=v_f(t)+v_{in}(t) \tag{7.49}$$

$$i_{ng}(t)+v_{in}(t)\cdot\left(Y_d+Y_g\right)=v_f(t)\cdot Y_F \tag{7.50}$$

$$v_{no}(t)=-K\cdot v_{in}(t) \tag{7.51}$$

where $Y_d=j\omega c_d$ stands for the detector admittance, $Y_g=j\omega c_g$ and $Y_F=1/Z_F$.

Solving the above equations leads to the following:

$$i_{ng}(t)=v_{no}(t)\cdot\left(Y_F+\frac{Y_F}{K}+\frac{Y_d}{K}+\frac{Y_g}{K}\right) \tag{7.52}$$

Assuming sufficient gain and bandwidth of the preamplifier ($K>>1$) one can find that the final value of the preamplifier output noise generated by the base current shot noise is:

$$v_{no}(t)=i_{ng}(t)\cdot Z_F \tag{7.53}$$

7.4. Fourier analysis of the output noise of the MOS preamplifier

The noise at the preamplifier output described in the time domain is given by the following equation (3.58).

$$v_{no}(t)=v_{no\_ind}(t)+v_{no\_GIC}(t)+v_{no\_f}(t) \tag{7.54}$$

One can assume the following Fourier series representation of the noise quantities:

$$i_{nd}(t)=\sum_{n=-\infty}^{\infty}a_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.55}$$

$$i_{ng}(t)=\sum_{n=-\infty}^{\infty}b_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.56}$$

$$i_{nf}(t)=\sum_{n=-\infty}^{\infty}c_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.57}$$

$$v_{no}(t)=\sum_{n=-\infty}^{\infty}d_n\cdot\exp(j\cdot\omega\cdot t) \tag{7.58}$$

Therefore the spectral densities of the noise generators and correlation term described in equations (3.46), (3.48), (3.49) and (3.51) will look as follows:

$$\overline{i_{nd}^2}=4\cdot k\cdot T\cdot\gamma\cdot n\cdot g_m\Delta f=\overline{a_n\cdot a_n^*}\Delta f \tag{7.59}$$

$$\overline{i_{ng}^2}=\frac{32}{45}\cdot k\cdot T\cdot\gamma\cdot\frac{\omega^2\cdot C_{OX}^2}{n\cdot g_m}\Delta f=\overline{b_n\cdot b_n^*}\,\Delta f \tag{7.60}$$

$$\overline{i_{nf}^2}=\frac{K_a}{f}\cdot\frac{g_m^2}{C_{OXU}^2\cdot W\cdot L}\Delta f=\overline{c_n\cdot c_n^*}\,\Delta f \tag{7.61}$$

$$\overline{i_{ng}\cdot i_{nd}^*}=\frac{\gamma}{6}\cdot j\cdot\omega\cdot C_{OX}\cdot 4\cdot k\cdot T\,\Delta f=\overline{b_n\cdot a_n^*}\,\Delta f \tag{7.62}$$

Using equation (7.54) one can find the following dependence for the *"n"* Fourier series term:

$$d_n=a_n\cdot\frac{Z_F}{g_m}\cdot Y_T+b_n\cdot Z_F+c_n\cdot\frac{Z_F}{g_m}\cdot Y_T \tag{7.63}$$

For better transparency the sum of admittances Y_d, Y_F and Y_g was replaced by the total admittance Y_T.

Consequently one can describe the spectral density of the output noise by (7.64):

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{d_n\cdot d_n^*}=\overline{\left(a_n\cdot\frac{Z_F}{g_m}\cdot Y_T+b_n\cdot Z_F+c_n\cdot\frac{Z_F}{g_m}\cdot Y_T\right)\cdot\left(a_n^*\cdot\frac{Z_F^*}{g_m}\cdot Y_T^*+b_n^*\cdot Z_F^*+c_n^*\cdot\frac{Z_F^*}{g_m}\cdot Y_T^*\right)}$$

Taking into account a non-zero correlation term between thermal channel noise and GIC noise and replacing the term related to spectral densities by its definitions one obtains the following expression for the spectral density of the output noise (7.65):

$$\frac{\overline{v_{no}^2}}{\Delta f}=\overline{a_n\cdot a_n^*}\cdot\frac{|Z_F|^2}{g_m^2}\cdot|Y_T|^2+\overline{b_n\cdot b_n^*}\cdot|Z_F|^2+\overline{c_n\cdot c_n^*}\cdot\frac{|Z_F|^2}{g_m^2}\cdot|Y_T|^2+2\cdot\mathrm{Im}\left[\overline{b_n\cdot a_n^*}\right]\cdot\frac{|Z_F|^2}{g_m}\cdot\omega\cdot\left(c_d+c_g+C_F\right)$$

And consequently:

$$\frac{\overline{v_{no}^2}}{\Delta f}=\frac{\overline{v_{no\_id}^2}}{\Delta f}+\frac{\overline{v_{no\_GIC}^2}}{\Delta f}+\frac{\overline{v_{no\_f}^2}}{\Delta f}+\frac{\overline{v_{no\_corr}^2}}{\Delta f} \tag{7.66}$$

The noise spectra densities related to each noise source are defined by the following equations:

$$\frac{\overline{v_{no\_id}^2}}{\Delta f}=\frac{4\cdot k\cdot T\cdot\gamma\cdot n}{g_m}\cdot\left(\omega^2\cdot\left(c_d+c_g+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.67}$$

$$\frac{\overline{v_{no\_GIC}^2}}{\Delta f}=\frac{32}{45}\cdot k\cdot T\cdot\gamma\cdot\frac{\omega^2\cdot C_{OX}^2}{n\cdot g_m}\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.68}$$

$$\frac{\overline{v_{no\_f}^2}}{\Delta f}=\frac{K_a}{f\cdot C_{OXU}^2\cdot W\cdot L}\cdot\left(\omega^2\cdot\left(c_d+c_g+C_F\right)^2+\frac{1}{R_F^2}\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.69}$$

$$\frac{\overline{v_{no\_corr}^2}}{\Delta f}=\frac{8}{6}\cdot\frac{\gamma\cdot k\cdot T}{g_m}\cdot\omega^2\cdot C_{OX}\cdot\left(c_d+c_g+C_F\right)\cdot\frac{R_F^2}{1+\tau_f^2\cdot\omega^2} \tag{7.70}$$

The feedback time constant τ_f was defined in equation (3.54).

7.5. Measurement of $r_{bb'}$ base spread resistance for the BJT working in common emitter configuration.

The equivalent schematic of the common emitter amplifier built with BJT device including all noise sources is shown in Figure 7.6. Assuming that base spread resistance $r_{bb'}$ is much less than the input impedance of the BJT $Z_e=1/Y_e$, the current flowing through $r_{bb'}$ is roughly equal to i_b. Initially one can consider the operation of the circuit in the time domain. Using the superposition method, one can obtain the noise at the amplifier input as the following:

$$v_{ni}(t)=i_b(t)\cdot r_{bb}^{'}+v_{nb}(t)+v_{nc}(t) \tag{7.71}$$

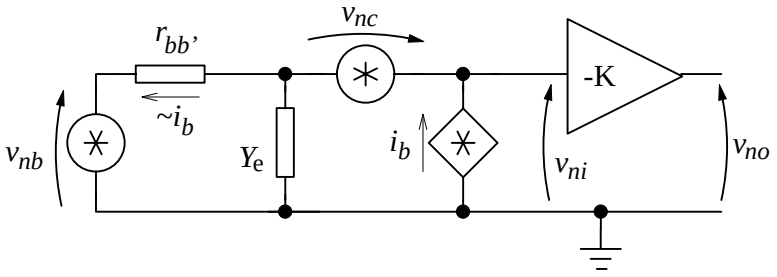


Figure 7.6: Equivalent schematics of the amplifier built with bipolar transistor working in common emitter configuration including all noise sources.

For simplicity of the calculation one can assume that the shot noise of the base current and shot noise of the collector current are uncorrelated. Therefore one can directly write the input noise spectrum density as:

$$\frac{\overline{v_{ni}^2}}{\Delta f}=\frac{\overline{i_b^2}}{\Delta f}\cdot r_{bb}^{'2}+\frac{\overline{v_{nb}^2}}{\Delta f}+\frac{\overline{v_{nc}^2}}{\Delta f}=\frac{2\cdot q\cdot I_C}{\beta}\cdot r_{bb}^{'2}+4\cdot k\cdot T\cdot r_{bb}^{'}+\frac{2\cdot k\cdot T}{g_m} \tag{7.72}$$

Provided that the term related to the base current shot noise is negligible in comparison with the other two expressions, the $r_{bb'}$ can be extracted using linear regression for the calculated equivalent noise resistance measured for various collector currents i.e. transconductance of the device. Therefore one can write:

$$\frac{\overline{v_{ni}^2}}{\Delta f}\cong 4\cdot k\cdot T\cdot R_{eq}=4\cdot k\cdot T\cdot r_{bb'}+\frac{2\cdot k\cdot T}{g_m} \tag{7.73}$$

And consequently:

$$R_{eq}=r_{bb'}+\frac{1}{2\cdot g_m} \tag{7.74}$$

The measurements of the equivalent input noise spectra for the DMILL bipolar transistors have been made in the test setup presented in Figure 7.7. The measured BJT marked on the schematic as *DUT* (*Device-Under-Test*) working in common emitter configuration is biased with different collector current using potentiometer R_b.

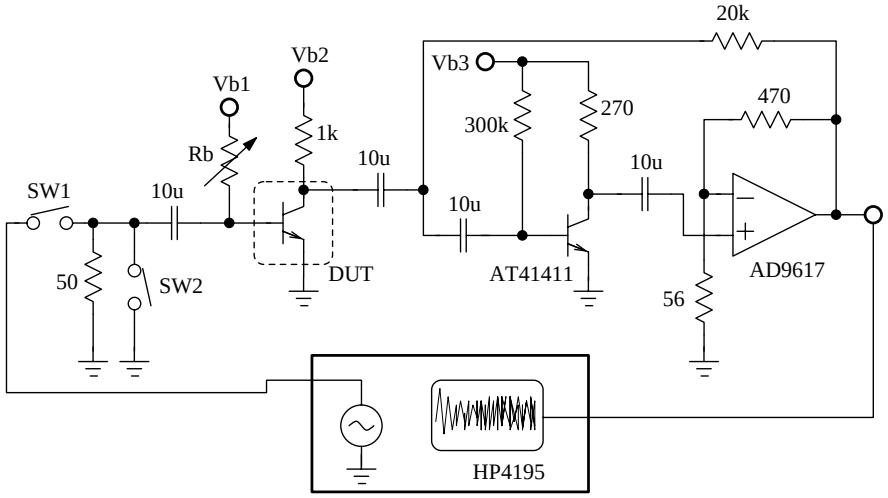


Figure 7.7: Schematic of the setup for the measurement of base spread resistance of the bipolar transistors.

A wide-bandwidth transimpedance booster amplifier is built with a low-noise BJT AT41411 device and a fast operational amplifier (AD9617) buffers the output of the measured transistor and improves the accuracy of the measurement by amplifying the noise of the *DUT*.

The core of the setup is an HP4195 programmable network-spectrum analyzer. The measurement of the equivalent input noise spectral density is done in three steps. First the HP4195 working as a network analyzer measures the frequency characteristic of the full chain with the *DUT* working as an input device biased with a given collector current (*SW1* closed, *SW2* open). In the second step, the HP4195 measures the noise spectra at the output of the amplifier with the *DUT* biased with the same collector current and input connected to AC ground (*SW1* open, *SW2* closed). In the third step the HP4195 measures the baseline noise of the setup without the *DUT* connected. The difference (calculated in square) between those two output noise spectra densities divided by the gain

characteristic of the full chain gives directly the equivalent input noise spectra density. The examples of the measured input noise spectra densities obtained for DMILL BJT 10μm×1.2μm biased with two values of the collector current are shown in Figure 7.8.

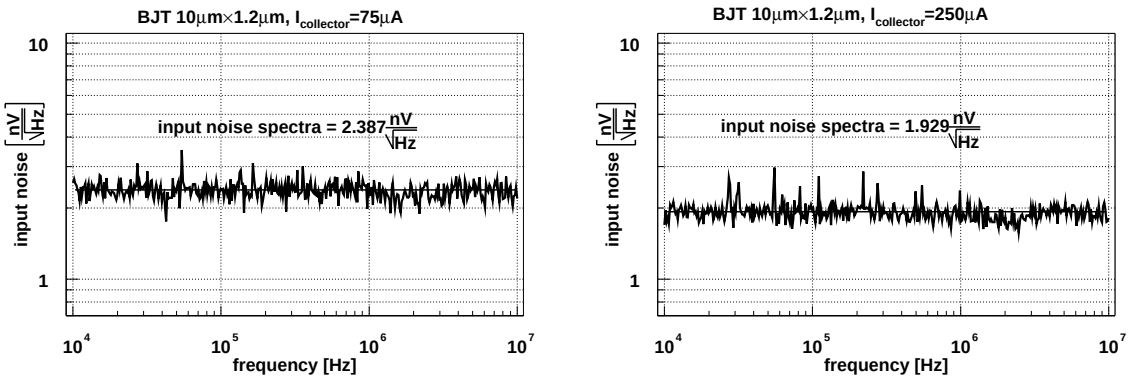


Figure 7.8: Examples of the input noise spectra for a 10μm ×1.2μm DMILL bipolar transistor working with two different collector currents.

Figure 7.9 shows the equivalent noise resistance R_{eq} for a 10μm×1.2μm DMILL BJT extracted from measured input noise spectral densities for various collector currents using equation (7.73). As we can see the $r_{bb'}$ is in the range of 180Ω. The slope of the fitted line is in the range of 13.3mV, which agrees well with the theoretical value of g_m at room temperature for the bipolar transistors ($g_m = I_C / 26mV$).

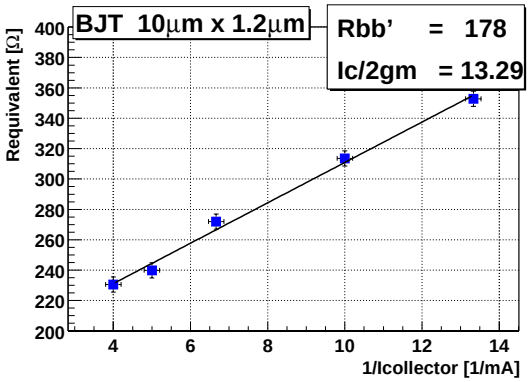


Figure 7.9: Measurement of the equivalent noise resistance for DMILL BJT (input device in SCTA and ABCD chip). The value of $r_{bb'}$ extracted from that measurement is equal to 180 Ohm.

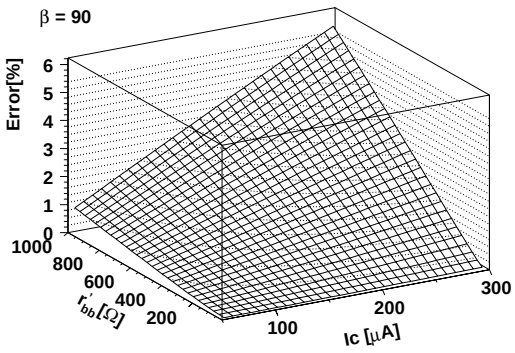


Figure 7.10: Error for the linear approximation of the equivalent noise resistance R_{eq} with respect to the $r_{bb'}$.

Figure 7.10 shows the error of the evaluation of the equivalent noise resistance R_{eq} due to the base current shot noise, defined as the following:

$$Error[\%] = \frac{\overline{i_b^2} \cdot r_{bb'}^2}{\overline{v_{ni}^2}} \qquad (7.75)$$

As can be seen, the error of the evaluation is proportional to the base current and square of the base spread resistance. For the measured bipolar transistors working with nominal bias condition and reasonable beta, with the emitter sizes 10μm×1.2μm and 2×10μm×1.2μm, where the expected $r_{bb'}$ is below 200Ω the error is below 1%, which is fully acceptable.

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