

OPTICAL FEC

Front End Control unit for Embedded Slow Control

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DRAFT



1. DOCUMENT HISTORY

000322 TIMEOUT in status reg 1 added

000330 TTCRX_READY and RESET_TTCRX added

010820 RELEASE FEC added to control reg 1. Illegal symbol generates status in receive FIFO.

020212 Due to the new TTCRx the clock for the localbus interface has been changed to the PCI clock (33MHz).

020212 The new CERN made optical receivers generate a reset signal in the absence of input signal. The reset has thus been modified to a generate a ~0.4µs long absence of signal on the serial data outputs.

030206 The Optical FEC contains a 4 channels optical tranciever on the mezzanine board and a more compact FPGA with FIFOs implemented inside.

030625 Addressing changed for FEC so that the FIFO's occupy 1 address each and the geographical addressing occupies bits [9:6]. QPLL introduced.

2. RELATED DOCUMENTS

1. CCU25 Communication and Control Unit ASIC for Embedded Slow Control
2. APV6 User Manual
3. PCI 9054 Data Book
4. TTCRx User Manual
5. Xilinx SPARTAN IIE Data Sheet
6. I2C documentation

3. GENERAL

The FEC is the Front End Control module for the slow control link in the CMS tracker. The FEC is implemented as a mezzanine module, i.e. a piggy-back board with a local bus interface. The mezzanine board can be plugged into different types of carrier board. For most test applications a PCI board is most suitable, for installation in the experiments a 9U VME board with 8 FECs is envisaged. In order to avoid electrical interference over the distance to the detector, optical links are used. The slow control links of the CMS tracker are implemented as a ring architecture. A complete ring consists of several components, first the FEC which controls the ring, then the optical drivers and receivers that bring the clock and data to the CCUs which contains the I2C masters that interface to the DCU, the APV and the PLL. The ring continues through several CCUs until the data is returned to the FEC where the status of an operation is returned

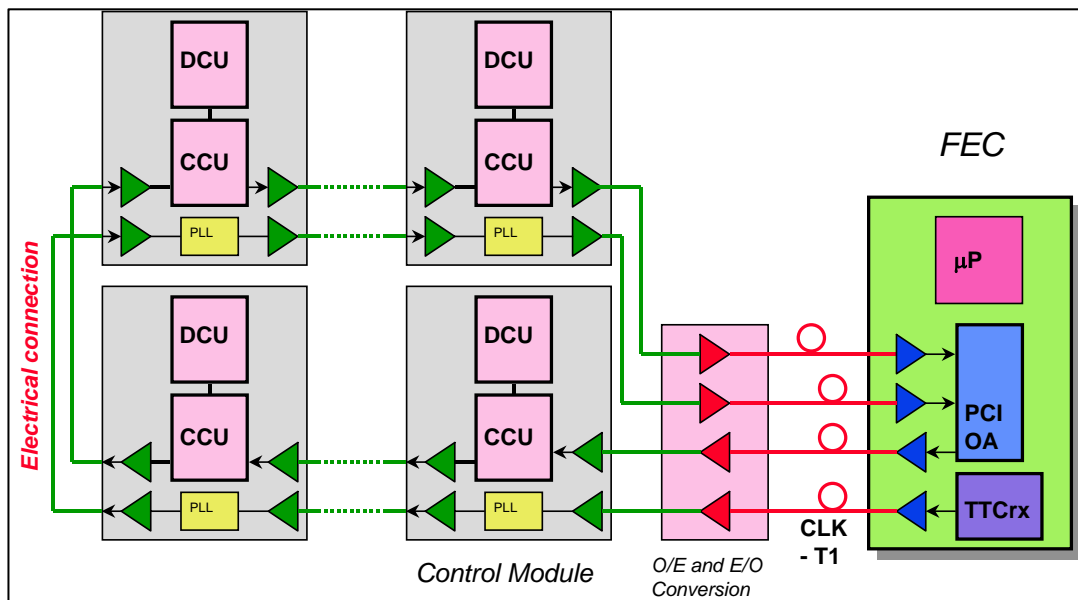


Figure 1 General block diagram

3.1. The FEC

The interface from PCI to the onboard logic is through a PLX PCI9054 chip. In the VME case a FPGA is used. The FEC controller is implemented in a Xilinx SpartanII chip which is a large FPGA. The FEC consists of a transmit FIFO for data to be sent out of the FEC onto the token-ring and a receive FIFO for data coming back from the ring. The 4b to 5b encoding and decoding is done in the FEC. The FEC also generates the CRC internally as data is transmitted, likewise the CRC is checked internally when received. This means that the FEC driver does not have to encode/decode the data neither generate nor check the CRC. There is a third FIFO used for data coming from the ring with destination FEC, this data is returned to the ring through the return FIFO. All three FIFOs can be read and written for testing purpose when the FEC is disabled. When the FEC is enabled it is only possible to write into the transmit FIFO and read from the receive FIFO.

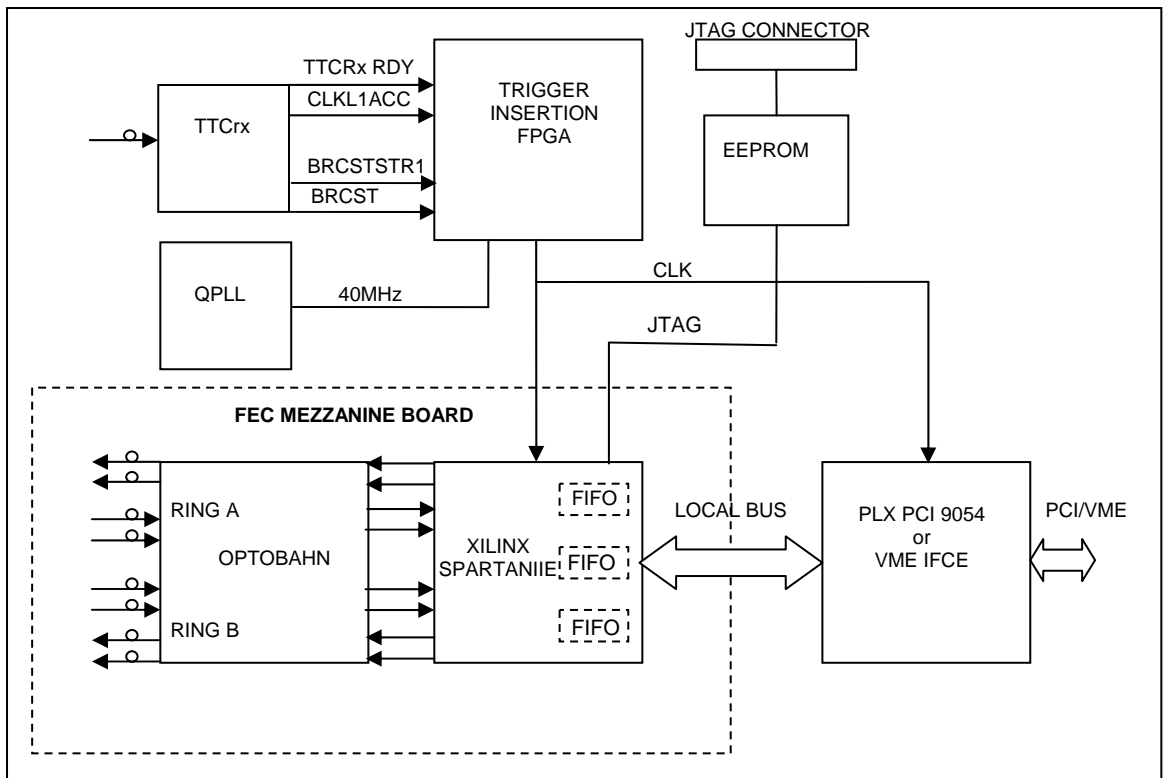


Figure 2 Optical FEC block diagram

3.1.1. PLX PCI 9054

The PCI 9054 chip is an interface chip between the host PCI bus in, and a local bus. The PLX PCI 9054 is compliant with PCI specification v2.1. The PLX PCI 9054 is register compatible with the PLX PCI 9080 as to the functions used in this application, the main difference is that the PLX PCI 9054 is 3.3v compatible. There is a choice of configuration possibilities on the local bus side, in our case it is configured as a multiplexed 32bit address/32bit data bus. For the addressing the whole 32bits are decoded. Data is 32bit wide for writing and reading in the FEC. For the moment the FEC only supports single word reads and writes but the PCI 9054 chip also contains all what is necessary to transfer data in DMA mode. The exploitation of this mechanism is however not yet implemented in the Xilinx SpartanIII chip. The default configuration of the internal registers of the PCI 9054 is stored in a serial EEPROM. This configuration can be overwritten from the host computer but care must be taken when changing the parameters.

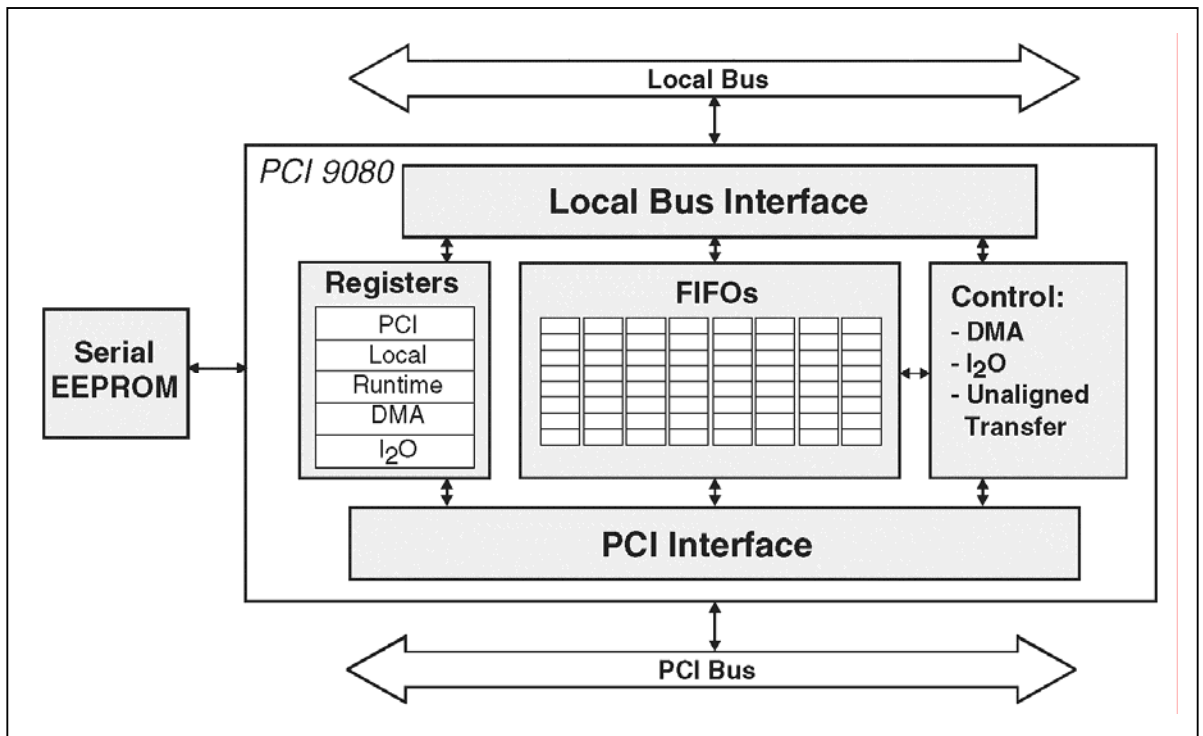


Figure 3 PLX PCI 9080/9054 block diagram

3.1.2. TTCrx

On the carrier board there is also a TTCrx module with its associated fiberoptic receiver. The default configuration for the mode of operation of the TTCrx is stored in a serial EEPROM which is loaded into the TTCrx upon power up or a reset generated from the control register 0 in the FEC. The TTCrx is used to generate the clock for the token ring as well as to insert the trigger information received on channel A. When a trigger is generated a "hole" is inserted instead of a clockpulse. There is a maximum of 3 consecutive missing clock pulses allowed in the system. The whole chains of devices connected to a ring see these missing pulses, but since the ring is a synchronous system, it is transparent to the ring devices. The local bus of the PLX 9054 chip is also driven from this clock. For devices not directly connected to the ring needing a continuous clock, a PLL is inserted to recover the continuous clock and generate trigger pulses instead of the missing pulses. When no optical fiber is present, an onboard QPLL generates the clock.

3.1.3. Trigger insertion

In order to generate special triggers or reset signals through the clock distribution an FPGA is inserted in the clock distribution after the TTCrx. The FPGA decodes commands that are broadcast on the channel B and inserts the special triggers in the clock stream by gating the CLKL1ACC with the special trigger pulses. The Trigger Insertion FPGA can also select a locally generated clock from a QPLL chip if no TTC fiber is available. At power up the QPLL oscillator is chosen by default. If the TTC_Ready signal goes active the output is switched over to the CLKL1ACC clock. If the TTC_Ready signal is present it is possible to switch over to the QPLL clock through a control bit in the FEC.

3.1.4. Addressing of the FEC

The addresses for the various registers and FIFOs are decoded from the 32 bit address on the local bus side of the PLX 9054. Seen from the PCI side these addresses are mapped into the memory space through a register called PCI Base Address Register for Local Space X (PCIBARX). The data words on the local bus are always 32 bits wide in the FEC. To be able to address multiple FECs on a VME64x card, each FEC has an individual geographic address assigned through biasing of 4 pins high or low. This geographical address is compared against address bits [9:6] on the local bus. Each FEC occupies 16 words, 32x0000_0000 to 32x0000_003C, out of which 8 are not used in this implementation but reserved for future use. The address space occupied by 8 FECs thus run from 32x0000_0000 to 32x0000_01FC. Between 32x0000_0200 and 32x0000_03FC the address space is reserved for the ECAL trigger logic. At address 32x0000_0400 is placed the interrupt vector consisting of 8 bits out of which the 5 most significant bits are derived from the geographical address in the crate and the 3 least significant bits contains the interrupting M-FEC number. At address 32x0000_0404 is placed a 16bit status word, which contains the geographical address of the VME-FEC card the status of the 8 M-FEC interrupt lines.

REGISTER	LOCAL_ADDR	PCI_ADDR_OFFSET	ACCESS
CONTROL0	32x0000_0000	16x0000	READ/WRITE bits [15:0]
CONTROL1	32x0000_0004	16x0001	WRITE ONLY bits [2:0]
STATUS0	32x0000_0008	16x0002	READ ONLY bits [14:0]
STATUS1	32x0000_000C	16x0003	READ ONLY bits [7:0]
SOURCE	32x0000_0010	16x0004	READ WRITE bits [6:0]
VERSION	32x0000_0010	16x0004	READ ONLY bits [15:8]
TRA-FIFO	32x0000_0020	16x0008	READ WRITE bits [31:0]
RET-FIFO	32x0000_0024	16x0009	READ WRITE bits [7:0]
REC-FIFO	32x0000_0028	16x000C	READ WRITE bits [31:0]

Figure 4 Addressing of the FEC

3.1.5. VME64x registers

Through the Plug and play mechanism the capabilities of the VME-FEC is determined. Before accessing user data, each card should be assigned a base-address and enabled.

3.2. Mode of operation

The normal mode of operation for the FEC is as follows. When an action is to be performed on a unit connected to the ring one first makes sure that the link is initialized and that no pending operation is active. A data frame is then prepared and written word by word (32bits) into the transmit FIFO. When the frame has been written the SEND bit in the control register 0 is toggled. The FEC then waits for a token to replace it by the data frame present in the transmit FIFO. Once the token is grabbed the status register 0 indicates TRANSMIT RUNNING. Depending on the ring delay the transmitted data will then start returning to the FEC at which point the status register 0 indicates RECEIVE RUNNING. Data will then be assembled into 32bit words and written into the receive FIFO. Normal ring delay is around (8x25 x #ofCCU) ns so the delays are normally rather short, i.e. in the order of microseconds. Once the whole message is returned the last word is written together with the status of the frame, i.e. Error, Address seen and Data copied. If errors have been detected in the FEC the status is signaled as CRC error, Illegal sequence or Illegal data depending of the case. In case packets return with the Data copied bit set to 0 that indicates that the addressed channel was busy and the packet should be retransmitted. The retransmission is not done

automatically in hardware but should be taken care of in the software. When the last word has been written into the receive FIFO the FEC sends an IRQ to the PCI 9054 which can be fed through to the host computer if this function is enabled in the PCI 9054 chip. If the interrupt function is not enabled it is possible to poll the status register0. Once the IRQ has been seen the CLEAR IRQ has to be sent to control register 1 to indicate that the IRQ has been taken care of. The two status bits mentioned before, TRANSMIT and RECEIVE RUNNING, are active only during the time needed for transmitting or receiving the data frame so if they are permanently on there is a problem somewhere. Together with the IRQ there is an indication in the status register if the frame is a returned frame or a frame destined for the FEC.

3.3. Control registers.

The operation of the FEC is controlled through two control registers.

3.3.1. Control register 0.

The main operation of the FEC is controlled through the control reg0 at address 0. For the time being there are 10 bits used. As more functionality is added more bits could be implemented.

The control register 0 is read-write. The following bits are defined:

15	14	8	7	6	5	4	3	2	1	0
RESET OUT	RESET LINK B	DISABLE RECEIVE	SEL REC CK POL	RESET TTCRX	NOT USED	SELECT SERIAL IN	SEL SERIAL OUT	SEL XTAL CLOCK	SEND	ENABLE FEC

Figure 5 Defined bits in control register 0

The function of each bit in the control register 0 is explained in the table below.

Bit	Name	Function
15	RESET_OUT	By setting this bit a 0.4μs reset pulse is transmitted, i.e. the serial data out is blocked for 0.4μs. If an optical link with the CERN developed receivers is used, the receiver generates the reset pulse during absence of signal on the input. This bit is or-ed with the LRESETo from the PCI 9054. The default value is "0" (no reset). It is automatically returned to its default state. This bit is always read as "0".
14	RESET LINK B	Works as RESET_OUT except it generates a reset pulse on link B. The default value is "0" (no reset). This bit is always read as "0".
8	DISABLE RECEIVE	Disables all FEC writes to the receive fifo. This is useful e.g. during reconfiguration of a non closed ring.
7	SEL RECEIVE CLOCK POLARITY	If delays in the data and clock chain for some reason are mismatched clocking on the other edge might help.
6	RESET_TTCrx	By toggling this bit the TTCRX is reset. After the TTCrx is reset the CCUs and PLLs should be reset after the TTCRX_READY bit is set. This bit is or-ed with the LRESETo from the PLX PCI9054. The default value is "0" (no reset).
5	NOT USED	
4	SELECT SERIAL IN	Enables one of the two serial data inputs used for redundancy. Writing a "1" in this bit enables SER_IN_B. The default value is "0" (SER_IN_A enabled).
3	SELECT SERIAL OUT	Enables one of the two serial data outputs used for redundancy. The non-enabled output is at a fixed "0" level. Writing a "1" in this bit enables SER_OUT_B. The default value is "0" (SER_OUT_A enabled).
2	SEL XTAL CLOCK	During power up the Trigger insertion chip on the carrier board selects the Xtal clock. If the TTCrx is operational and the TTCrx_READY signal activated the TTCrx clock is selected automatically. If for some reason it is preferred to use the Xtal clock it is possible to select it with this bit. If the TTCrx READY signal is not present it is not possible to chose the TTCrx clock. The default value is "0" (TTCrx clock selected).
1	SEND	By toggling this bit the data present in the TRANSMIT FIFO is transmitted. The data is assumed to be logically and syntactically correct since no further checking is undertaken in the FEC. The default value is "0".
0	EN_FEC	Writing a "1" to this bit enables the transmission of data already present in the TRANSMIT FIFO. At the same time WRITE operations from PCI to the RETURN FIFO and the RECEIVE FIFO are disabled like the READ operations from PCI to the TRANSMIT FIFO and the RETURN FIFO. This bit must be set to "1" before or at the same time as the SEND or RESEND bits are set to "1". The default value is "0".

Figure 6 Function of control register 0

3.3.2. Remark on RESET

At power up or booting of the host CPU a PCI reset is generated which causes activation of LRESETo. LRESETo is the master reset for the Xilinx SpartanIIe which in its turn generates the two signals RESET_OUT and RESET_TTCRX. To reset the FEC and the FIFOs when the host CPU is up and running the PLX PCI 9054 CNTRL register (PCI:6Ch bit 30) should be toggled. This generates the LRESETo signal. After toggling PCI:6Ch bit 30 the default values from the EPROM are loaded into the PLX PCI 9054 which imposes a pause before accessing the FEC again. Any special configurations not included in the default EPROM of the PLX PCI 9054 must subsequently be repeated by writing into the corresponding configuration registers. A jumper on the carrier board allows the reloading of the configuration data into the Xilinx SpartanIIe chip when a LRESETo is generated. Reloading implies a deadtime of approximately 0.5s. In order to be sure that the PLLs are properly locked RESET_OUT (CONTROL0[15] or CONTROL0[9]) should not be toggled until STATUS0[14] indicates TTC_READY when the TTCRx is used as the system clock.

3.3.3. Control register 1.

Control reg1 at address 4 is used to clear the level sensitive interrupt generated by the FEC and the error indicators in status register1.

The control register 1 is write only since the bits are automatically cleared. The following bits are defined:

2	1	0
RELEASE FEC	CLEAR ERROR BITS	CLEAR INTERRU PT

Figure 7 Defined bits in control register 1

The function of each bit in the control register 1 is explained in the table below

Bit	Name	Function
2	RELEASE FEC	By writing a 1 to this register the FEC generates a token and stops waiting for a return packet. This is intended to be used in case the ring is opened during redundancy reconfiguring for example. The control register is automatically reset after the operation.
1	CLEAR ERROR BITS	By writing a 1 to this register the bits [2:0] in STATUS REG1 are cleared. The control register is automatically reset after the operation.
0	CLEAR INTERRUPT	By writing a 1 to this register the bits PENDING IRQ and DATA TO FEC (bits [13:12]) are cleared as well as bits [6:3] in STATUS REG1. The control register is automatically reset after the operation.

Figure 8 Function of control register 1

3.4. Status registers.

The result of an operation in the FEC can be determined through the status registers.

3.4.1. Status register 0.

The status register0 at address 8 contains 14 bits right now, but more bits might be added in the future if necessary.

The status register is read only. The following bits are defined:

14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TTCRX READY	DATA TO FEC	PENDING IRQ	LINK INITIALIZED	TRANSMIT FIFO EMPTY	TRANSMIT FIFO FULL	NOT USED	RETURN FIFO EMPTY	RETURN FIFO FULL	NOT USED	RECEIVE FIFO EMPTY	RECEIVE FIFO FULL	NOT USED	RECEIVE RUNNING	TRANSMIT RUNNING

Figure 9 Status register 0

The function of each bit in the status register 0 is explained in the table below

Bit	Name	Function
14	TTCRX READY	This bit is set when the TTCRX is locked
13	DATA TO FEC	This bit is set when the last byte of an incoming message destined for the FEC is written into the RECEIVE FIFO. Since it is destined to the FEC it is also written into the RETURN FIFO to be circulated back to the source. This makes it possible to distinguish between messages destined to the FEC and messages destined to a CCU and returning to the FEC. The bit is cleared by writing a "1" to CONTROL REGISTER1[0].
12	PENDING IRQ	This bit follows the local interrupt transmitted to the PLX PCI9054. An interrupt is generated when the last byte of an incoming message is written into the RECEIVE FIFO. The interrupt is cleared by writing a "1" to CONTROL REGISTER1[0].
11	LINK INITIALIZED	This bit is "0" until the FEC has transmitted 512 bytes of "IDLE " symbols in order to initialize the optical link and received the first TOKEN back.
10	TRANSMIT FIFO EMPTY	This bit follows the empty flag from the TRANSMIT FIFO but is high active. PCI read operations when empty produce FFFF as data.
9	TRANSMIT FIFO FULL	This bit follows the full flag from the TRANSMIT FIFO but is high active
8	NOT USED	
7	RETURN FIFO EMPTY	This bit follows the empty flag from the RETURN FIFO but is high active. PCI read operations when empty produce FFFF as data.
6	RETURN FIFO FULL	This bit follows the full flag from the RETURN FIFO but is high active.
5	NOT USED	
4	RECEIVE FIFO EMPTY	This bit follows the empty flag from the RECEIVE FIFO but is high active. PCI read operations when empty produce FFFF as data.
3	RECEIVE FIFO FULL	This bit follows the full flag from the RECEIVE FIFO but is high active.
2	NOT USED	
1	RECEIVE RUNNING	This bit is "1" when data is being written into the RECEIVE FIFO. The status bit goes to "0" between frames and during tokens and idle characters.
0	TRANSMIT RUNNING	This bit is "1" if EN FEC is set and a SEND command has been issued. TRANSMIT RUNNING stays "1" until the TRANSMIT FIFO is empty and the EOF has been transmitted. The TRANSMIT FIFO should not be refilled before TRANSMIT RUNNING has gone to "0" unless the writing speed to the TRANSMIT FIFO is guaranteed to exceed the reading speed of the FEC.

Figure 10 Function of status register 0

3.4.2. Status register 1.

The status register1 at address 3 contains 6 bits right now, but more bits might be added in the future if necessary.

The status register 1 is read-only. The following bits are defined.

7	6	5	4	3	2	1	0
CLOCK ERROR	TIMEOUT	ERROR	ADDRESS SEEN	DATA COPIED	CRC ERROR	ILLEGAL SEQUENCE	ILLEGAL DATA

Figure 11 Defined bits in status register 1

The function of each bit in the status register 1 is explained in the table below.

Bit	Name	Function
7	CLOCK ERROR	This bit indicates that a difference (>4) in the number of active transitions between the transmitted clock and the received clock has been detected. This can happen e.g. if the power of the return laser has been reduced too much. This bit is cleared by writing a "1" to CONTROL REGISTER 1[1]
6	TIMEOUT	This bit is set if a TIMEOUT has been detected, i.e. the FEC has not seen a token or data frame during the timeout period which is ~500µs This bit is cleared by writing a "1" to CONTROL REGISTER 1[1]
5	ERROR	This bit corresponds to the error symbol in the End of Frame that is transmitted after data (TRRR) It indicates that a CRC error or some other error has been detected in a CCU. This bit is cleared together with the IRQ.
4	ADDRESS SEEN	This bit corresponds to the address seen symbol in the End of Frame that is transmitted after data (TRRR) It indicates that the destination has been addressed. This bit is cleared together with the IRQ.
3	DATA COPIED	This bit corresponds to the data copied symbol in the End of Frame that is transmitted after data (TRRR) It indicates that the destination has accepted the frame. This bit is cleared together with the IRQ.
2	CRC ERROR	Indicates that a CRC error has been detected in the FEC. If set this bit stays on until intentionally cleared. This bit is cleared by writing a "1" to CONTROL REGISTER 1[1]
1	ILLEGAL SEQUENCE	Indicates that an illegal symbol sequence has been detected in the FEC. If set this bit stays on until intentionally cleared. This bit is cleared by writing a "1" to CONTROL REGISTER 1[1].
0	ILLEGAL DATA	Indicates that an illegal symbol has been detected in the FEC. If set this bit stays on until intentionally cleared. This bit is cleared by writing a "1" to CONTROL REGISTER 1[1].

Figure 12 Function of status register 1

3.4.3. Source register

The source register is used for testing purposes. It is an 7 bit register (bit[6:0]) It replaces the default source (7x00) normally used by the FEC.

3.4.4. Version register

The version register contains the firmware version of the FEC. It is used to distinguish between different versions of the internal implementation of the FEC. It is a read only register. It is read together with the source register in bit positions [15:8].

3.5. Token ring packet Format

Two basic packet types are foreseen, one for signaling availability of the ring and the second to actually carry data.

The network token format is defined as:

SOF [1 B]	EOF [2 B]
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Figure 13 Token packet format

The network data packet format is defined below:

SOF [1B]	Destination DAddress [1 B]	Source SAddress [1 B]	Length [1/2 B]	Data [<128/32K B]	CRC-16 [2 B]	EOF [2 B]
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Figure 14 Data packet format

The Start of Frame (SOF), End of Frame (EOF), Source and Destination fields are mandatory for all circulating data packets.

The SOF field is defined as the unique “J-H/K” sequence, using the two special characters defined in the “Figure 20 Control characters in network”.

The SOF field is defined as follows:

Symbol	Name	Comment
0	J	Special symbol used for synchronisation
1	H/K	K used to mark token packet H used to mark normal data packet

Figure 15 Frame Header format

The End of Frame (EOF) field consists of two bytes and is defined as follows:

End Delimiter [0.5 B]	Frame Status [1.5 B]
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Figure 16 EOF definition

The End Delimiter consists of a single “T” character as defined in the Figure 20 Control characters in network. The Frame status is generated by the transmitter as three “R” characters and contains the three following sub-fields:

Symbol	Value	Comment
ER	R/S	Error symbol
AR	R/S	Address recognised
DC	R/S	Data copied

Figure 17 The EOF frame

These symbols are set by the receiving node; they are generated as “R” symbols from the source and modified to “S” by the receiver.

The Length field can be one or two bytes long and gives the length of the data payload, excluding the two length bytes themselves and the CRC field.

When the high bit [bit 7] of the first byte is '0' the length of the field is one byte only and the maximum payload can be 0-127 bytes long. When the high bit is a '1', the length field is two bytes long and the data payload can be 0-32K long.

The Data field is not interpreted by the ring protocol and is used exclusively by the channel adapter (CCU 25) for internal addressing and data. These fields are defined explicitly by the functionality of each channel. The CCU 25 documentation contains the details.

The data portion of the packet is shown below:

CH#	TR#	Channel Specific Command
[1 B]	[1 B]	[(Length-2) B]

Figure 18 Data portion of packet

Two data bytes are mandatory as payload at the beginning of each data packet:

- a channel number (single byte field), used to identify a device channel within a node
- a transaction number (single byte field with wrap-around) used to assure correct identification of operation within a given channel. This field is always generated by the initiator of a transaction.

For transactions initiated by the FEC, the transaction number should always be in the range 1-255, as the special transaction number 0 is used for Alarms generated by the CCUs.

The CRC-16 field covers the packet content from the Destination address to the end of the Data field. The polynomial used for the CRC-16 calculations is:

$$X^{16} + X^{15} + X^2 + 1$$

3.5.1. Data encoding

Data on the data line are qualified by the rising edge of the clock signal. In addition, the data bits on the data line will be transmitted using 4bit to 5bit encoding, using a NRZI (Non Return to Zero with Invert 1 on change) signaling scheme as follows:

4 bit Binary	Hex Value	5 bit Symbol
0000	0	11110
0001	1	01001
0010	2	10100
0011	3	10101
0100	4	01010
0101	5	01011
0110	6	01110
0111	7	01111
1000	8	10010
1001	9	10011
1010	A	10110
1011	B	10111
1100	C	11010
1101	D	11011
1110	E	11100
1111	F	11101

Figure 19 4B/5B encoding

This encoding scheme has been chosen because it requires very limited hardware resources and can be easily implemented in hardware. The worst case DC unbalance deriving from the usage of this coding is estimated to be about 10%.

The control symbols are defined as follows:

Control Symbol	Code	Comment
Idle	11111	Idle
J	11000	In SOF field
K	10001	in SOF field
H	00100	Special
R	00111	Reset
S	11001	Set
T	01101	Termination

Figure 20 Control characters in network

3.5.2. The NRZI signaling scheme

Basically, this scheme uses a line transition to represent a "1" and no transition to represent a "0". The 4B/5B symbols used above are made such that there are never more than 3 consecutive zeros in the line, assuring an adequate number of line transitions, to avoid large DC shifts.

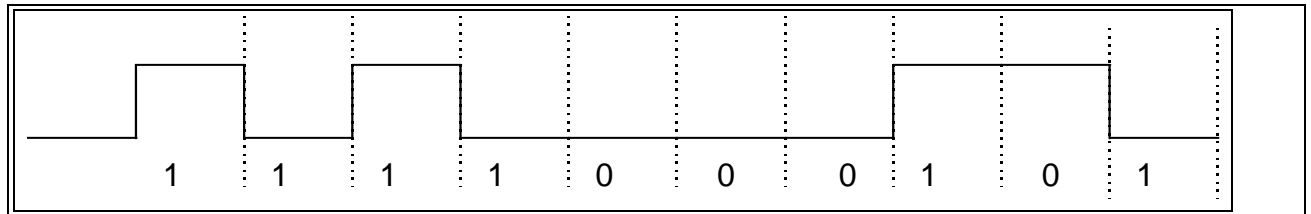


Figure 21 NRZI encoding format

3.6. Transmit FIFO data structure

The organization of data packets for the TRANSMIT FIFO is shown below. Access to the TRANSMIT FIFO is through 32bit word access. Several packets can be written one after the other, provided padding is used so that each new message starts on a word boundary. The data packets are embedded into a token ring frame by the FEC through adding the control symbols for SOF and EOF. While sending out a frame the CRC is calculated and inserted after the last data byte.

3.6.1. Transmit FIFO data structure

BITS [31:24]	BITS [23:16]	BITS [15:8]	BITS [7:0]
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	DATA	PADDING
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	DATA	DATA
DATA	PADDING	PADDING	PADDING
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	DATA	PADDING

Figure 22 Transmit FIFO data structure

3.7. Receive FIFO data structure

The organization of the receive fifo is similar to the transmit fifo but one byte containing the status is added after the last byte in the frame. Several messages can be stored consecutively in the receive FIFO, the size of the fifo being 512 words. In case an error is detected in a frame, the FEC writes the status byte in bits [7:0] with padding (0) in the remaining bits.

3.7.1. Receive FIFO data structure

BITS [31:24]	BITS [23:16]	BITS [15:8]	BITS [7:0]
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	STATUS	PADDING
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	DATA	DATA
DATA	STATUS	PADDING	PADDING
DESTINATION	SOURCE	LENGTH	DATA
DATA	DATA	DATA	STATUS

Figure 23 Receive FIFO data structure

3.7.2. Received data status

The bits [6:4] should be 011 for a frame that is returning to the FEC, i.e. it was originated in the FEC. In a frame destined for the FEC the bits [6:4] should be 000. Bits [3:1] correspond to errors in the data stream detected in the FEC.

If an illegal symbol or an illegal sequence of symbols is encountered, a data word (STATUS) is immediately written to the receive fifo. The status word is 32 bits long and the layout is 32'h {00, 00, 01, STATUS}. This word can be interpreted like a FEC frame, DEST = 00, SOURCE = 00, LENGTH = 01, DATA = STATUS. The receive fifo will contain either a truncated message and the status or just the status, depending on when the error occurred. When the status has been written the FEC waits for a new message.

BIT	FUNCTION
7	HIGH
6	ERROR
5	ADDR SEEN
4	DATA COPIED
3	CRC_ERROR
2	ILLEGAL SEQUENCE
1	ILLEGAL DATA
0	NOT USED (LOW)

Figure 24 Receive status

3.8. FEC power consumption

The power consumption of the FEC is ~0.5 A on the +3.3V supply.

3.9. FEC physical layout

4. LIST OF FIGURES

Figure 1 General block diagram	4
Figure 2 Optical FEC block diagram	5
Figure 3 PCI 9080/9054 block diagram	6
Figure 4 Addressing of the FEC	7
Figure 5 Defined bits in control register 0	8
Figure 6 Function of control register 0	9
Figure 7 Defined bits in control register 1	10
Figure 8 Function of control register 1	10
Figure 9 Status register 0/1	
Figure 10 Function of status register 0	13
Figure 11 Defined bits in status register 1	13
Figure 12 Function of status register 1	14
Figure 13 Token packet format	15
Figure 14 Data packet format	15
Figure 15 Frame Header format	15
Figure 16 EOF definition	15
Figure 17 The EOF frame	15
Figure 18 Data portion of packet	16
Figure 19 4B/5B encoding	17
Figure 20 Control characters in network	17
Figure 21 NRZI encoding format	18
Figure 22 Transmit FIFO data structure	18
Figure 23 Receive FIFO data structure	19
Figure 24 Receive status	19

5.	INDEX	
1.	<i>Document History</i>	2
2.	<i>Related documents</i>	3
3.	<i>General</i>	4
3.1.	The FEC	4
3.1.1.	PLX PCI 9054	5
3.1.2.	TTCrx	6
3.1.3.	Trigger insertion	6
3.1.4.	Addressing of the FEC	7
3.2.	Mode of operation	7
3.3.	Control registers.	8
3.3.1.	Control register 0.	8
3.3.2.	Remark on RESET	10
3.3.3.	Control register 1.	10
3.4.	Status registers.	11
3.4.1.	Status register 0.	11
3.4.2.	Status register 1.	13
3.4.3.	Source register	14
3.4.4.	Version register	14
3.5.	Token ring packet Format	15
3.5.1.	Data encoding	16
3.5.2.	The NRZI signaling scheme	17
3.6.	Transmit FIFO data structure	18
3.6.1.	Transmit data structure	18
3.7.	Receive FIFO data structure	18
3.7.1.	Receive data structure	19
3.7.2.	Received data status	19
3.8.	FEC power consumption	19
3.9.	FEC physical layout	19
4.	<i>LIST OF FIGURES</i>	21
5.	<i>INDEX</i>	22